

JURY, PATENT

U.S. District Court [LIVE]
Eastern District of TEXAS LIVE (Marshall)
CIVIL DOCKET FOR CASE #: 2:06-cv-00151-TJW

07-187

Fairchild Semiconductor Corporation et al v. Power Integrations, Inc.
Assigned to: Judge T. John Ward
Cause: 28:1338 Patent Infringement
Date Filed: 04/11/2006
Jury Demand: Both
Nature of Suit: 830 Patent
Jurisdiction: Federal Question

Plaintiff

Fairchild Semiconductor Corporation
a Delaware Corporation

represented by **G Hopkins Guy, III**
Orrick Herrington & Sutcliffe -
Menlo Park
1000 Marsh Rd
Menlo Park, CA 94025
650/614-7452
Fax: 16506147401
Email: hopguy@orrick.com
LEAD ATTORNEY
ATTORNEY TO BE NOTICED

Bas de Blank
Orrick Herrington & Sutcliffe -
Menlo Park
1000 Marsh Rd
Menlo Park, CA 94025
650/614-7400
Fax: 650/614-7401
Email: basdeblank@orrick.com
ATTORNEY TO BE NOTICED

Gabriel M Ramsey
Orrick Herrington & Sutcliffe -
Menlo Park
1000 Marsh Rd
Menlo Park, CA 94025
650/614-7400
Fax: 16506147401
Email: gramsey@orrick.com
ATTORNEY TO BE NOTICED

A TRUE COPY I CERTIFY
DAVID MALAND, CLERK
U.S. DISTRICT COURT
EASTERN DISTRICT, TEXAS

By: 

Michael Charles Smith
The Roth Law Firm
115 N. Wellington
Suite 200
P.O. Box 876
Marshall, TX 75671-0876
US
903/935-1665
Fax: 19039351797
Email: ms@rothfirm.com
ATTORNEY TO BE NOTICED

Vickie L Feeman
Orrick Herrington & Sutcliffe -
Menlo Park
1000 Marsh Rd
Menlo Park, CA 94025
650/614-7400
Fax: 650/614-7401
Email: vfeeman@orrick.com
ATTORNEY TO BE NOTICED

Plaintiff

Intersil Corporation
a Delaware Corporation

represented by **G Hopkins Guy, III**
(See above for address)
LEAD ATTORNEY
ATTORNEY TO BE NOTICED

Jeffrey Ray Bragalone
Shore Chan Bragalone
325 N St Paul St
Suite 4450
Dallas, TX 75201
(214) 593-9110
Fax: (214) 593-9111
Email:
jbragalone@shorechan.com
LEAD ATTORNEY
ATTORNEY TO BE NOTICED

Michael Wayne Shore
Shore Chan Bragalone

325 N St Paul St
Suite 4450
Dallas, TX 75201
(214) 593-9110
Fax: (214) 593-9111
Email: shore@shorechan.com
LEAD ATTORNEY
ATTORNEY TO BE NOTICED

Gabriel M Ramsey
(See above for address)
ATTORNEY TO BE NOTICED

Joseph F DePumpo
Shore Chan Bragalone
325 N St Paul St
Suite 4450
Dallas, TX 75201
(214) 593-9110
Fax: (214) 593-9111
Email: jdepumpo@shorechan.com

ATTORNEY TO BE NOTICED

Michael Charles Smith
(See above for address)
ATTORNEY TO BE NOTICED

V.

Defendant

Power Integrations, Inc.
a Delaware Corporation

represented by **Allen Franklin Gardner**
Potter Minton PC
110 N College
Suite 500
PO Box 359
Tyler, TX 75710-0359
903/597-8311
Email:
allengardner@potterminton.com
ATTORNEY TO BE NOTICED

Frank E Scherkenbach

Fish & Richardson PC - Boston
225 Franklin St
Boston, MA 02110
617/542-5070
Fax: 617/542-8906
Email: scherkenbach@fr.com
ATTORNEY TO BE NOTICED

Howard G Pollack
Fish & Richardson - Redwood
City
500 Arguello St
Suite 500
Redwood City, CA 94063
650/839-5070
Fax: 650/839-5071
Email: pollack@fr.com
ATTORNEY TO BE NOTICED

James Matthew Rowan
Potter Minton
P. O. Box 359
Tyler, TX 75710
903/597/8311
Fax: 19035930846
Email:
mattrowan@potterminton.com
ATTORNEY TO BE NOTICED

Michael R Headley
Fish & Richardson - Redwood
City
500 Arguello St
Suite 500
Redwood City, CA 94063
650/839-5070
Fax: 650/839-5071
Email: headley@fr.com
ATTORNEY TO BE NOTICED

Michael Edwin Jones
Potter Minton PC
110 N College

Suite 500
 PO Box 359
 Tyler, TX 75710-0359
 903/597/8311
 Fax: 9035930846
 Email:
 mikejones@potterminton.com
ATTORNEY TO BE NOTICED

Date Filed	#	Docket Text
04/11/2006	<u>1</u>	COMPLAINT against Power Integrations, Inc. (Filing fee \$ 350.) , filed by Fairchild Semiconductor Corporation, Intersil Corporation. (Attachments: # (1) Civil Cover Sheet)(ehs,) (Entered: 04/11/2006)
04/11/2006	<u>2</u>	DEMAND for Trial by Jury by Fairchild Semiconductor Corporation, Intersil Corporation. (ehs,) (Entered: 04/11/2006)
04/11/2006	<u>3</u>	Summons Issued as to Power Integrations, Inc. (ehs,) (Entered: 04/11/2006)
04/11/2006	<u>4</u>	Form mailed to Commissioner of Patents and Trademarks. (ehs,) (Entered: 04/11/2006)
04/11/2006	<u>5</u>	Filing fee: \$ 250.00, receipt number 2-1-1354 (ehs,) (Entered: 04/11/2006)
04/11/2006	<u>6</u>	Filing fee: \$ 100.00, receipt number 2-1-1362 (ehs,) (Entered: 04/12/2006)
04/12/2006	<u>7</u>	NOTICE of Attorney Appearance by Michael Charles Smith on behalf of Fairchild Semiconductor Corporation, Intersil Corporation (Smith, Michael) (Entered: 04/12/2006)
04/21/2006	<u>8</u>	NOTICE of Attorney Appearance by Michael Edwin Jones on behalf of Power Integrations, Inc. (Jones, Michael) (Entered: 04/21/2006)
04/21/2006	<u>9</u>	SUMMONS Returned Executed by Intersil Corporation. Power Integrations, Inc. served on 4/12/2006, answer due 5/2/2006. (ehs,) (Entered: 04/21/2006)
05/01/2006	<u>10</u>	MOTION for Extension of Time to File Answer re <u>1</u> Complaint (<i>Agreed Motion for Extension of Time to Answer</i> ,

		<i>Move or Otherwise Respond</i>) by Power Integrations, Inc.. (Attachments: # <u>1</u> Text of Proposed Order)(Jones, Michael) (Entered: 05/01/2006)
05/02/2006	<u>7</u>	ORDER granting <u>6</u> Motion for Extension of Time to Answer Deadline is 6/1/06. Signed by Judge T. John Ward on 5/2/06. (ch,) (Entered: 05/02/2006)
05/02/2006		Answer Due Deadline Updated for Power Integrations, Inc. to 6/1/2006. (ch,) (Entered: 05/02/2006)
05/19/2006	<u>8</u>	AMENDED COMPLAINT against Power Integrations, Inc., filed by Fairchild Semiconductor Corporation, Intersil Corporation. (Attachments: # <u>1</u> Exhibit A# <u>2</u> Exhibit B# <u>3</u> Exhibit C# <u>4</u> Exhibit D# <u>5</u> Exhibit E# <u>6</u> Exhibit F)(Smith, Michael) (Entered: 05/19/2006)
06/02/2006	<u>9</u>	MOTION for Extension of Time to File Answer re <u>8</u> Amended Complaint by Power Integrations, Inc.. (Attachments: # <u>1</u> Text of Proposed Order)(Jones, Michael) (Entered: 06/02/2006)
06/09/2006	<u>10</u>	ORDER granting <u>9</u> Motion for Extension of Time to Answer. Power Intergrations deadline to answer is extended to 6/19/06 . Signed by Judge T. John Ward on 6/9/06. (ch,) (Entered: 06/09/2006)
06/09/2006		Answer Due Deadline Updated for Power Integrations, Inc. to 6/19/2006. (ch,) (Entered: 06/09/2006)
06/19/2006	<u>11</u>	<i>Power Integrations, Inc.'s</i> ANSWER to Amended Complaint by Power Integrations, Inc..(Jones, Michael) (Entered: 06/19/2006)
06/19/2006	<u>12</u>	***FILED IN ERROR; PLEASE IGNORE*** MOTION to Dismiss <i>or, in the Alternative, to Transfer this Case to Delaware</i> by Power Integrations, Inc.. (Attachments: # <u>1</u> Declaration of Michael E. Jones# <u>2</u> Exhibit A to Declaration of M. Jones# <u>3</u> Exhibit B to Declaration of M. Jones# <u>4</u> Exhibit C to Declaration of M. Jones# <u>5</u> Exhibit D to Declaration of M. Jones# <u>6</u> Exhibit E to Declaration of M. Jones# <u>7</u> Exhibit F to Declaration of M. Jones# <u>8</u> Exhibit G to Declaration of M. Jones# <u>9</u> Exhibit H to Declaration of M. Jones# <u>10</u> Appendix 1# <u>11</u> Text of Proposed Order)(Jones, Michael) Modified on 6/20/2006 (mpv,). (Entered: 06/19/2006)

06/19/2006	● <u>13</u>	CORPORATE DISCLOSURE STATEMENT filed by Power Integrations, Inc. (Jones, Michael) (Entered: 06/19/2006)
06/19/2006	● <u>14</u>	***REPLACES #12*** MOTION to Dismiss <i>or, in the Alternative, to Transfer this Case to Delaware</i> by Power Integrations, Inc.. (Attachments: # <u>1</u> Declaration of Mike Jones# <u>2</u> Exhibit A# <u>3</u> Exhibit B# <u>4</u> Exhibit C# <u>5</u> Exhibit D# <u>6</u> Exhibit E# <u>7</u> Exhibit F# <u>8</u> Exhibit G# <u>9</u> Exhibit H# <u>10</u> Appendix 1# <u>11</u> Text of Proposed Order) (Jones, Michael) Modified on 6/20/2006 (mpv,). (Entered: 06/19/2006)
06/19/2006	●	***FILED IN ERROR. Document # 12, MOTION to Dismiss <i>or, in the Alternative, to Transfer this Case to Delaware</i> . PLEASE IGNORE. REPLACED BY # <u>14</u> *** (mpv,) (Entered: 06/20/2006)
07/05/2006	● <u>15</u>	MOTION for Extension of Time to File Response/Reply as to <u>14</u> MOTION to Dismiss <i>or, in the Alternative, to Transfer this Case to Delaware Unopposed</i> by Fairchild Semiconductor Corporation. (Attachments: # <u>1</u> Text of Proposed Order) (Smith, Michael) (Entered: 07/05/2006)
07/07/2006	● <u>16</u>	NOTICE of Attorney Appearance by Joseph F DePumpo on behalf of Intersil Corporation (DePumpo, Joseph) (Entered: 07/07/2006)
07/07/2006	● <u>18</u>	ORDER granting <u>15</u> Motion for Extension of Time to File Response/Reply re <u>14</u> MOTION to Dismiss <i>or, in the Alternative, to Transfer this Case to Delaware</i> . Responses due by 7/26/2006. Signed by Judge T. John Ward on 7/7/06. (kjr,) (Entered: 07/11/2006)
07/10/2006	● <u>17</u>	NOTICE of Attorney Appearance by Jeffrey Ray Bragalone on behalf of all plaintiffs (Bragalone, Jeffrey) (Entered: 07/10/2006)
07/14/2006	● <u>19</u>	NOTICE of Attorney Appearance by Michael Wayne Shore on behalf of Intersil Corporation (Shore, Michael) (Entered: 07/14/2006)
07/18/2006	● <u>21</u>	APPLICATION to Appear Pro Hac Vice by Attorney G Hopkins Guy, III for Fairchild Semiconductor Corporation. (ch,) (Entered: 07/26/2006)

07/18/2006	●	Pro Hac Vice Filing fee paid by GuyIII; Fee: \$25, receipt number: 2-1-1712 (ch,) (Entered: 07/26/2006)
07/18/2006	● <u>22</u>	APPLICATION to Appear Pro Hac Vice by Attorney Bas de Blank for Fairchild Semiconductor Corporation. (ch,) (Entered: 07/26/2006)
07/18/2006	●	Pro Hac Vice Filing fee paid by Blank; Fee: \$25, receipt number: 2-1-1711 (ch,) (Entered: 07/26/2006)
07/18/2006	● <u>23</u>	APPLICATION to Appear Pro Hac Vice by Attorney Gabriel M Ramsey for Fairchild Semiconductor Corporation and Intersil Corporation. (ch,) (Entered: 07/26/2006)
07/18/2006	●	Pro Hac Vice Filing fee paid by Ramsey; Fee: \$25, receipt number: 2-1-1710 (ch,) (Entered: 07/26/2006)
07/26/2006	● <u>20</u>	RESPONSE in Opposition re <u>14</u> MOTION to Dismiss <i>or, in the Alternative, to Transfer this Case to Delaware</i> filed by Fairchild Semiconductor Corporation, Intersil Corporation. (Attachments: # <u>1</u> Exhibit 1# <u>2</u> Exhibit 2# <u>3</u> Exhibit 3# <u>4</u> Exhibit 4# <u>5</u> Exhibit 5# <u>6</u> Exhibit 6# <u>7</u> Exhibit 7# <u>8</u> Exhibit 8# <u>9</u> Exhibit 9# <u>10</u> Exhibit 10# <u>11</u> Declaration of Ramsey# <u>12</u> Text of Proposed Order)(Smith, Michael) (Entered: 07/26/2006)
08/02/2006	● <u>24</u>	REPLY to Response to Motion re <u>14</u> MOTION to Dismiss <i>or, in the Alternative, to Transfer this Case to Delaware</i> filed by Power Integrations, Inc.. (Attachments: # <u>1</u> Declaration of Michael E. Jones# <u>2</u> Exhibit 1)(Jones, Michael) (Entered: 08/02/2006)
08/03/2006	● <u>25</u>	APPLICATION to Appear Pro Hac Vice by Attorney Michael R Headley for Power Integrations, Inc.. (ch,) (Entered: 08/10/2006)
08/03/2006	●	Pro Hac Vice Filing fee paid by Headley; Fee: \$25, receipt number: 6-1-6200 (ch,) (Entered: 08/10/2006)
08/03/2006	● <u>26</u>	APPLICATION to Appear Pro Hac Vice by Attorney Frank E Scherkenbach for Power Integrations, Inc.. (ch,) (Entered: 08/10/2006)
08/03/2006	●	Pro Hac Vice Filing fee paid by Scherkenbach; Fee: \$25, receipt number: 6-1-6200 (ch,) (Entered: 08/10/2006)
10/04/2006	● <u>27</u>	NOTICE of Attorney Appearance by Allen Franklin Gardner on behalf of Power Integrations, Inc. (Gardner, Allen)

		(Entered: 10/04/2006)
01/26/2007	28	NOTICE of Hearing: Scheduling Conference set for 3/6/2007 at 1:30 PM in Ctrm 106 (Marshall) before Judge T. John Ward. (shd,) (Entered: 01/26/2007)
01/29/2007	29	Notice of Scheduling Conference, Proposed Deadlines for Docket Control Order and Discovery Order Scheduling Conference set for 3/6/2007 1:30 PM in (Marshall) before Judge T. John Ward.. Signed by Judge T. John Ward on 1/29/07. (ch,) (Entered: 01/29/2007)
01/29/2007	30	APPLICATION to Appear Pro Hac Vice by Attorney Howard G Pollack for Power Integrations, Inc.. (ch,) (Entered: 01/29/2007)
01/29/2007		Pro Hac Vice Filing fee paid by Pollack; Fee: \$25, receipt number: 6-1-8535 (ch,) (Entered: 01/29/2007)
01/29/2007	31	APPLICATION to Appear Pro Hac Vice by Attorney Howard G Pollack for Power Integrations, Inc. (ehs,) (Entered: 01/30/2007)
01/31/2007	32	NOTICE of Attorney Appearance by James Matthew Rowan on behalf of Power Integrations, Inc. (Rowan, James) (Entered: 01/31/2007)
03/02/2007	33	APPLICATION to Appear Pro Hac Vice by Attorney Vickie L Feeman for Fairchild Semiconductor Corporation. (FEE PAID) 2-1-2318 (ehs,) (Entered: 03/02/2007)
03/05/2007	34	***FILED IN ERROR; PLEASE IGNORE*** NOTICE by Intersil Corporation <i>Vacation</i> (Shore, Michael) Modified on 3/6/2007 (mpv,). (Entered: 03/05/2007)
03/05/2007		***FILED IN ERROR. Document # 34, NOTICE of Vacation, these are not filed on the docket with the court, these letters are mailed directly to the Judge. PLEASE IGNORE.*** (mpv,) (Entered: 03/06/2007)
03/06/2007	35	MEMORANDUM OPINION and ORDER - granting in part and denying in part deft's motion to dismiss or, in the alternative, to transfer this case to Delaware #14 The court transfers this case to the District of Delaware. Signed by Judge

		T. John Ward on 3/6/07. (ehs,) (Entered: 03/06/2007)
03/29/2007	●	Interdistrict transfer to the District of Delaware. Certified copy of Transfer Order, Complaint and Docket Sheet sent to Dist of Delaware (ehs,) (Entered: 03/29/2007)

IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS

FILED-CLERK
U.S. DISTRICT COURT

06 APR 11 AM 10:13

TX EASTERN-MARSHALL

FAIRCHILD SEMICONDUCTOR
CORPORATION, a Delaware corporation,
and INTERSIL CORPORATION, a Delaware
corporation

Plaintiff,

v.

POWER INTEGRATIONS, INC., a Delaware
corporation,

Defendants.

JURY

2-06CV-151TJW

PLAINTIFFS' ORIGINAL COMPLAINT

Plaintiffs FAIRCHILD SEMICONDUCTOR CORPORATION (hereinafter, "Fairchild"),
and INTERSIL CORPORATION, (hereinafter, "Intersil") (collectively, "Plaintiffs") by and
through their undersigned counsel, hereby alleges as follows:

THE PARTIES

1. Fairchild Semiconductor Corporation is a Delaware corporation with its principal
place of business in South Portland, Maine.

2. Intersil Corporation is a Delaware corporation with its principal place of business
in Milpitas, California.

3. Power Integrations, Inc. is a Delaware is a Delaware corporation with its principal
place of business in San Jose, California.

JURISDICTION AND VENUE

4. This is an action arising under the patent laws of the United States, Title 35 of the
United States Code. This court has jurisdiction over the subject matter of this action pursuant to
28 U.S.C. §§ 1331 and 1338(a).

5. Upon information and belief, this Court has personal jurisdiction over the
defendant because Power Integrations sells the accused devices within this district.

6. Upon information and belief, venue is proper in the Court pursuant to 28 U.S.C. § 1391(b) and (c) and § 1400 as the defendant is subject to personal jurisdiction in this district.

FIRST CAUSE OF ACTION

INFRINGEMENT OF U.S. PATENT NO. 5,264,719

7. The allegations of paragraphs 1-6 are incorporated as though fully set forth herein.

8. U.S. Patent No. 5,264,719 (the “’719 Patent”), entitled *High Voltage Lateral Semiconductor Device*, duly and lawfully issued on November 23, 1993 and assigned to Intersil and exclusively licensed to Fairchild. A true and correct copy of the ‘719 Patent is attached hereto as Exhibit A.

9. Upon information and belief, Power Integrations has been and is now infringing the ‘719 Patent, both literally and under the doctrine of equivalents, by making, using, selling, offering for sale, and importing devices and products in the United States covered by one or more claims of the ‘719 Patent.

10. Upon information and belief, Power Integrations has been and is now inducing infringement and contributing to the infringement of the ‘719 Patent, both literally and under the doctrine of equivalents, by inducing or contributing to the making, using, selling, offering for sale, and importing by others devices and products in the United States covered by one or more claims of the ‘719 Patent.

11. Power Integrations’ infringement has caused irreparable injury to Fairchild and Intersil and will continue to cause irreparable injury until Power Integrations is enjoined from further infringement by the Court.

PRAYER FOR RELIEF

WHEREFORE, FAIRCHILD and INTERSIL pray for the following relief:

A. Judgment by the Court that Power Integrations directly infringes the ‘719 Patent;

B. Judgment by the Court that Power Integrations induces or contributes to others’ infringement of the ‘719 Patent;

C. Preliminary and permanent injunctive relief pursuant to 35 U.S.C. § 283 enjoining Power Integrations, its officers, agents, servants, employees, successors, assigns and all other persons or entities acting in concert or participation with Power Integrations or on Power Integrations' behalf from further infringement of the '719 Patent;

D. Money damages sustained as a result of Power Integrations' infringement of the '719 Patent;

E. Costs and reasonable attorneys' fees incurred in connection with this action pursuant to 35 U.S.C. § 285; and,

F. Such other relief as the Court finds just and proper.

DEMAND FOR JURY TRIAL

Pursuant to Rule 38(b) of the Federal Rules of Civil Procedure, Fairchild Semiconductor Corporation and Intersil Corporation hereby demand a trial by jury on this action.

Respectfully submitted by,


ORRICK, HERRINGTON & SUTCLIFFE LLP

G. Hopkins Guy, III (Calif. SBN 124811)

Vickie Feeman (Calif. SBN 177487)

Bas de Blank (Calif. SBN 191487)

Brian Vander Zanden (Calif. SBN 233134)

1000 Marsh Road

Menlo Park, CA 94025

(650) 614-7400

Carl R. Roth, Texas Bar No. 901984225

cr@rothfirm.com

Michael C. Smith, Texas Bar No. 900641877

ms@rothfirm.com

THE ROTH LAW FIRM, P.C.

115 North Wellington, Suite 200

P.O. Box 876

Marshall, Texas 75671

Tel: (903) 935-1665

Fax: (903) 935-1797

Attorneys for Plaintiffs,
FAIRCHILD SEMICONDUCTOR
CORPORATION and INTERSIL
CORPORATION

SHORE CHAN, L.L.P.
Michael Shore, Texas Bar No. 18294915
shore@shorechan.com
Jeffrey R. Bragalone, Texas Bar No. 02855775
jbragalone@shorechan.com
325 North St. Paul, Suite 4450
Dallas, Texas 75201
Tel: (214) 593-9110
Fax: (214) 593-9111

ATTORNEYS FOR INTERSIL
CORPORATION

United States Patent [19]

Beasom

[11] Patent Number: 5,264,719

[45] Date of Patent: Nov. 23, 1993

[54] HIGH VOLTAGE LATERAL SEMICONDUCTOR DEVICE

[75] Inventor: James D. Beasom, Melbourne Village, Fla

[73] Assignee: Harris Corporation, Melbourne, Fla

[21] Appl. No.: 705,509

[22] Filed: May 24, 1991

Related U.S. Application Data

[63] Continuation of Ser. No. 242,405, Sep. 8, 1988, abandoned, which is a continuation-in-part of Ser. No. 831,384, Jan. 7, 1986, Pat. No. 4,823,173

[51] Int. Cl.⁵ H01L 29/80

[52] U.S. Cl. 257/335; 257/336; 257/339

[58] Field of Search 357/38, 55, 23 8, 46

[56] References Cited

U.S. PATENT DOCUMENTS

4,626,879 12/1986 Colak 357/23 8

4,628,341 12/1986 Thomas 357/23 8
4,811,075 3/1989 Eklund et al 357/46
4,994,889 2/1991 Takeuchi et al 357/55
4,994,904 2/1991 Nakagawa et al 357/38

Primary Examiner—Rolf Hille

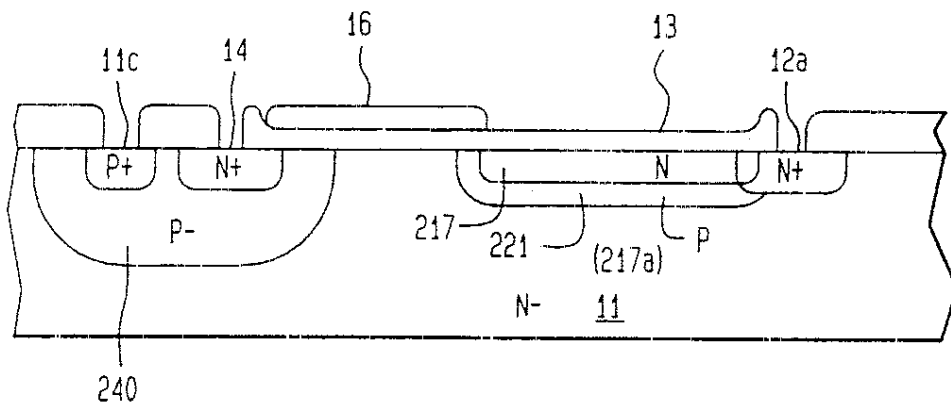
Assistant Examiner—Roy Potter

Attorney, Agent, or Firm—Evenson, Wands, Edwards, Lenahan & McKeown

[57] ABSTRACT

The present invention provides an improved lateral drift region for both bipolar and MOS devices where improved breakdown voltage and low ON resistance are desired. A top gate of the same conductivity type as the device region with which it is associated is provided along the surface of the substrate and overlying the lateral drift region. In an MOS device, the extremity of the lateral drift region curves up to the substrate surface beyond the extremity of the top gate to thereby provide contact between the JFET channel and the MOS channel.

42 Claims, 7 Drawing Sheets



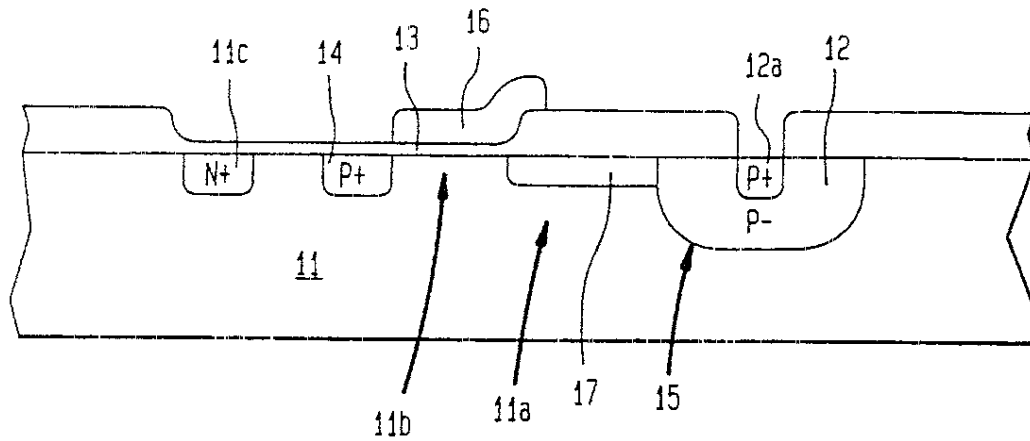


FIG. 1

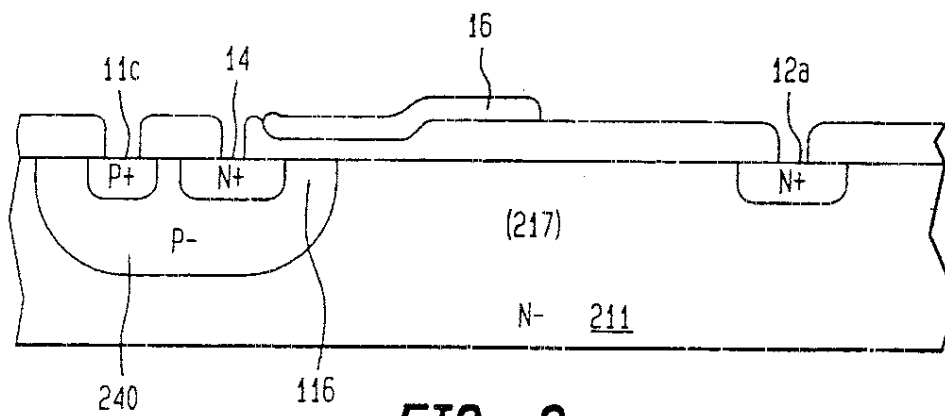


FIG. 2
(PRIOR ART)

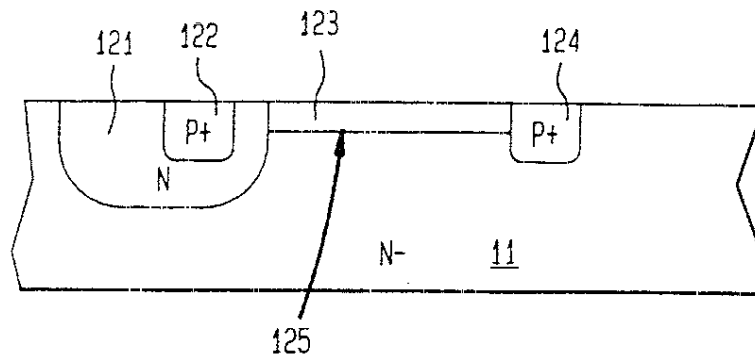


FIG. 3

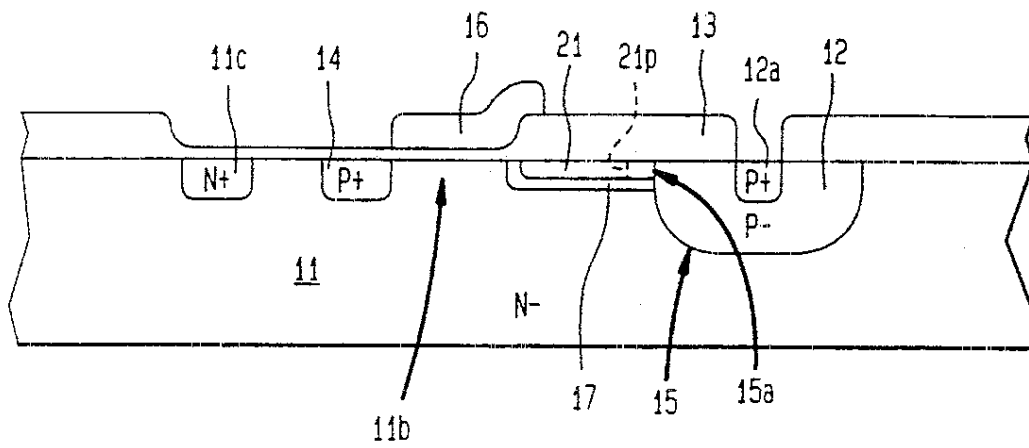


FIG. 4

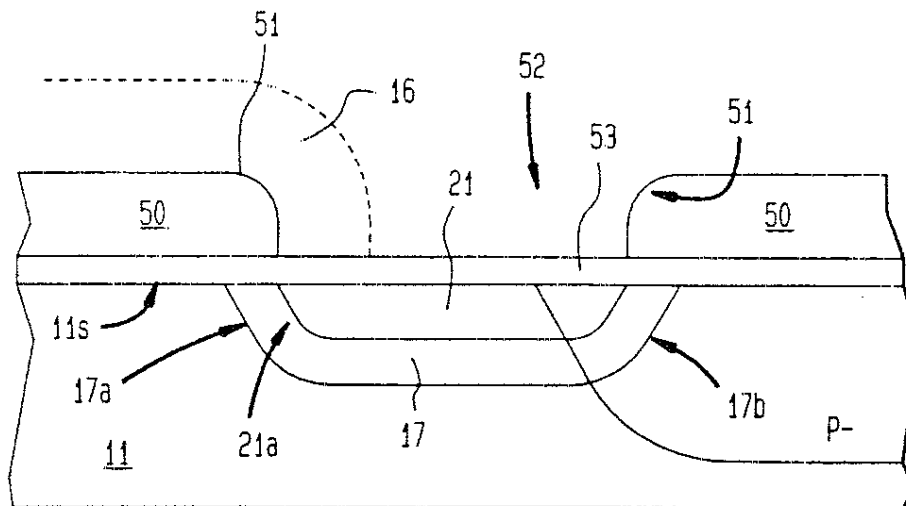


FIG. 5

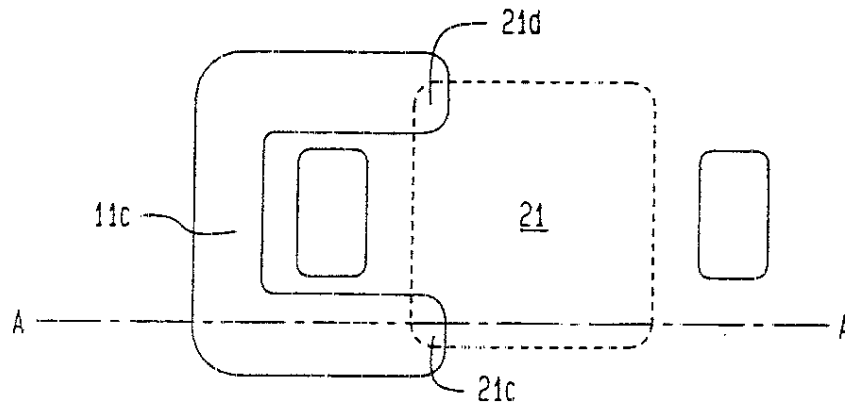


FIG. 6a

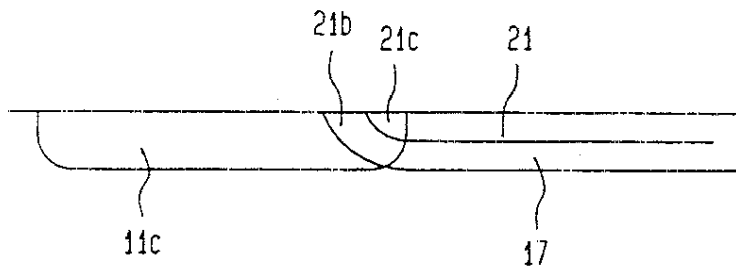


FIG. 6b

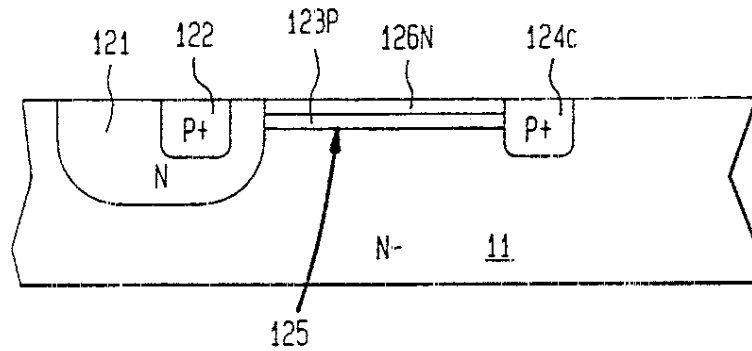


FIG. 7

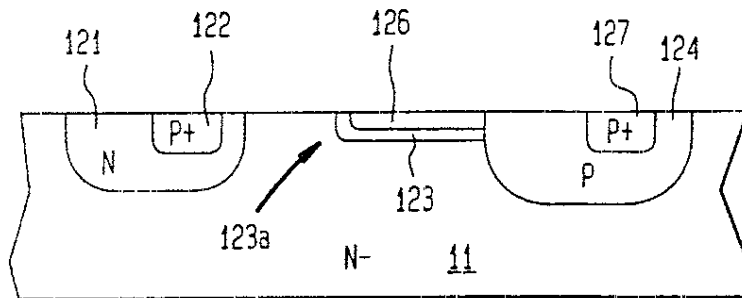


FIG. 8

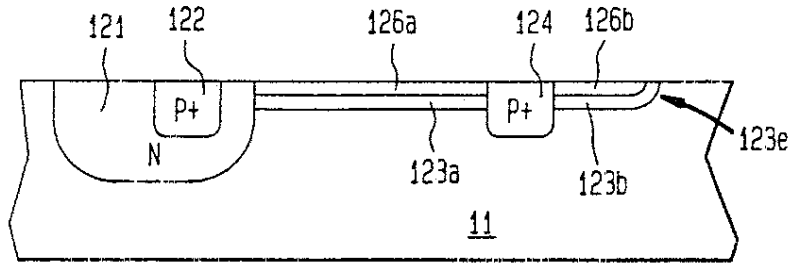


FIG. 9

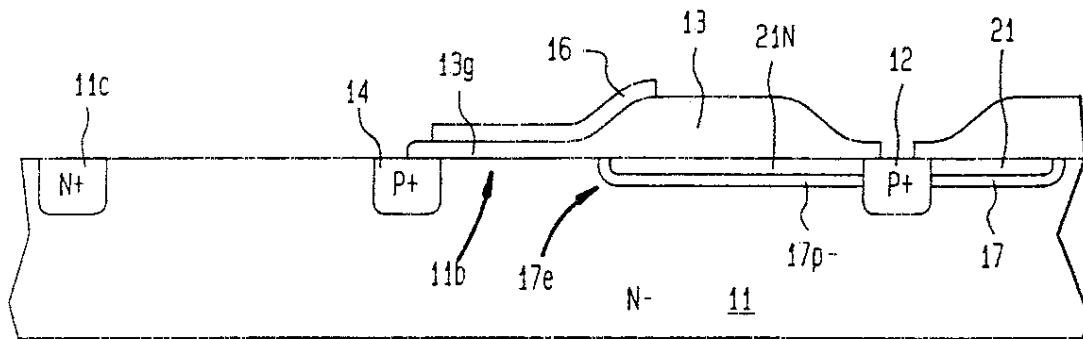
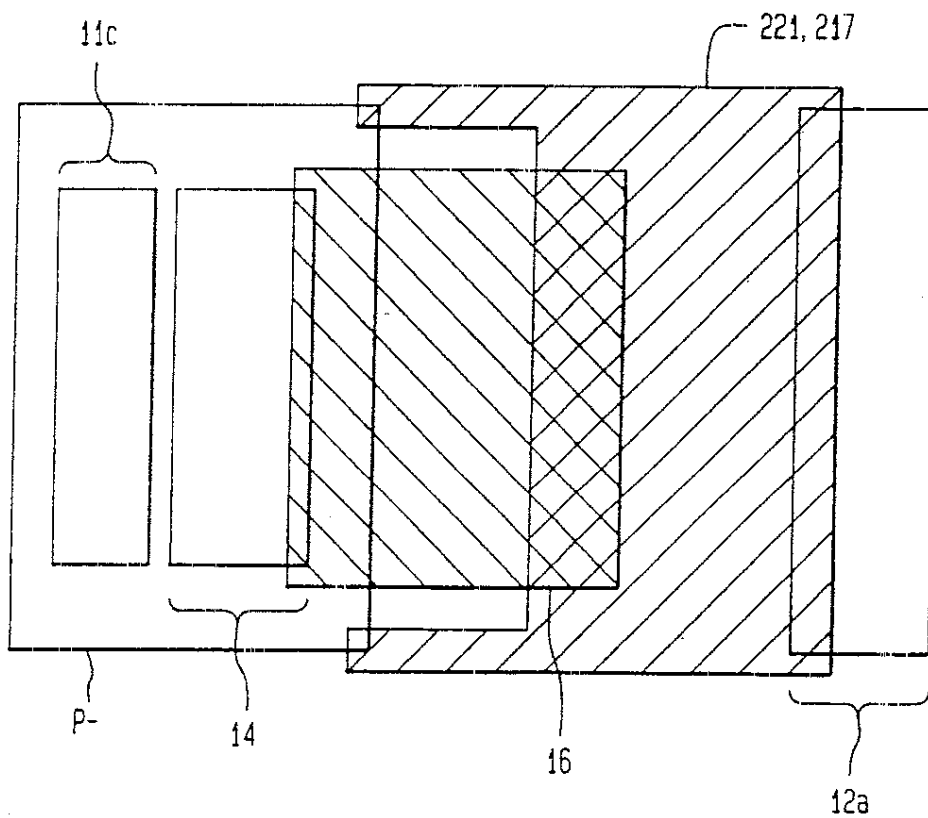
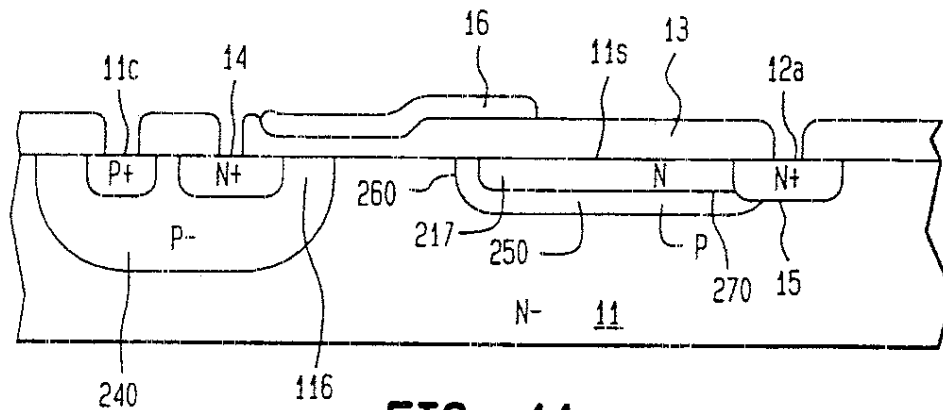


FIG. 10



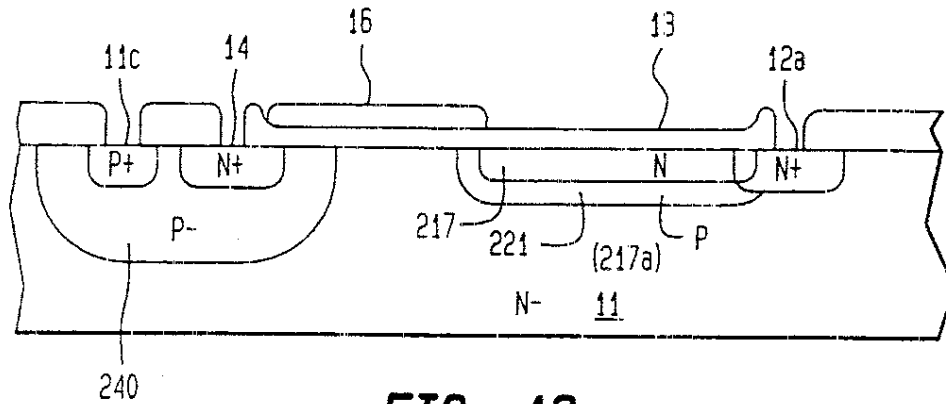


FIG. 13

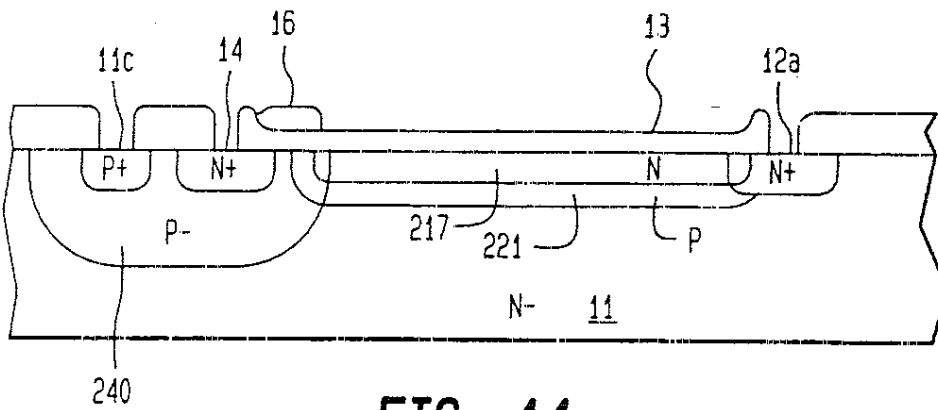


FIG. 14

HIGH VOLTAGE LATERAL SEMICONDUCTOR DEVICE

This is a continuation of application, Ser. No. 242,405, filed Sep. 8, 1988, now abandoned which, in turn, is a continuation-in-part of application, Ser. No. 831,384, filed Jan. 7, 1986, now U.S. Pat. No. 4,823,173, issued Apr. 18, 1989.

FIELD OF THE INVENTION

The present invention relates to lateral semiconductor devices and an improved method of making lateral semiconductor devices. More specifically, the invention relates to high voltage lateral devices with reduced ON resistance and a method of making such devices.

Previous high voltage lateral devices include both MOS devices and bipolar transistors. For example, FIG. 1 illustrates a known structure which can be used as a high voltage lateral MOS device. This device is known as a lateral drift region MOS device and is dependent upon the drain-to-body junction 15 as the basic high voltage junction of the device. The drift region 17 is a P region along the top surface of the N⁻ substrate 11 and is located so as to lie adjacent the P⁻ drain region 12. The drift region 17 is used to connect the high voltage drain 12 to the gate 16 and source 14. The two contacts, drain contact 12_a and body contact 11_c, are shown for completeness. In the operation of this circuit, the gate 16 and source 14 never assume large voltages relative to the body 11. The drift region 17 serves as a JFET channel with the portion 11_a of body region 11 underlying the channel acting as a JFET gate. The JFET channel 17 is designed to totally deplete when the drain 12 is reverse biased to a voltage less than the voltage necessary to reach critical field in the channel-to-body depletion layer. This design preserves the effective high breakdown voltage of drain body junction 15. Also the source 14 and gate 16 (over the gate oxide 13) are safely shielded from the high drain body voltage by the pinched off JFET channel 17.

The resistance of the lateral drift region JFET channel 17 is in series with the resistance of the MOS channel 11_b, consequently the total channel resistance of the device is the sum of these two individual resistances. The JFET channel, which must be quite long to sustain high drain body voltages, is often the larger of the two resistance terms. Thus it is desirable to find ways to reduce the resistance of the drift region so that devices of a given size can be made with smaller channel resistance.

FIG. 2 illustrates a known structure which can be used as a high voltage lateral DMOS (LDMOS) device. In this device, an N⁺ drain contact 12A is formed in the N⁻ substrate 211 and an N⁺ source 14 and P⁺ body contact 11_c are formed in a P⁻ body region 240. The drift region 217 is an N⁻ region along the top surface of the N⁻ substrate 211 which connects the drain 12 to the gate 16 and source 14. In this high voltage device, the N⁻ drift region 217 must be lightly doped to obtain high body 240 to drain breakdown.

The ON resistance of the LDMOS is approximately the sum of the channel resistance and the bulk resistance in the N⁻ drift region 217. The lateral distance from the N⁺ drain 12 to the adjacent edge of the MOS channel 11_b underlying the gate on the P⁻ body 240 must be large to allow space for the reverse bias depletion layer which spreads from the body-to-drain junction into the

lightly doped drain. This distance, along with the high N⁻ resistivity contribute to the high drift region resistance, which is often much greater than the channel resistance. Thus, it is desirable to reduce the drift region resistance of the LDMOS device.

FIG. 3 shows a known structure which can be used as a lateral bipolar transistor. Another illustration of such a device is contained in FIG. 7 of U.S. Pat. No. 4,283,236 issued Aug. 11, 1981. Referring to FIG. 3, an N⁻ substrate 11, has an N type emitter shield 121 formed therein and P⁺ emitter 122 and collector 124 formed as shown. Additionally, a P⁻ drift region 123 is provided along the surface of the substrate between the collector 124 and the emitter shield 121. In the operation of this device, the total collector resistance is equal to the sum of the resistance across the drift region 125 plus the resistance of the P⁺ collector between the drift region and the collector contact. In order to provide devices of equal size having a lower collector resistance, it is desirable to find ways to reduce the resistance of the drift region.

In the operation of this device, the drift region extends the collector to the edge of the emitter shield, 121, so that the base width is just that small distance between the adjacent edges of the emitter, 121, and the drift region, therefore, providing improved frequency response.

At high base-collector voltages, the drift region, 123, depletes by JFET action with the N-base, 11, and N shield, 121, which is part of the base, acting as gate before critical field is reached just as for the MOS of FIG. 1. This preserves the high breakdown of the structure.

SUMMARY OF THE INVENTION

The present invention provides a structure having a reduced channel resistance and a process capable of efficiently obtaining the structure of the invention. The reduction in channel resistance is accomplished by providing a top gate which is located between the lateral drift region of the prior art and the surface of the channel region and which may be in contact with the high voltage device region. This top gate allows the total channel doping to be increased because the top gate to channel depletion layer holds some additional channel charge when reverse biased in addition to that held by the bottom gate to channel depletion layer of the prior art structure. The ionized channel impurity atoms associated with this additional channel charge causes the reduction in channel resistance.

With respect to providing an improved LDMOS structure having a lower drift region resistance, a second drift region which is separated from the original drift region by a region of opposing conductivity is formed. The second drift region provides a conductive path which is in parallel with the original drift region thereby achieving the desired reduction in resistance. Because of the formation of the second drift region, the first enclosed drift region can now have a much higher doping than the second drift region which it replaces, while achieving the same breakdown voltage.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cross section of a known MOS device having typical ON resistance.

FIG. 2 is a cross section of a known LDMOS device having typical ON resistance.

FIG. 3 is a cross section of a known bipolar transistor having typical collector resistance.

FIG. 4 is a cross section of an MOS device including the improved drift region and top gate of the invention.

FIG. 5 illustrates optimized process steps for obtaining the desired shape of the top gate and drift region of the invention

FIGS. 6a and 6b are, respectively, a top view and a cutaway perspective view of the body contact extending through the top gate and drift region of the invention.

FIG. 7 is a cross section of a bipolar device made in accordance with one aspect of the invention.

FIG. 8 is a cross section of a bipolar device made in accordance with another aspect of the invention

FIG. 9 is a cross section of a bipolar device made in accordance with a preferred aspect of the invention.

FIG. 10 is a cross section of an MOS device, including the lateral drift region and top gate of the invention, in a preferred embodiment.

FIG. 11 is a cross section of a LDMOS device made in accordance with a preferred embodiment of the invention

FIG. 12 is a top view of the LDMOS device of FIG. 11.

FIG. 13 is a cross section of a LDMOS device made in accordance with another preferred embodiment of the invention.

FIG. 14 is a cross section of a LDMOS device made in accordance with still another preferred embodiment of the invention

DETAILED DESCRIPTION OF THE INVENTION

The present invention is described herein with reference to the drawings for both MOS and bipolar applications. FIG. 4 shows an MOS device where P⁺ drain contact 12_a is formed in P⁻ type drain 12, P⁺ source 14 is formed in the N⁻ body 11 and N⁺ body contact 11_c is provided in the N⁺ body 11. The MOS channel region 11_b is in the N⁻ body 11 below the MOS gate 16. The N type top gate 21 is provided along the surface 11_i of the body 11 above the P type drift region 17 which acts as a JFET channel. The lateral edge or peripheral edge of both the top gate 21 and drift region 17 extend to the drain-to-body junction 15 and preferably terminate at the junction 15. It is noted that situations may exist where the doping level in the top gate may be sufficiently high so as to render it desirable to provide a shorter top gate having a lateral extension which stops short of contacting the junction 15. In this case care should be taken to insure that any nondepleted portion of the top gate does not result in a breakdown of the top gate-to-drift region junction 17A. Proper doping of the top gate 21 will generally be a sufficient preventative step. Dashed line 21_p designates the peripheral edge of top gate 21 in an embodiment where the top gate does not extend all the way to the junction 15.

The structure of FIG. 4 provides reduced ON resistance in the JFET channel 17 relative to the prior art lateral drift MOS device as shown in FIG. 1. The reduction in ON resistance is accomplished by providing a structure which can accommodate increased drift region doping without suffering from reduced body-to-drain breakdown. This is possible because of the provision of the top gate 21. The top gate-to-channel depletion layer which holds some channel charge when reverse biased, is in addition to the channel charge held by

the bottom gate to channel depletion layer of the prior art. This additional channel charge, in the form of ionized channel impurity atoms, causes the reduction in channel resistance. It is possible to provide more than twice the doping level previously acceptable due to the additional ability to hold channel charge. Thus, for a drift region 17 having a doping of 1×10^{12} boron atoms per square centimeter in a bottom gate arrangement, the present invention will permit 2×10^{12} boron atoms per square centimeter. Thus, the ON resistance will be only half the ON resistance of the prior arrangement.

In order to optimize performance of the structure of the invention, the top gate 21 must be designed differently than an ordinary JFET gate. Top gate 21 should become totally depleted at a body-to-drain voltage of less than the breakdown voltage of the top gate-to-drain junction 15. Since top gate 21 is connected to body 11 (as shown in FIGS. 6A, 6B to be described below), the voltage at the top gate-to-drain junction 15_a will equal the voltage of the body-to-drain junction 15 voltage and the top gate-to-drain breakdown voltage should be greater than the voltage at which top gate 21 becomes totally depleted. Additionally, the top gate 21 must totally deplete before the body 11 to channel 17 depletion layer reaches the top gate 21 to channel 17 depletion layer to thereby assure that a large top gate 21 to drain 12 voltage is not developed by punch-through action from the body 11. An ordinary JFET gate never totally depletes regardless of operating conditions.

In addition to the above described characteristics of the device of the invention, it is also necessary to insure that the channel of the JFET drift region 17 contacts the inversion layer MOS surface channel. This can be accomplished as shown in FIG. 5 where an implant mask 50 having a tapered edge 51 is provided over the body 11. An implant aperture 52 is provided in mask 50 at the location where the P drift region 17 and N top gate 21 are to be formed. The aperture 52 is shown as exposing the protective oxide 53. Ion implantation is not substantially affected by the oxide 53 due to the oxide thickness of only about 0.1-0.2 micrometers, yet the oxide provides surface passivation for the underlying body 11.

The drift region 17 is ion implanted and, because of the graduated thickness of the implant mask 50 (along the edge 51), the depth of the implanted drift region 17 is graduated or tapered. In the illustration, a fairly good rounding of the drift region 17 occurs at the peripheral edges or extremities 17_a, 17_b of the region 17. The curved extremity 17_a is of interest because at this location the channel of the JFET drift region 17 contacts the surface 11_s of body 11 beyond the end 21_a of top gate 21 and is desirably beneath the gate 16 of the MOS device. The top gate 21 may be ion-implanted using the implant mask 50 but at an energy level which results in a shallower implantation. This tapered profile, particularly if curved, provides improved performance.

In a variation of this method, a diffusion process can be used to bring the JFET channel into contact with the surface of body 11, and hence insure that the JFET channel 17 will contact the inversion layer MOS surface channel (lateral drift region 17 and top gate 21 are diffused after initial introduction by ion implant). The doping levels and diffusion times are chosen such that the extremity 17_a of JFET channel 17 diffuses beyond the end 21_a of the top gate 21 and so that the end 17_a reaches the surface 11_s of body 11. In practice, this approach can be facilitated by choosing a top gate dop-

ant which has a lower diffusion coefficient than that of the drift region dopant

The formation of the drift region 17 and top gate 21 may be conveniently carried out by forming a mask over the gate oxide which is present in a lateral MOS application. The MOS gate may be utilized as one delineating edge of the implant for the drift region and top gate and a thick oxide portion surrounding a thinner oxide portion may form the remainder of the implant mask. The thinner oxide portion shall be located such that it extends from beneath the MOS gate to the drain and preferably overlaps the drain. The implant mask 50 illustrated in FIG. 5 is shown as having thin oxide portion 53 being surrounded by the implant mask 50. If the MOS gate 16 shown in dashed lines were used as a portion of the mask 50, the edge of the drift region and top gate would be self-aligned with the MOS gate as shown in dashed lines. Then, when diffused, the drift region will extend laterally to a point beneath the MOS gate, while the top gate 21 may be formed such that there is little or no lateral overlap with the MOS gate. The extent of lateral diffusion of the top gate is dependent upon the dopant material and processing temperatures following top gate implant. It is noted that there is a separation between the drift region and the source. This separation zone is the location where the MOS channel is located.

The top gate 21 will perform as previously described if it is tied to the body 11. Thus, the top gate 21 and the body which operates as the bottom gate of the JFET channel will be at equal potential. According to the invention, this may be accomplished in a particularly effective manner if the drift region 17 is widened to overlap with the body contact region 11_c. This is shown in FIG. 6a which shows the overlapping of the top gate 21 and the body contact 11_c at the overlap regions 21_c, 21_d. In order for this arrangement to be effective, it is necessary that the body contact 11_c have a higher dopant concentration than the JFET channel (or drift region) 17, as shown in FIG. 6b to insure that the body contact 11_c forms a continuous region horizontally and/or vertically through the JFET channel and to the body region 11 from the top gate, 21.

FIG. 6b shows a cross section of the structure of FIG. 6a taken along dashed line A—A. The body 11 is provided with body contact 11_c which is located such that the top gate 21 and drift region 17 can be conveniently extended to overlap the body contact 11_c. The depth of body contact 11_c may be made greater than the depth of region 17 such that a portion of the body contact 11_c extends below region 17 and provides contact with the body 11. This arrangement provides a contact portion 21_c where the top gate 21 is in contact with body contact 11_c. Thus, as long as the body contact doping concentration in region 21_b is sufficiently high to overcome the opposite doping in region 17, then a good connection of uniform conductivity type will be provided between the top gate 21 and the body 11, via contact region 11_c. It is also noted that the body contact 11_c extends laterally beyond the end of both of the top gate 21 and the drift region 17. The lateral extension of the contact 11_c will also provide a structure which results in a good connection of uniform conductivity type from the top gate 21 to the body 11, again, provided that the doping of body contact 11_c converts region 21_b.

Another area where the present invention finds application is in lateral bipolar transistors which employ a lateral drift region. The known structure of FIG. 3 may

be improved by providing an N type top gate 126 as shown in FIG. 7. In this arrangement the N type gate 126 extends from the collector 124 to the emitter shield 121 along the surface of body 11. The operation of this device is enhanced by the same phenomenon as the lateral drift region of the previously described MOS device. As the base 11 becomes positive relative to the collector 124, the top gate-to-drift region depletion layer facilitates pinch-off of the drift region 123. However, as the base 11 becomes more negative, the top gate 126 contributes additional surface exposure to the drift region 123 and further enhances carrier transportation.

FIG. 8 shows an improvement over the arrangement shown in FIG. 7. In FIG. 8 the drift region 123 does not extend all the way over to the emitter shield 121. The curved end 123_a of the drift region 123 contacts the top surface of body 11. It is noted that in this arrangement, the emitter shield 121 may be omitted.

An additional improvement shown in FIG. 8 is the use of a deep diffusion to form the collector 124 resulting in a significantly increased breakdown voltage. The deep diffusion step may be the same step used for forming the emitter, in which case the collector 124 shown in FIG. 7 would be deeper, or a separate collector implant and diffusion step may be employed and the collector contact 127 may then be formed simultaneously with the formation of the emitter 122. This improvement in junction breakdown voltage is equally obtainable, for example, at the body to drain junction in the MOS devices described previously.

A further extension of the invention which may be used to increase base-to-collector breakdown voltage for a PNP device is shown in FIG. 9. In addition to the provision of the N type top gate 126_a over the P—drift region 123_a, the top gate 126_a and drift region 123_a are enlarged to surround the collector 124 and a curved edge 123_c is provided at the periphery of the enlarged portion 123_b of the drift region 123_a. This enlarged portion is designated by reference numerals 123_b for the drift region and 126_b for the top gate. The collector 124 to base 11 breakdown voltage is increased relative to alternative arrangements because of mitigation of the breakdown reduction due to the junction curvature. The top gate 126_a extends to the emitter shield 121 as does the drift region 123_a. The P+ emitter 122 is formed in the N+ type emitter shield 121.

FIG. 10 illustrates an extension of the invention with respect to a P channel MOS device similar to the improvement described with respect to the bipolar device shown in FIG. 9. For the MOS device, the drain 12 is surrounded by the P—drift region 17 and N type top gate 21. Around the entire periphery of the drift region 17 there is a curved portion 17_c which rounds up to the surface of the N—substrate 11 to insure that the JFET channel in the drift region 17 contacts the MOS channel 11_b under the MOS gate 16. The drift region 17 extends outward from the entire perimeter of the drain 12. This arrangement mitigates the breakdown reduction due to junction curvature. The P+ source 14 and N+ body contact 11_c are shown as is the dielectric 13 which serves as the gate oxide 13_g beneath the MOS gate 16.

In both the arrangements shown in FIG. 9 and FIG. 10, the planar diode breakdown improvement created by the drift region acting as a surface layer of the same conductivity type as the collector in FIG. 9 and drain in FIG. 10 and extending out from the perimeter of the collector and drain can be implemented by a single series of process steps. According to the invention, a

common set of process steps produces both a suitable breakdown improvement layer and an improved drift region. The breakdown improvement layer is a two layer component.

A further extension of the invention is illustrated in FIG 11 which shows an LDMOS device where N⁺ drain contact 12_a is formed in an N⁻ type substrate and an N⁺ source 14 and P⁺ body contact 11_c are formed in a P⁻ type body region 240. The DMOS channel region 11_b is in the P⁻ body 240 below the DMOS gate 16. The N type first drift region 217 is provided along the surface 11_i of the substrate 11 above a P⁻ type separation region 250. A second drift region 217_a exists in the substrate 11 underneath the P⁻ type separation region. The lateral edge of both the first drift region 217 and the separation region 250 extend from the gate 16 to the N⁺ drain contact 12_a.

The structure in FIG 11 provides reduced ON resistance by way of the second (surface) drift region 217_a relative to the (deeper) prior art lateral first drift region 217_a device, refer to above in FIG. 2. To illustrate this, consider an example in which the N⁻ region 11 has a doping of 1×10^{14} ions cm⁻³. The top gate layer 217 has an integrated doping of about 1×10^{12} ions cm⁻² and is preferably not more than two microns thick while maintaining full breakdown. The thickness of the N and P layers 217, 250 together is preferably less than ten microns and can be less than one micron. The same integrated doping in the N⁻ body 11 requires a thickness of 100 microns. Thus, the N and P layers 217, 250 respectively consume only a small fraction of the N⁻ thickness required to provide doping equal to that portion of the N layer of the prior art device.

The lateral spacing between the drain contact 12_a and the channel 11_b in the device described above would be approximately 30 microns. In such a device, even if a full 100 micron thick N⁻ body 11 were provided, it would have a higher resistance than the N⁻ first drift region 217 provided according to the invention. This is because the average path length of current flowing from the drain contact 12A down through the thick N⁻ body 11 and back up to the surface edge of the channel at the drain-to-body junction would be greater than the direct path through the N⁻ first drift region.

Maximum breakdown is achieved in the invention by providing doping densities of the N and P layers 217, 250 such that they become totally depleted before breakdown is reached at any point along the junctions which they form with adjoining regions and before breakdown is reached at the junction between them. To insure that this occurs, the N region 217 should have an integrated doping not exceeding approximately 1×10^{12} ions cm⁻² and the P region 250 should have a higher integrated doping not exceeding about 1.5 to 2×10^{12} ions cm⁻².

To insure proper depletion of the P and N regions 250, 217, they must have the proper voltages applied. The N layer bias is achieved by connecting the N first drift region 217 to the higher concentration N⁺ drain contact 12_a by overlapping the N first drift region 217 and drain contact 12_a. The P region 250 bias is achieved by overlapping the P region 250 with the P⁻ body 240 at least at one end of the channel, thereby applying the body voltage to the P layer 250. This is illustrated in FIG. 12.

With this structure and choice of doping levels, the desired results are achieved. When a reverse bias voltage is applied to the drain-to-body junction 15, the same

reverse bias appears on both the PN⁻ junction 260 and the PN junction 270. Depletion layers spread up into the N first drift region 217 and down into the N⁻ body 11 from the P layer 250. In a preferred embodiment, the P and N first drift region dopings are chosen such that the N layer 217 becomes totally depleted at a lower voltage than that at which the P layer 250 becomes totally depleted. This insures that no residual undepleted portion of the N layer 217 is present which could reduce breakdown voltage.

As a result of the invention, the improved DMOS device provides a reduced resistance current path in the drain which does not depend on the N⁻ doping. This allows the N⁻ doping to be reduced to achieve a desired breakdown voltage with good manufacturing margin, while maintaining desirable low drift region resistance. In a multi-device process which includes LDMOS devices, the N⁻ region can be adjusted to achieve the desired characteristics of one or more of the other device types, while the N first drift region 217 sets the drift region 217 resistance of the LDMOS.

Another embodiment of the DMOS invention is illustrated in FIG 13, where the N and P regions 217, 221 are self-aligned to the gate 16 by using the gate 16 as a mask. An advantage of this structure is that N and P regions can be defined by the uncovered thin oxide area which extends from gate edge to overlap the drain contact. This embodiment requires no explicit mask step to delineate the location where the N and P regions are formed.

Still another embodiment, as illustrated in FIG 14, provides no gap between the P⁻ body 240 and the P region 221 adjacent to the channel edge. The absence of the gap prevents current from flowing in the N⁻ body 11; so the entire drift region current path is in the N first drift region 217. Elimination of the gap also allows the device structure to be made smaller. As with the other structure, the N and P regions may be self-aligned to the gate edge, as illustrated in FIG 14, or not self-aligned. They may also be covered by thick or thin oxide as a design option.

A preferred feature of the present invention provides that the body or substrate regions 11 shown in the FIGS. 3, 4, 6, 7, 8, 9, 11, 13 and 14 are designed to be dielectrically or self-isolated regions. In contrast with the typical RESERF type of devices in which the bottom isolation junction plays a central role in the action of the device, the present invention contemplates that the isolation junction does not contribute to the depletion of the drift or top gate regions which are taught to be totally depleted. Prior art RESERF devices such as that described in U.S. Pat. No. 4,300,150 to Colak always require the substrate to be part of such depletion whereby the substrate must assume the most negative voltage in the device because of its role as one side of the isolation junction. As a result of this bias on the substrate or body region, the prior art RESERF type devices are susceptible to punch through from the device region through the epitaxial layer to the substrate. As a result of the present invention not having the substrate as part of the depletion mechanism, the invention can more effectively provide high voltage protection while not increasing the resistance of the channel path. Although the figures illustrate a nonisolating structure or self-isolated structure, it is understood that the invention applies equally well to dielectrically or junction isolated substrates.

9

While the present invention has been described with respect to several preferred manners of implementing the invention, it is to be understood that the claims appended hereto are intended to cover the invention in its broadest sense and are not to be limited to the specific implementations disclosed.

What is claimed is:

1 A semiconductor device comprising:

- a semiconductor body of a first conductivity type having a first surface;
 - a first semiconductor region of a second conductivity type formed in a first portion of said first surface of said semiconductor body, and defining a first PN junction with said semiconductor body;
 - a second semiconductor region of said first conductivity type formed in a surface portion of said first semiconductor region and defining therewith a second PN junction, said second PN junction being spaced apart from said first PN junction by material of said first semiconductor region therebetween;
 - a third semiconductor region of said first conductivity type formed in a second surface portion of said semiconductor body, spaced apart from said first surface portion by a third surface portion thereof;
 - a fourth semiconductor region of said second conductivity type formed in a first surface part of said third surface portion of said semiconductor body spaced apart from said first surface portion of said semiconductor body by a second surface part of said third surface portion thereof and defining with said semiconductor body a third PN junction, said fourth semiconductor region being connected to said first semiconductor region and being contiguous with said third semiconductor region;
 - a fifth semiconductor region of said first conductivity type, and having an impurity concentration greater than that of said semiconductor body, formed in said fourth semiconductor region and defining therewith a fourth PN junction, said fifth semiconductor region being contiguous with said third semiconductor region;
 - an insulator layer formed on said first surface of said semiconductor body; and
 - a gate electrode formed on said insulator layer so as to overlie said second surface part of said third surface portion of said semiconductor body and material of said first and fourth semiconductor regions, that portion of said first semiconductor region lying beneath said gate electrode serving as a channel region of said device, said gate electrode having a gate voltage applied to induce a conductive channel through said first semiconductor region therebeneath; and wherein
- when said device is reverse-biased, a first depletion region extends from said fourth PN junction into said fourth semiconductor region and said semiconductor body, and a second depletion region extends from said fifth PN junction into said fifth semiconductor region and said fourth semiconductor region;
- said semiconductor body having a first ON resistance in a first current flow path therethrough between said second and third semiconductor regions, and said fifth semiconductor region providing a second ON resistance in a second current flow path along the surface of said semiconductor body from said second semiconductor region through said channel

10

and said fourth and fifth semiconductor regions to said third semiconductor region, so that said fifth semiconductor region serves to provide a current flow path in parallel with said first current flow path, thereby effectively reducing the total ON resistance of the overall current flow path between said second and third semiconductor regions.

2 A semiconductor device according to claim 1, wherein a peripheral edge of said gate electrode is aligned with a peripheral edge of said fifth semiconductor region.

3 A semiconductor device according to claim 1, wherein said fourth semiconductor region overlaps said first semiconductor region.

4 A semiconductor device according to claim 1, wherein the impurity concentration said fifth semiconductor region is such that said fifth semiconductor region is completely depleted by said second depletion region at a reverse bias less than that at which said first and second depletion regions come together within and punch through said fourth semiconductor region.

5 A semiconductor device comprising:

- a semiconductor body of a first conductivity type having a first surface;
 - a first semiconductor region of a second conductivity type formed in a first portion of said first surface of said semiconductor body, and defining a first PN junction with said semiconductor body;
 - a second semiconductor region of said first conductivity type formed in a surface portion of said first semiconductor region and defining therewith a second PN junction, said second PN junction being spaced apart from said first PN junction by material of said first semiconductor region therebetween;
 - a third semiconductor region of said first conductivity type formed in a second surface portion of said semiconductor body, spaced apart from said first surface portion by a third surface portion thereof;
 - a fourth semiconductor region of said second conductivity type formed in said third surface portion of said semiconductor body and defining with said semiconductor body a third PN junction, said fourth semiconductor region being connected to said first semiconductor region and being contiguous with said first and third semiconductor regions;
 - a fifth semiconductor region of said first conductivity type, and having an impurity concentration greater than that of said semiconductor body, formed in said fourth semiconductor region and defining therewith a fourth PN junction, said fifth semiconductor region being contiguous with said first and third semiconductor regions;
 - an insulator layer formed on said first surface of said semiconductor body; and
 - a gate electrode formed on said insulator layer so as to overlie material of said first and fourth semiconductor regions, that portion of said first semiconductor region lying beneath said gate electrode serving as a channel region of said device, said gate electrode having a gate voltage applied to induce a conductive channel through said first semiconductor region therebeneath; and wherein
- when said device is reverse-biased, a first depletion region extends from said fourth PN junction into said fourth semiconductor region and said semiconductor body, and a second depletion region extends from said fifth PN junction into said fifth semiconductor region.

11

ductor region and said fourth semiconductor region.

6. A semiconductor device according to claim 5, wherein the impurity concentration said fifth semiconductor region is such that said fifth semiconductor region is completely depleted by said second depletion region at a reverse bias less than that at which said first and second depletion regions come together within and punch through said fourth semiconductor region.

7. A semiconductor device comprising:

a semiconductor body of a first conductivity type having a first surface;

a first semiconductor region of a second conductivity type formed in a first portion of said first surface of said semiconductor body, and defining a first PN junction with said semiconductor body;

a second semiconductor region of said second conductivity type formed in a second surface portion of said semiconductor body, spaced apart from said first surface portion by a third surface portion thereof and defining a second PN junction with said semiconductor body;

a third semiconductor region of said second conductivity type formed in a first surface part of said third surface portion of said semiconductor body spaced apart from said first surface portion of said semiconductor body by a second surface part of said third surface portion thereof and defining with said semiconductor body a third PN junction, said third semiconductor region being contiguous with said second semiconductor region;

a fourth semiconductor region of said first conductivity type, and having an impurity concentration greater than that of said semiconductor body, formed in said third semiconductor region and defining therewith a fourth PN junction;

an insulating layer formed on said first surface of said semiconductor body; and

a gate electrode formed on said insulator layer so as to overlie said second surface part of said third surface portion of said semiconductor body, that portion of said semiconductor body lying beneath said gate electrode serving as a channel region of said device said gate electrode being applied with a gate voltage for inducing a conductive channel through said channel region;

said device being reverse-biased, so that a first depletion region extends from said third PN junction into said third semiconductor region and said semiconductor body and a second depletion region extends from said fourth PN junction into said third semiconductor region and said fourth semiconductor region;

said semiconductor body having a first ON resistance in a first current flow path therethrough between said first and second semiconductor regions, and said fourth semiconductor region providing a second ON resistance, less than said first ON resistance, in a second current flow path along the surface of said semiconductor body from said first semiconductor region through said channel and said third and fourth semiconductor regions to said second semiconductor region, so that said fourth semiconductor region serves to provide a reduced resistance current flow path in parallel with said first current flow path, thereby effectively reducing the total ON resistance of the overall current

12

flow path between said first and second semiconductor regions; and

wherein the impurity concentration said fourth semiconductor region is such that said fourth semiconductor is completely depleted by said second depletion region at a reverse bias less than that at which said first and second depletion regions come together within and punch through said third semiconductor region.

8. A high voltage MOS transistor comprising:

a semiconductor substrate of a first conductivity type having a surface,

a pair of laterally spaced source and drain pockets of semiconductor material of a second conductivity type within the substrate and adjoining the substrate surface,

an extended drain region of the second conductivity type extending laterally each way from said drain pocket to surface-adjoining positions,

a surface adjoining, top layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain pocket and the surface-adjoining positions,

said top layer of material and said substrate being subject to application of a reverse-bias voltage,

an insulating layer on the surface of the substrate and covering at least that portion between the source pocket and the nearest surface-adjoining position of the extended drain region, and

a gate electrode on the insulating layer and electrically isolated from the substrate region thereunder which forms a channel laterally between the source pocket and the nearest surface-adjoining position of the extended drain region, said gate electrode controlling by field-effect the flow of current thereunder through the channel.

9. A high voltage MOS transistor according to claim 8, wherein said extended drain region has an impurity concentration greater than $1 \times 10^{12} \text{ cm}^{-2}$.

10. A high voltage MOS transistor according to claim 8, further including an ohmic contact region of said first conductivity type formed in a surface adjoining portion of said semiconductor substrate, said ohmic contact region overlapping said top layer of material.

11. A high voltage MOS transistor comprising: semiconductor material of a first conductivity type having a surface,

a pair of laterally spaced source and drain pockets of semiconductor material of a second conductivity type within the substrate and adjoining the surface of said semiconductor material,

an extended drain region of the second conductivity type extending laterally from said drain pocket to a surface-adjoining position,

a surface adjoining top layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain pocket and said surface-adjoining position,

said top layer of material and said semiconductor material being subject to application of a reverse-bias voltage,

an insulating layer on the surface of said semiconductor material and covering at least that portion between the source pocket and the nearest surface-adjoining position of the extended drain region, and

a gate electrode on the insulating layer and electrically isolated from a semiconductor material re-

13

gion thereunder containing a channel that extends laterally between the source pocket and the nearest surface-adjointing position of the extended drain region, said gate electrode controlling by field-effect the flow of current thereunder through the channel.

12. A high voltage MOS transistor according to claim 11, wherein said extended drain region extends in a plurality of different directions from said drain pocket to respective plural surface adjoining positions.

13. A high voltage MOS transistor according to claim 11, wherein said extended drain region surrounds said drain pocket and extends to a surrounding surface adjoining position.

14. A high voltage MOS transistor according to claim 11, wherein said drain pocket comprises a first relatively deep pocket of a first impurity concentration and a second relatively shallow pocket formed in a surface portion of said first relatively deep pocket and having a second impurity concentration greater than said first impurity concentration and providing a drain contact region.

15. A high voltage MOS transistor according to claim 11, wherein said extended drain region has an impurity concentration greater than $1 \times 10^{12} \text{ cm}^{-2}$.

16. A high voltage MOS transistor according to claim 11, further including an ohmic contact region of said first conductivity type formed in a surface adjoining portion of said semiconductor material, said ohmic contact region overlapping said top layer of material.

17. A high voltage field effect transistor device comprising:

semiconductor material of a first conductivity type having a surface;

a source region of a second conductivity type formed in a first surface portion of said semiconductor material;

a drain region of said second conductivity type formed in a second surface portion of said semiconductor material spaced apart from said first surface portion by a third surface portion therebetween; an extended drain region of said second conductivity type extending from said drain region beneath a first portion of said third surface portion of said semiconductor material, to adjoin a second portion of said third surface portion of said semiconductor material, spaced apart from said said second surface portion of said semiconductor material, by said first portion of said third surface portion of said semiconductor material;

a surface region of said first conductivity type formed in said first portion of said third surface portion of said semiconductor material;

an insulating layer disposed on said surface of said semiconductor material, so as to overlie a third portion of said third surface portion of said semiconductor material between the second portion of said third surface portion of said semiconductor material and said first surface portion of said semiconductor material; and

a gate electrode disposed on that portion of said insulating layer overlying said third portion of said third surface portion of said semiconductor material, and wherein said surface region and said semiconductor material are subject to the application of a reverse bias voltage.

18. A high voltage field effect transistor device according to claim 17, wherein said extended drain region

14

extends laterally in a plurality of different directions from said drain region to adjoin said second portion of said third surface portion of said semiconductor material and to adjoin a fifth surface portion of said semiconductor material

19. A high voltage field effect transistor device according to claim 17, wherein said extended drain region surrounds said drain region and extends to a surrounding surface-adjointing portion of said semiconductor material.

20. A high voltage field effect transistor device according to claim 17, wherein said drain region comprises a first relatively deep region of a first impurity concentration and a second relatively shallow region formed in a surface portion of said first relatively deep region and having a second impurity concentration greater than said first impurity concentration and providing a drain contact region.

21. A high voltage field effect transistor device according to claim 17, wherein said extended drain region has an impurity concentration greater than $1 \times 10^{12} \text{ cm}^{-2}$.

22. A high voltage field effect transistor device according to claim 17, further including an ohmic contact region of said first conductivity type formed in a surface adjoining portion of said semiconductor material, said ohmic contact region overlapping said surface region.

23. An integrated MOS/JFET transistor device comprising an insulated gate field effect transistor and a double-sided junction field effect transistor integrated together in semiconductor substrate which contains a source region, and a drain region, and a dual channel path formed in said semiconductor material between said source and drain regions, said dual channel path comprising an insulated gate-controlled channel region having a first conductivity type in the presence of a channel-inducing gate voltage, said insulated gate controlled channel region being contiguous with a double-sided junction channel region of said first conductivity type, and wherein said source region adjoins said insulated gate-controlled channel region and said drain region adjoins said double-sided channel region.

24. An integrated MOS/JFET transistor device according to claim 23, wherein said insulated gate-controlled channel region comprises a surface portion of said semiconductor material adjoining said source region, and wherein said double-sided junction channel region comprises an extended drain region extending laterally from said drain region beneath a top gate region to said surface portion of said semiconductor material, an underlying portion of said semiconductor material extending beneath and adjoining said extended drain region and forming a bottom gate, said top gate region and said bottom gate forming respective PN junctions with said double-sided junction channel region.

25. An integrated MOS/JFET transistor device according to claim 23, wherein said extended drain region and said double-sided junction channel region surround said drain region and extend to a surrounding surface-adjointing position.

26. An integrated MOS/JFET transistor device according to claim 23, wherein said extended drain region and said double, wherein said drain region comprises a first relatively deep region of a first impurity concentration and a second relatively shallow region formed in a surface portion of said first relatively deep region and having a second impurity concentration greater than

15

said first impurity concentration and providing a drain contact region.

27. An integrated MOS/IFET transistor device according to claim 23, wherein said extended drain region and said double, further including an ohmic contact region of said first conductivity type formed in a surface adjoining portion of said semiconductor material, said ohmic contact region overlapping said top gate.

28. An integrated MOS/IFET transistor device according to claim 23, wherein said extended drain region has an impurity concentration greater than $1 \times 10^{12} \text{ cm}^{-2}$.

29. A high voltage MOS transistor comprising: semiconductor material of a first conductivity type having a surface;

source and drain regions of a second conductivity type adjoining spaced apart portions of the surface of said semiconductor material;

an extended drain region of said second conductivity type extending laterally from said drain region through said semiconductor material to a surface-adjoining portion of the surface of said semiconductor material;

a top gate semiconductor layer of said first conductivity type adjoining said drain region and adjoining said extended drain region along the surface of said semiconductor material to said surface-adjoining portion of the surface of said semiconductor material, said top gate semiconductor layer and said semiconductor material being subject to the application of a reverse-bias voltage;

an insulating layer on the surface of the semiconductor material and covering at least that portion of the surface of said semiconductor material between said source region and said surface-adjoining portion of said extended drain region; and

a gate electrode disposed on said insulating layer and being electrically isolated from that portion of the surface of said semiconductor material thereunder which forms a channel laterally between said source region and said surface-adjoining portion of said extended drain region, said gate electrode controlling, by field-effect, the flow of current thereunder through said channel.

30. A high voltage MOS transistor according to claim 29, wherein said extended drain region extends laterally each way from said drain region to surface-adjoining portions of the surface of said semiconductor material, and wherein said top gate semiconductor layer extends laterally in a plurality of different directions from said drain region and adjoins said extended drain region along the surface of said semiconductor material to said surface-adjoining portions of the surface of said semiconductor material.

31. A high voltage MOS transistor according to claim 29, wherein said extended drain region surrounds said drain region and extends to a surrounding surface adjoining position.

32. A high voltage MOS transistor according to claim 29, wherein said drain region comprises a first relatively deep region of a first impurity concentration and a second relatively shallow region formed in a surface portion of said first relatively deep region and having a second impurity concentration greater than said first impurity concentration and providing a drain contact region.

33. A high voltage MOS transistor according to claim 29, wherein said extended drain region has an impurity concentration greater than $1 \times 10^{12} \text{ cm}^{-2}$.

34. A high voltage MOS transistor according to claim 29, further including an ohmic contact region of said

16

first conductivity type formed in a surface adjoining portion of said semiconductor material, said ohmic contact region overlapping said top gate layer.

35. A high voltage diode comprising:

semiconductor material of a first conductivity type having a surface,

a first, surface-adjoining region of a second conductivity type;

a second surface-adjoining region of said first conductivity type spaced apart from said first, surface-adjoining region;

a third region of said second conductivity type extending laterally from said first, surface-adjoining region; and

a fourth, surface-adjoining region of said first conductivity type overlying an intermediate portion of said third, laterally extending and surface-adjoining region.

36. A high voltage diode according to claim 35, wherein said third region surrounds said first, surface-adjoining region and extends to a surrounding surface adjoining position.

37. A high voltage diode according to claim 35, wherein said first region comprises a first relatively deep region of a first impurity concentration and a second relatively shallow region formed in a surface portion of said first relatively deep region and having a second impurity concentration greater than said first impurity concentration.

38. A high voltage diode according to claim 35, wherein said third region has an impurity concentration greater than $1 \times 10^{12} \text{ cm}^{-2}$.

39. A lateral bipolar transistor having a high voltage base-collector diode comprising:

semiconductor material of a first conductivity type having a surface and forming a base of said bipolar transistor,

a first, surface-adjoining collector region of a second conductivity type forming a base-collector junction with said semiconductor material;

a second surface-adjoining base region of said first conductivity type spaced apart from said first, surface-adjoining collector region;

a third, extended collector region of said second conductivity type extending laterally from said first, surface-adjoining collector region, so that said base-collector junction extends laterally from said first, surface adjoining collector region;

a fourth, surface-adjoining region of said first conductivity type overlying an intermediate portion of said third, laterally extending and surface-adjoining extended collector region; and

a fifth, surface-adjoining emitter region of said second conductivity type formed in said second surface-adjoining base region and defining therewith an emitter-base junction.

40. A lateral bipolar transistor according to claim 39, wherein said third region surrounds said first, surface-adjoining region and extends to a surrounding surface adjoining position.

41. A lateral bipolar transistor according to claim 39, wherein said first region comprises a first relatively deep region of a first impurity concentration and a second relatively shallow region formed in a surface portion of said first relatively deep region and having a second impurity concentration greater than said first impurity concentration.

42. A lateral bipolar transistor according to claim 39, wherein said third, extended collector region has an impurity concentration greater than $1 \times 10^{12} \text{ cm}^{-2}$.

* * * * *

JS-44 civil cover sheet and the information contained herein neither replace nor supplement the filing and service of pleadings or other papers as required by law, except as provided by local rules of court. This form, approved by the Judicial Conference of the United States in September 1974, is required for the use of the Clerk of Court for the purpose of initiating the civil docket sheet. (SEE INSTRUCTIONS ON THE REVERSE OF THE FORM)

I. (a) PLAINTIFFS

FAIRCHILD SEMICONDUCTOR CORPORATION,
a Delaware Corporation, and INTERSIL CORPORATION, a Delaware Corporation

(b) County of Residence of First Listed Plaintiff Delaware
(EXCEPT IN U.S. PLAINTIFF CASES)

(c) Attorney's (Firm Name, Address, and Telephone Number)
G. Hopkins Guy, III
ORRICK, HERRINGTON & SUTCLIFFE, LLP
1000 Marsh Road
Menlo Park, CA 94025
(650) 614-7400

DEFENDANTS

POWER INTEGRATIONS, INC., a Delaware Corporation

County of Residence of First Listed Defendant Delaware

(IN U.S. PLAINTIFF CASES, USE THE LOCATION OF THE

NOTE: IN LAND CONDEMNATION CASES, USE THE LOCATION OF THE LAND INVOLVED

Attorneys (If Known)

RECEIVED
U.S. DISTRICT COURT
EASTERN DISTRICT OF TEXAS

APR 11 2006

II. BASIS OF JURISDICTION (Place an "X" in One Box Only)

- ☐ 1 U.S. Government Plaintiff
- ☒ 3 Federal Question (U.S. Government Not a Party)
- ☐ 2 U.S. Government Defendant
- ☐ 4 Diversity (Indicate Citizenship of Parties in Item III)

III. CITIZENSHIP OF PRINCIPAL PARTIES (Place an "X" in One Box for Plaintiff and One Box for Defendant)

- | | | | | | |
|---|----------------------------|----------------------------|---|----------------------------|----------------------------|
| | PTF | DEF | | PTF | DEF |
| Citizen of This State | <input type="checkbox"/> 1 | <input type="checkbox"/> 1 | Incorporated or Principal Place of Business In This State | <input type="checkbox"/> 4 | <input type="checkbox"/> 4 |
| Citizen of Another State | <input type="checkbox"/> 2 | <input type="checkbox"/> 2 | Incorporated and Principal Place of Business In Another State | <input type="checkbox"/> 5 | <input type="checkbox"/> 5 |
| Citizen or Subject of a Foreign Country | <input type="checkbox"/> 3 | <input type="checkbox"/> 3 | Foreign Nation | <input type="checkbox"/> 6 | <input type="checkbox"/> 6 |

IV. NATURE OF SUIT (Place an "X" in One Box Only)

CONTRACT	TORTS	FORFEITURE/PENALTY	BANKRUPTCY	OTHER STATUTES
<input type="checkbox"/> 110 Insurance <input type="checkbox"/> 120 Marine <input type="checkbox"/> 130 Miller Act <input type="checkbox"/> 140 Negotiable Instrument <input type="checkbox"/> 150 Recovery of Overpayment & Enforcement of Judgment <input type="checkbox"/> 151 Medicare Act <input type="checkbox"/> 152 Recovery of Defaulted Student Loans (Excl. Veterans) <input type="checkbox"/> 153 Recovery of Overpayment of Veteran's Benefits <input type="checkbox"/> 160 Stockholders' Suits <input type="checkbox"/> 190 Other Contract <input type="checkbox"/> 195 Contract Product Liability	PERSONAL INJURY <input type="checkbox"/> 310 Airplane <input type="checkbox"/> 315 Airplane Product Liability <input type="checkbox"/> 320 Assault Libel & Slander <input type="checkbox"/> 330 Federal Employers Liability <input type="checkbox"/> 340 Marine <input type="checkbox"/> 345 Marine Product Liability <input type="checkbox"/> 350 Motor Vehicle <input type="checkbox"/> 355 Motor Vehicle Product Liability <input type="checkbox"/> 360 Other Personal Injury	<input type="checkbox"/> 610 Agriculture <input type="checkbox"/> 620 Other Food & Drug <input type="checkbox"/> 625 Drug Related Seizure of Property 21 USC 881 <input type="checkbox"/> 630 Liquor Laws <input type="checkbox"/> 640 R.R. & Truck <input type="checkbox"/> 650 Airline Regs. <input type="checkbox"/> 660 Occupational Safety/Health <input type="checkbox"/> 690 Other	<input type="checkbox"/> 422 Appeal 28 USC 158 <input type="checkbox"/> 423 Withdrawal 28 USC 157 PROPERTY RIGHTS <input type="checkbox"/> 820 Copyrights <input checked="" type="checkbox"/> 830 Patent <input type="checkbox"/> 840 Trademark	<input type="checkbox"/> 400 State Reapportionment <input type="checkbox"/> 410 Antitrust <input type="checkbox"/> 430 Banks and Banking <input type="checkbox"/> 450 Commerce/ICC Rates/etc <input type="checkbox"/> 460 Deportation <input type="checkbox"/> 470 Racketeer Influenced and Corrupt Organizations <input type="checkbox"/> 810 Selective Service <input type="checkbox"/> 850 Securities/Commodities/Exchange <input type="checkbox"/> 875 Customer Challenge 12 USC 3410 <input type="checkbox"/> 891 Agricultural Acts <input type="checkbox"/> 892 Economic Stabilization Act <input type="checkbox"/> 893 Environmental Matters <input type="checkbox"/> 894 Energy Allocation Act <input type="checkbox"/> 895 Freedom of Information Act <input type="checkbox"/> 900 Appeal of Fee Determination Under Equal Access to Justice <input type="checkbox"/> 950 Constitutionality of State Statutes <input type="checkbox"/> 890 Other Statutory Actions
REAL PROPERTY <input type="checkbox"/> 210 Land Condemnation <input type="checkbox"/> 220 Foreclosure <input type="checkbox"/> 230 Rent Lease & Ejectment <input type="checkbox"/> 240 Torts to Land <input type="checkbox"/> 245 Tort Product Liability <input type="checkbox"/> 290 All Other Real Property	CIVIL RIGHTS <input type="checkbox"/> 441 Voting <input type="checkbox"/> 442 Employment <input type="checkbox"/> 443 Housing/Accommodations <input type="checkbox"/> 444 Welfare <input type="checkbox"/> 440 Other Civil Rights	PRISONER PETITIONS <input type="checkbox"/> 510 Motions to Vacate Sentence <input type="checkbox"/> Habeas Corpus: <input type="checkbox"/> 530 General <input type="checkbox"/> 535 Death Penalty <input type="checkbox"/> 540 Mandamus & Other <input type="checkbox"/> 550 Civil Rights <input type="checkbox"/> 555 Prison Condition	LABOR <input type="checkbox"/> 710 Fair Labor Standards Act <input type="checkbox"/> 720 Labor/Mgmt. Relations <input type="checkbox"/> 730 Labor/Mgmt. Reporting & Disclosure Act <input type="checkbox"/> 740 Railway Labor Act <input type="checkbox"/> 790 Other Labor Litigation <input type="checkbox"/> 791 Empl. Ret. Inc. Security Act	SOCIAL SECURITY <input type="checkbox"/> 861 HIA (1395ff) <input type="checkbox"/> 862 Black Lung (923) <input type="checkbox"/> 863 DIWC/DIWW (405(g)) <input type="checkbox"/> 864 SSID Title XVI <input type="checkbox"/> 865 RSI (405(g)) FEDERAL TAX SUITS <input type="checkbox"/> 870 Taxes (U.S. Plaintiff or Defendant) <input type="checkbox"/> 871 IRS—Third Party 26 USC 7609

V. ORIGIN (PLACE AN "X" IN ONE BOX ONLY)

- ☒ 1 Original Proceeding
- ☐ 2 Removed from State Court
- ☐ 3 Remanded from Appellate Court
- ☐ 4 Reinstated or Reopened
- ☐ 5 Transferred from another district (specify)
- ☐ 6 Multidistrict Litigation
- ☐ 7 Appeal to District Judge from Magistrate Judgment

VI. CAUSE OF ACTION (Cite the U.S. Civil Statute under which you are filing and write brief statement of cause. Do not cite jurisdictional statutes unless diversity.)

28 USC 31338 Patent infringement

VII. REQUESTED IN COMPLAINT:

☐ CHECK IF THIS IS A CLASS ACTION UNDER F.R.C.P. 23

DEMAND \$

CHECK YES only if demanded in complaint:
JURY DEMAND: ☒ Yes ☐ No

VIII. RELATED CASE(S) (See instructions):

IF ANY

JUDGE

DOCKET NUMBER

DATE

SIGNATURE OF ATTORNEY OF RECORD

FOR OFFICE USE ONLY

RECEIPT # _____ AMOUNT _____ APPLYING IFP _____ JUDGE _____ MAG. JUDGE _____

AO 120 (Rev. 3/04)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
--	--

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been
 filed in the U.S. District Court Marshall, Texas on the following ☒ Patents or ☐ Trademarks:

DOCKET NO. 2:06cv151	DATE FILED 4/11/2006	U.S. DISTRICT COURT Marshall, Texas
PLAINTIFF		DEFENDANT
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY	
	<input type="checkbox"/> Amendment <input type="checkbox"/> Answer <input type="checkbox"/> Cross Bill <input type="checkbox"/> Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
 Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

**IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION**

**FAIRCHILD SEMICONDUCTOR,
CORPORATION, a Delaware
Corporation, and INTERSIL
CORPORATION, a Delaware Corporation,**

Plaintiffs.

CIVIL ACTION NO. 2-06-CV-151

VS.

**POWER INTEGRATIONS, INC. a
Delaware Corporation,**

Defendants.

NOTICE OF APPEARANCE

The following designated attorney hereby enters an appearance as additional counsel of record for Plaintiffs Fairchild Semiconductor, Corporation and Intersil Corporation, and is authorized to receive service on all pleadings, notices, orders and other papers in the above-captioned matter on behalf of Plaintiffs.

Michael C. Smith
State Bar No. 18650410
THE ROTH LAW FIRM
115 N. Wellington, Suite 200
Marshall, Texas 75670
Telephone: (903) 935-1665
Facsimile: (903) 935-1797
Email: ms@rothfirm.com

Respectfully submitted,



Carl R. Roth, Texas Bar No. 901984225

cr@rothfirm.com

Michael C. Smith, Texas Bar No. 900641877

ms@rothfirm.com

THE ROTH LAW FIRM, P.C.

115 North Wellington, Suite 200

P.O. Box 876

Marshall, Texas 75671

Tel: (903) 935-1665

Fax: (903) 935-1797

ORRICK, HERRINGTON & SUTCLIFFE LLP

G. Hopkins Guy, III (Calif. SBN 124811)

Vickie Feeman (Calif. SBN 177487)

Bas de Blank (Calif. SBN 191487)

Brian Vander Zanden (Calif. SBN 233134)

1000 Marsh Road

Menlo Park, CA 94025

(650) 614-7400

Attorneys for Plaintiffs,

FAIRCHILD SEMICONDUCTOR

CORPORATION and INTERSIL

CORPORATION

SHORE CHAN, L.L.P.

Michael Shore, Texas Bar No. 18294915

shore@shorechan.com

Jeffrey R. Bragalone, Texas Bar No. 02855775

jbragalone@shorechan.com

325 North St. Paul, Suite 4450

Dallas, Texas 75201

Tel: (214) 593-9110

Fax: (214) 593-9111

ATTORNEYS FOR INTERSIL

CORPORATION

CERTIFICATE OF SERVICE

The undersigned hereby certifies that all counsel of record who are deemed to have consented to electronic service are being served with a copy of this document via the Court's CM/ECF system per Local Rule CV-5(a)(3) this 12th day of April, 2006. Any other counsel of record will be served by facsimile transmission and/or first class mail.


Michael Smith

IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

FAIRCHILD SEMICONDUCTOR	§	
CORPORATION, a Delaware corporation,	§	
And INTERSIL CORPORATION, a Delaware	§	
Corporation	§	
	§	
v.	§	C.A. No. 2:06cv151 (TJW)
	§	JURY
POWER INTEGRATIONS, INC. a Delaware	§	
Corporation	§	

**NOTICE OF APPEARANCE OF COUNSEL
FOR DEFENDANT POWER INTEGRATIONS, INC.**

Defendant, POWER INTEGRATIONS, INC., files this Notice of Appearance of Counsel, and hereby notifies the Court that Michael E. Jones of the law firm Potter Minton, A Professional Corporation, 110 N. College, Suite 500, Tyler, Texas 75702, is appearing as counsel in the above-referenced matter. All pleadings, discovery, correspondence and other material should be served upon counsel at the address referenced above.

Respectfully submitted,

/s/ Michael E. Jones
Michael E. Jones
State Bar No. 10929400
mikejones@potterminton.com
POTTER MINTON
A Professional Corporation
110 N. College, Suite 500
Tyler, Texas 75702
903/597-8311
903/593-0846 Facsimile

ATTORNEYS FOR
POWER INTEGRATIONS, INC.

CERTIFICATE OF SERVICE

I hereby certify that all counsel of record who have consented to electronic service and are being served with a copy of this document via the Court's CM/ECF system per Local Rule CV-5(a)(3) on this the 21ST day of April, 2006. Any other counsel of record will be served by first class mail.

/s/ Michael E. Jones
Michael E. Jones

UNITED STATES DISTRICT COURT

EASTERN

District of

TEXAS

FILED-CLERK
DISTRICT COURT
APR 21 AM 10:23

FAIRCHILD SEMICONDUCTOR CORPORATION,
a Delaware Corporation, and INTERSIL CORPORATION,
a Delaware Corporation

Plaintiffs

V

POWER INTEGRATIONS, INC., a Delaware
Corporation

Defendant

SUMMONS IN A CIVIL CASE

TX EASTERN-MARSHALL

CASE NUMBER: 2-06cv-151

TO: (Name and address of Defendant)

POWER INTEGRATIONS, INC., a Delaware corporation, by and through its registered agent for service,
Incorporating Services, Ltd., 3500 South Dupont Highway, Dover, Delaware 19901.

YOU ARE HEREBY SUMMONED and required to serve upon PLAINTIFF'S ATTORNEY (name and address)

G. Hopkins Guy, III
Orrick, Herrington & Sutcliffe, LLP
1000 Marsh Road
Menlo Park, CA 94025

an answer to the complaint which is herewith served upon you, within twenty (20) days after service of this
summons upon you, exclusive of the day of service. If you fail to do so, judgment by default will be taken against you for
the relief demanded in the complaint. You must also file your answer with the Clerk of this Court within a reasonable
period of time after service.

DAVID MALAND, CLERK

APR 11 2006

CLERK

DATE

(By) DEPUTY CLERK

(By) DEPUTY CLERK

AO 440 (Rev. 10-93) Summons in a Civil Action

RETURN OF SERVICE

Service of the Summons and complaint was made by me ⁽¹⁾	DATE <u>4-12-06</u>
NAME OF SERVER (PRINT) <u>Hall Reavis</u>	TITLE <u>Investigator</u>

Check one box below to indicate appropriate method of service

- ☐ Served personally upon the defendant. Place where served: _____
- ☐ Left copies thereof at the defendant's dwelling house or usual place of abode with a person of suitable age and discretion then residing therein
Name of person with whom the summons and complaint were left: _____
- ☐ Returned unexecuted: _____
- ☐ Other (specify): certified mail

STATEMENT OF SERVICE FEES

TRAVEL	SERVICES	TOTAL
--------	----------	-------

DECLARATION OF SERVER

I declare under penalty of perjury under the laws of the United States of America that the foregoing information contained in the Return of Service and Statement of Service Fees is true and correct.

Executed on 4-12-06 Date Hall Reavis Signature of Server

18 Pineburr Circle Address of Server
Marshall, TX 75670

SENDER: COMPLETE THIS SECTION ■ Complete items 1, 2, and 3. Also complete item 4 if Restricted Delivery is desired. ■ Print your name and address on the reverse so that we can return the card to you. ■ Attach this card to the back of the mailpiece, or on the front if space permits.		COMPLETE THIS SECTION ON DELIVERY A. Signature <u>[Signature]</u> <input checked="" type="checkbox"/> Agent <input type="checkbox"/> Addressee B. Received by (Printed Name) <u>[Signature]</u> C. Date of Delivery <u>4-12-06</u> D. Is delivery address different from item 1? <input type="checkbox"/> Yes <input checked="" type="checkbox"/> No If YES, enter delivery address below: _____		MAIL RECEIPT (Insurance Coverage Provided) Visit our website at www.usps.com SPECIAL USE UNIT ID: 0670 Postmark Here Clerk: <u>[Signature]</u> 04/12/06 APR 12 2006 1-800-4USPS
1. Article Addressed to: Power Integrations, Inc. Registered Agent for Service Incorporating Services, Ltd 3500 South Dupont Highway Dover, Delaware 19901		3. Service Type <input checked="" type="checkbox"/> Certified Mail <input type="checkbox"/> Express Mail <input type="checkbox"/> Registered <input checked="" type="checkbox"/> Return Receipt for Merchandise <input type="checkbox"/> Insured Mail <input type="checkbox"/> C.O.D. 4. Restricted Delivery? (Extra Fee) <input type="checkbox"/> Yes		
2. Article Number (Transfer from service label) <u>7005 1820 0002 7119 6171</u>		5. Delivery Point <u>3500 South Dupont Hwy</u> <u>Dover, Delaware 19901</u> See Reverse for Instructions		

IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

FAIRCHILD SEMICONDUCTOR	§	
CORPORATION, a Delaware corporation,	§	
And INTERSIL CORPORATION, a Delaware	§	
Corporation	§	
	§	
v.	§	C.A. No. 2:06cv151 (TJW)
	§	JURY
POWER INTEGRATIONS, INC. a Delaware	§	
Corporation	§	

**AGREED MOTION FOR EXTENSION OF TIME TO ANSWER, MOVE
OR OTHERWISE RESPOND**

POWER INTEGRATIONS, INC. moves the Court for an extension of time to answer, move or otherwise respond to FAIRCHILD SEMICONDUCTOR CORPORATION and INTERSIL CORPORATION's Original Complaint, and would respectfully show the Court as follows:

1. Plaintiffs, FAIRCHILD SEMICONDUCTOR CORPORATION and INTERSIL CORPORATION, filed their Original Complaint against POWER INTEGRATIONS on or about April 11, 2006 [Dkt. 1].

2. The issues involved in this case are such that POWER INTEGRATIONS, INC. requires additional time to prepare a response.

3. POWER INTEGRATIONS, INC. respectfully requests an extension of time to answer, move or otherwise respond, in any manner whatsoever, to Plaintiffs' Original Complaint, up to and including June 1, 2006.

4. Plaintiffs, FAIRCHILD SEMICONDUCTOR CORPORATION and INTERSIL CORPORATION, are not opposed to said extension of time to answer, move or otherwise respond.

WHEREFORE, PREMISES CONSIDERED, POWER INTEGRATIONS, INC. prays that the Court grant this Agreed Motion for Extension of Time by extending the time period for POWER INTEGRATIONS, INC. to answer or otherwise respond to Plaintiff's Complaint until June 1, 2006.

Respectfully submitted,

/s/ Michael E. Jones
MICHAEL E. JONES
State Bar No. 10929400
POTTER MINTON
A Professional Corporation
110 N. College, Suite 500 (75702)
P. O. Box 359
Tyler, Texas 75710
(903) 597 8311
(903) 593 0846 (Facsimile)
mikejones@potterminton.com

ATTORNEYS FOR DEFENDANT
POWER INTEGRATIONS, INC.

CERTIFICATE OF CONFERENCE

I certify that Michael Headley, counsel for Power Integrations, has conferred with Guy Hopkins, counsel for plaintiffs, and that Guy Hopkins states that plaintiffs are unopposed to the relief sought in this motion.

/s/ Michael E. Jones
Michael E. Jones

CERTIFICATE OF SERVICE

The undersigned hereby certifies that all counsel of record who are deemed to have consented to electronic service are being served with a copy of this document via the Court's CM/ECF system per Local Rule CV-5(a)(3) on May 1, 2006. Any other counsel of record will be served by facsimile transmission and first class mail.

/s/ Michael E. Jones
Michael E. Jones

IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

FAIRCHILD SEMICONDUCTOR	§	
CORPORATION, a Delaware corporation,	§	
And INTERSIL CORPORATION, a Delaware	§	
Corporation	§	
	§	
v.	§	C.A. No. 2:06cv151 (TJW)
	§	JURY
POWER INTEGRATIONS, INC. a Delaware	§	
Corporation	§	

**ORDER GRANTING POWER INTEGRATION'S AGREED MOTION FOR
EXTENSION OF TIME TO ANSWER, MOVE OR OTHERWISE RESPOND**

ON THIS DAY, came on to be considered the Agreed Motion for Extension of Time to Answer, Move or Otherwise Respond to the Original Complaint of Plaintiffs, FAIRCHILD SEMICONDUCTOR CORPORATION and INTERSIL CORPORATION in the above-styled and numbered cause up to and including June 1, 2006. After considering said motion, the Court is of the opinion that said motion should be GRANTED.

IT IS THEREFORE ORDERED that POWER INTEGRATION shall have up to and including June 1, 2006 to answer, move or otherwise respond in any manner whatsoever to Plaintiffs', FAIRCHILD SEMICONDUCTOR CORPORATION and INTERSIL CORPORATION's Original Complaint [Dkt. 1].

IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

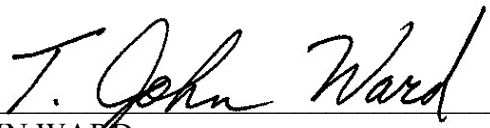
FAIRCHILD SEMICONDUCTOR	§	
CORPORATION, a Delaware corporation,	§	
And INTERSIL CORPORATION, a Delaware	§	
Corporation	§	
	§	
v.	§	C.A. No. 2:06cv151 (TJW)
	§	JURY
POWER INTEGRATIONS, INC. a Delaware	§	
Corporation	§	

**ORDER GRANTING POWER INTEGRATION'S AGREED MOTION FOR
EXTENSION OF TIME TO ANSWER, MOVE OR OTHERWISE RESPOND**

ON THIS DAY, came on to be considered the Agreed Motion for Extension of Time to Answer, Move or Otherwise Respond to the Original Complaint of Plaintiffs, FAIRCHILD SEMICONDUCTOR CORPORATION and INTERSIL CORPORATION in the above-styled and numbered cause up to and including June 1, 2006. After considering said motion, the Court is of the opinion that said motion should be GRANTED.

IT IS THEREFORE ORDERED that POWER INTEGRATION shall have up to and including June 1, 2006 to answer, move or otherwise respond in any manner whatsoever to Plaintiffs', FAIRCHILD SEMICONDUCTOR CORPORATION and INTERSIL CORPORATION's Original Complaint [Dkt. 1].

SIGNED this 2nd day of May, 2006.



T. JOHN WARD
UNITED STATES DISTRICT JUDGE

IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS

FAIRCHILD SEMICONDUCTOR
CORPORATION, a Delaware corporation,
INTERSIL AMERICAS, INC., a Delaware
corporation and INTERSIL CORPORATION,
a Delaware corporation

Plaintiff,

v.

POWER INTEGRATIONS, INC., a Delaware
corporation,

Defendants.

JURY

CIVIL ACTION NO. 2:06-cv-151

PLAINTIFFS' AMENDED COMPLAINT

Plaintiffs FAIRCHILD SEMICONDUCTOR CORPORATION (hereinafter, "Fairchild"), INTERSIL AMERICAS, INC. and INTERSIL CORPORATION, (Intersil Americas, Inc. and Intersil Corp. are collectively "Intersil") by and through their undersigned counsel, hereby alleges as follows:

THE PARTIES

1. Fairchild Semiconductor Corporation is a Delaware corporation with its principal place of business in South Portland, Maine.

2. Intersil Corporation is a Delaware corporation with its principal place of business in Milpitas, California.

3. Intersil Americas, Inc. is a Delaware corporation with its principal place of business in Milpitas, California.

4. Power Integrations, Inc. is a Delaware is a Delaware corporation with its principal place of business in San Jose, California.

JURISDICTION AND VENUE

5. This is an action arising under the patent laws of the United States, Title 35 of the United States Code. This court has jurisdiction over the subject matter of this action pursuant to 28 U.S.C. §§ 1331 and 1338(a).

6. Upon information and belief, this Court has personal jurisdiction over the defendant because Power Integrations sells the accused devices within this district.

7. Upon information and belief, venue is proper in the Court pursuant to 28 U.S.C. § 1391(b) and (c) and § 1400 as the defendant is subject to personal jurisdiction in this district.

FIRST CAUSE OF ACTION

INFRINGEMENT OF U.S. PATENT NO. 5,264,719

8. The allegations of paragraphs 1-7 are incorporated as though fully set forth herein.

9. U.S. Patent No. 5,264,719 (the “719 Patent”), entitled *High Voltage Lateral Semiconductor Device*, duly and lawfully issued on November 23, 1993 and was assigned to Harris Corporation. A true and correct copy of the ‘719 Patent is attached hereto as Exhibit A.

10. Upon information and belief, on or about September 27, 1999 the ‘719 Patent was assigned by Harris Corporation to Intersil Corporation. A true and correct copy of that assignment is attached as Exhibit B.

11. Upon information and belief, on or about April 14, 2006, Intersil Corporation changed its name to Intersil Communications, Inc. A true and correct copy of the restated certificate of incorporation is attached as Exhibit C.

12. Upon information and belief, on or about April 14, 2006 the ‘719 Patent was assigned by Intersil Communications, Inc. to Intersil Americas, Inc. A true and correct copy of that assignment is attached as Exhibit D.

13. On or about March 30, 2006, Fairchild Semiconductor Corporation and Intersil Corporation entered into a Patent License Agreement that gave Fairchild the right to assert the

'719 Patent against Power Integrations. A redacted copy of that Patent License Agreement is attached as Exhibit E.

14. On or about May 17, 2006, Fairchild Semiconductor Corporation, Intersil Corporation, and Intersil Americas, Inc. entered into a Supplemental Agreement effective March 30, 2006 that gave Fairchild the right to assert the '719 Patent against Power Integrations. A true and correct copy of that Supplemental Agreement is attached as Exhibit F.

15. Upon information and belief, Power Integrations has been and is now infringing the '719 Patent, both literally and under the doctrine of equivalents, by making, using, selling, offering for sale, and importing devices and products in the United States covered by one or more claims of the '719 Patent.

16. Upon information and belief, Power Integrations has been and is now inducing infringement and contributing to the infringement of the '719 Patent, both literally and under the doctrine of equivalents, by inducing or contributing to the making, using, selling, offering for sale, and importing by others devices and products in the United States covered by one or more claims of the '719 Patent.

17. Power Integrations' infringement has caused irreparable injury to Fairchild and Intersil and will continue to cause irreparable injury until Power Integrations is enjoined from further infringement by the Court.

PRAYER FOR RELIEF

WHEREFORE, FAIRCHILD and INTERSIL pray for the following relief:

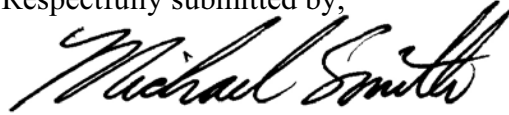
- A. Judgment by the Court that Power Integrations directly infringes the '719 Patent;
- B. Judgment by the Court that Power Integrations induces or contributes to others' infringement of the '719 Patent;
- C. Preliminary and permanent injunctive relief pursuant to 35 U.S.C. § 283 enjoining Power Integrations, its officers, agents, servants, employees, successors, assigns and all other persons or entities acting in concert or participation with Power Integrations or on Power Integrations' behalf from further infringement of the '719 Patent;

- D. Money damages sustained as a result of Power Integrations' infringement of the '719 Patent;
- E. Costs and reasonable attorneys' fees incurred in connection with this action pursuant to 35 U.S.C. § 285; and,
- F. Such other relief as the Court finds just and proper.

DEMAND FOR JURY TRIAL

Pursuant to Rule 38(b) of the Federal Rules of Civil Procedure, Fairchild Semiconductor Corporation and Intersil Corporation hereby demand a trial by jury on this action.

Respectfully submitted by,



ORRICK, HERRINGTON & SUTCLIFFE LLP
G. Hopkins Guy, III (SBN 124811)
Bas de Blank (SBN 191487)
1000 Marsh Road
Menlo Park, CA 94025
(650) 614-7400

Carl R. Roth, Texas Bar No. 901984225
cr@rothfirm.com
Michael C. Smith, Texas Bar No. 900641877
ms@rothfirm.com
THE ROTH LAW FIRM, P.C.
115 North Wellington, Suite 200
P.O. Box 876
Marshall, Texas 75671
Tel: (903) 935-1665
Fax: (903) 935-1797


Attorneys for Plaintiffs,
FAIRCHILD SEMICONDUCTOR
CORPORATION, INTERSIL CORPORATION,
and INTERSIL AMERICAS, INC.

SHORE CHAN, L.L.P.
Michael Shore, Texas Bar No. 18294915
shore@shorechan.com
Jeffrey R. Bragalone, Texas Bar No. 02855775
jbragalone@shorechan.com
325 North St. Paul, Suite 4450
Dallas, Texas 75201
Tel: (214) 593-9110
Fax: (214) 593-9111

Attorneys for Plaintiffs,
INTERFIL CORPORATION, and INTERFIL
AMERICAS, INC.

CERTIFICATE OF SERVICE

The undersigned hereby certifies that all counsel of record who are deemed to have consented to electronic service are being served with a copy of this document via the Court's CM/ECF system per Local Rule CV-5(a)(3) this 19th day of May, 2006. Any other counsel of record will be served by facsimile transmission and/or first class mail.



Michael C. Smith



US005264719A

United States Patent [19]

[11] Patent Number: 5,264,719

Beasom

[45] Date of Patent: Nov. 23, 1993

[54] HIGH VOLTAGE LATERAL SEMICONDUCTOR DEVICE

[75] Inventor: James D. Beasom, Melbourne Village, Fla.

[73] Assignee: Harris Corporation, Melbourne, Fla.

[21] Appl. No.: 705,509

[22] Filed: May 24, 1991

4,628,341 12/1986 Thomas 357/23.8
4,811,075 3/1989 Eklund et al. 357/46
4,994,889 2/1991 Takeuchi et al. 357/55
4,994,904 2/1991 Nakagawa et al. 357/38

Primary Examiner—Rolf Hille

Assistant Examiner—Roy Potter

Attorney, Agent, or Firm—Evenson, Wands, Edwards, Lenahan & McKeown

[57] ABSTRACT

The present invention provides an improved lateral drift region for both bipolar and MOS devices where improved breakdown voltage and low ON resistance are desired. A top gate of the same conductivity type as the device region with which it is associated is provided along the surface of the substrate and overlying the lateral drift region. In an MOS device, the extremity of the lateral drift region curves up to the substrate surface beyond the extremity of the top gate to thereby provide contact between the JFET channel and the MOS channel.

Related U.S. Application Data

[63] Continuation of Ser. No. 242,405, Sep. 8, 1988, abandoned, which is a continuation-in-part of Ser. No. 831,384, Jan. 7, 1986, Pat. No. 4,823,173.

[51] Int. Cl.⁵ H01L 29/80

[52] U.S. Cl. 257/335; 257/336;
257/339

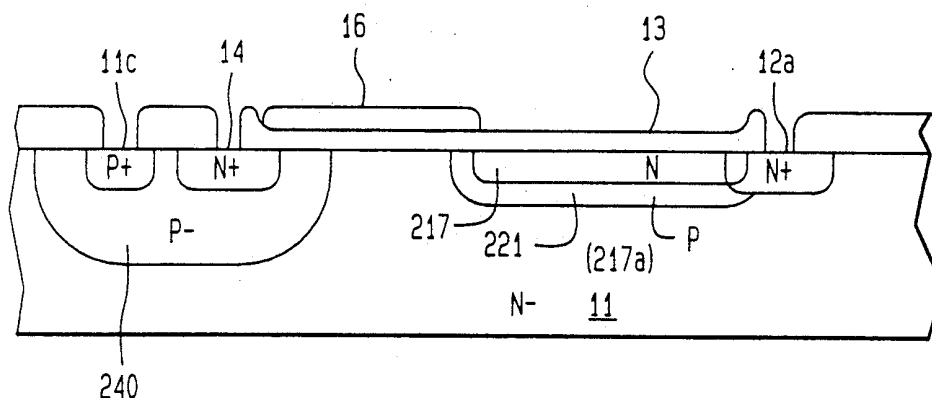
[58] Field of Search 357/38, 55, 23.8, 46

[56] References Cited

U.S. PATENT DOCUMENTS

4,626,879 12/1986 Colak 357/23.8

42 Claims, 7 Drawing Sheets



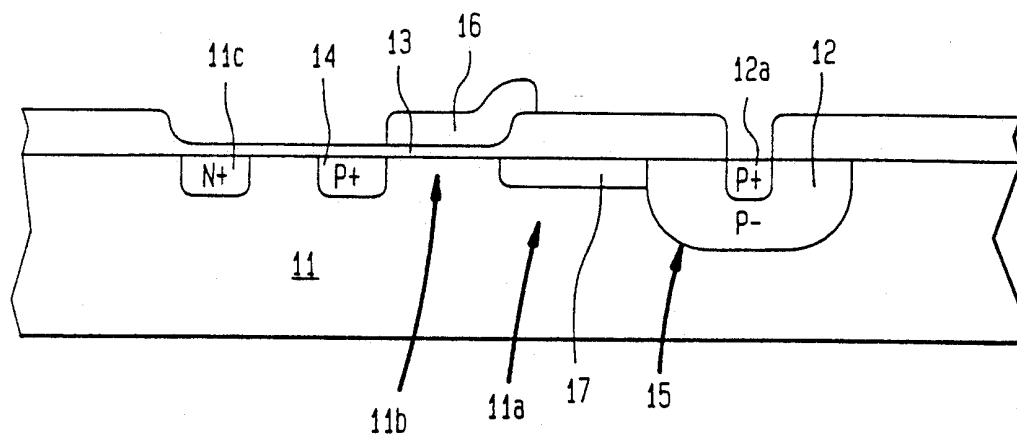


FIG. 1

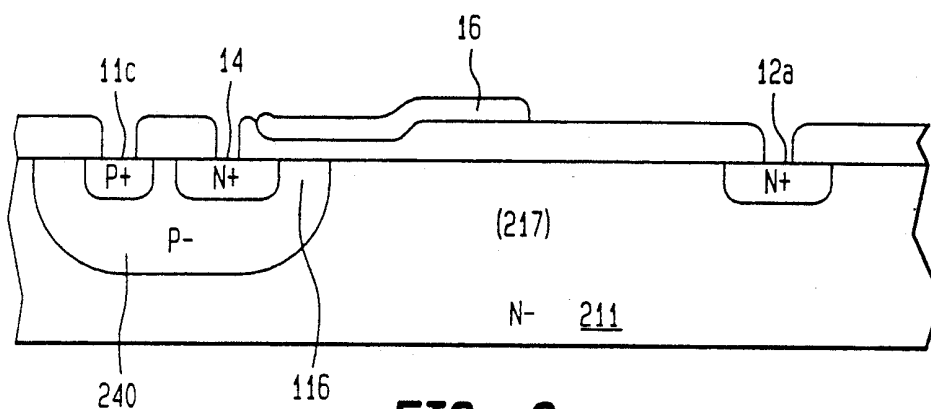


FIG. 2
(PRIOR ART)

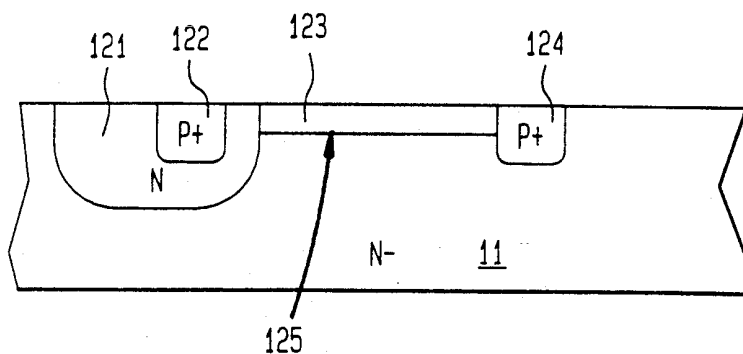


FIG. 3

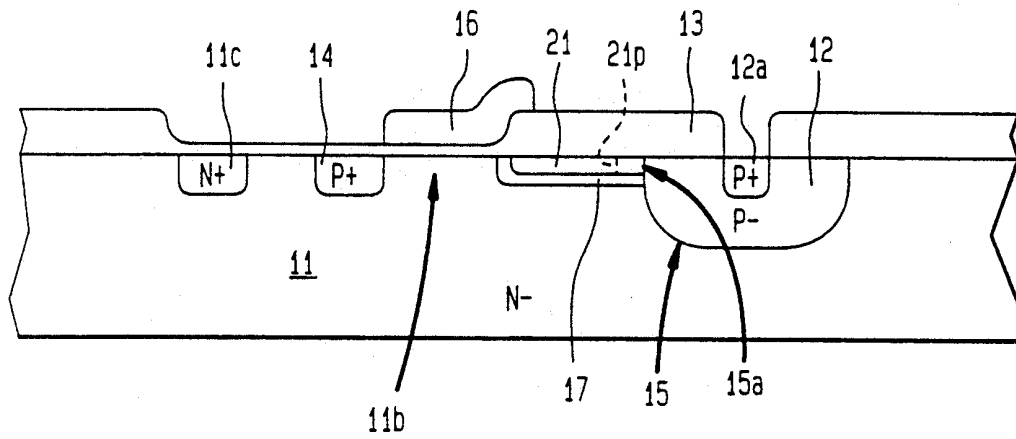


FIG. 4

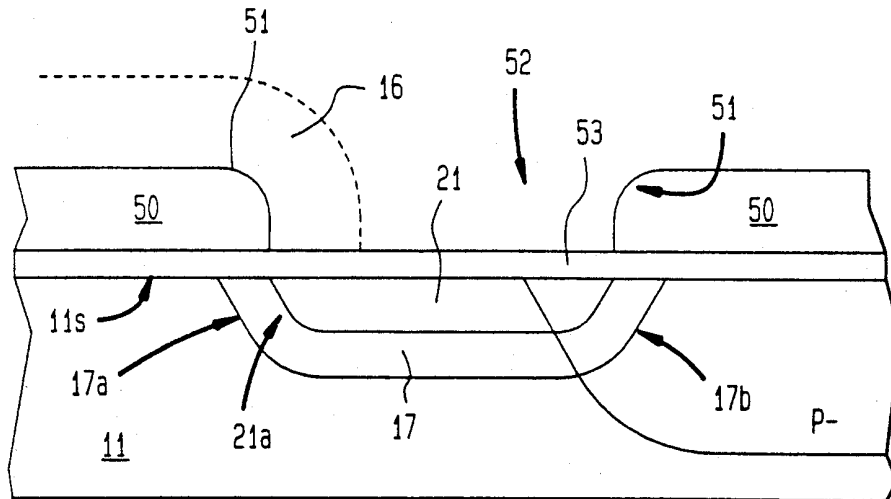


FIG. 5

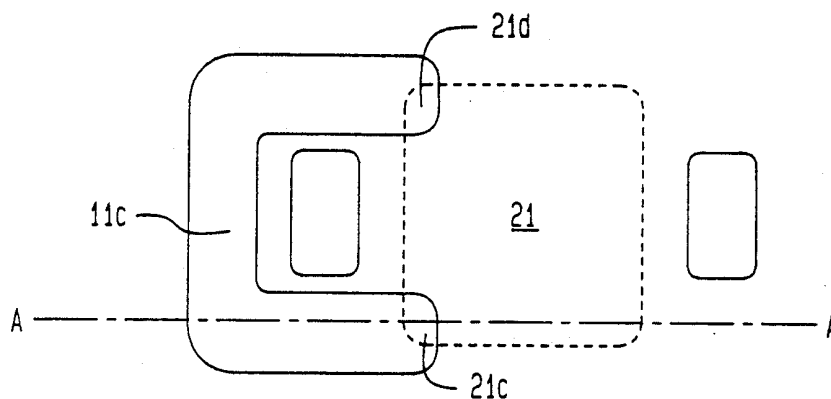


FIG. 6a

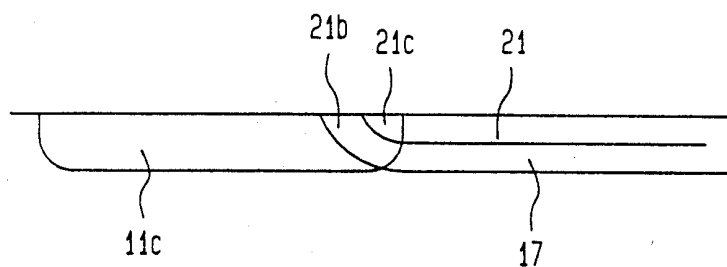


FIG. 6b

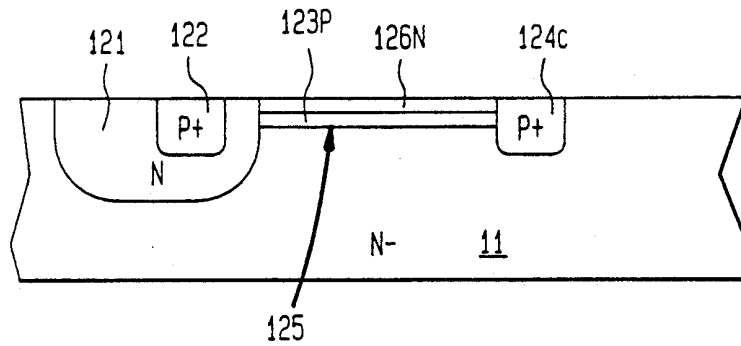


FIG. 7

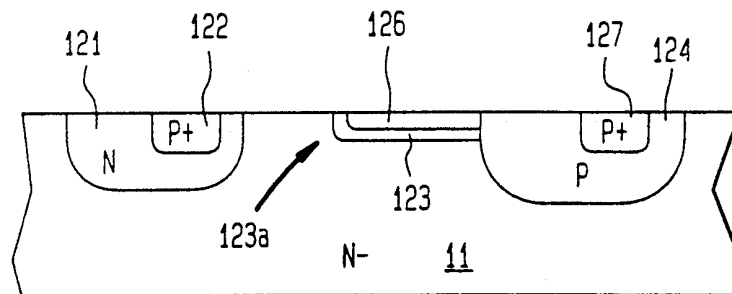


FIG. 8

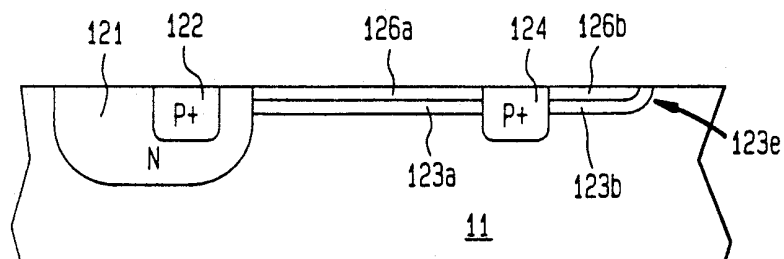


FIG. 9

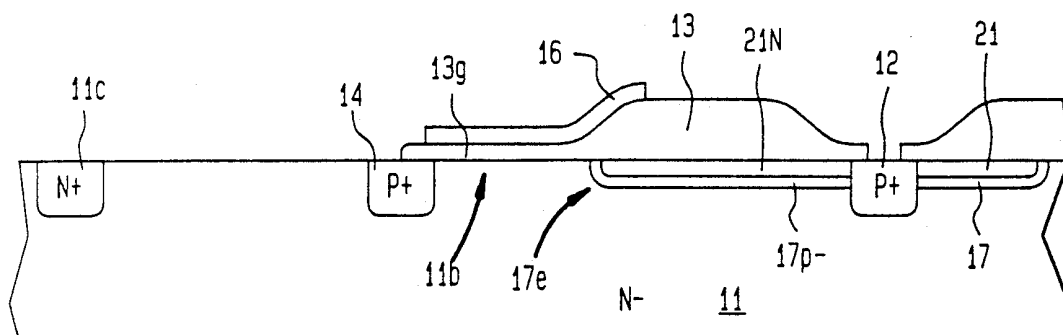
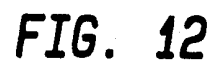
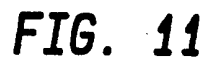


FIG. 10



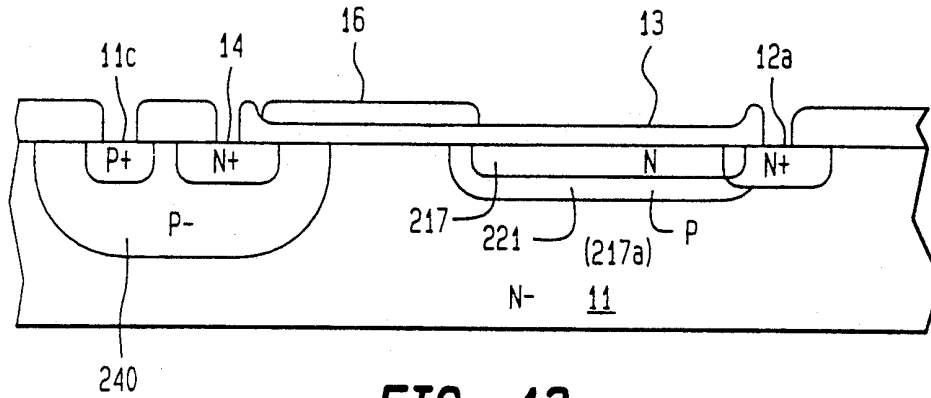


FIG. 13

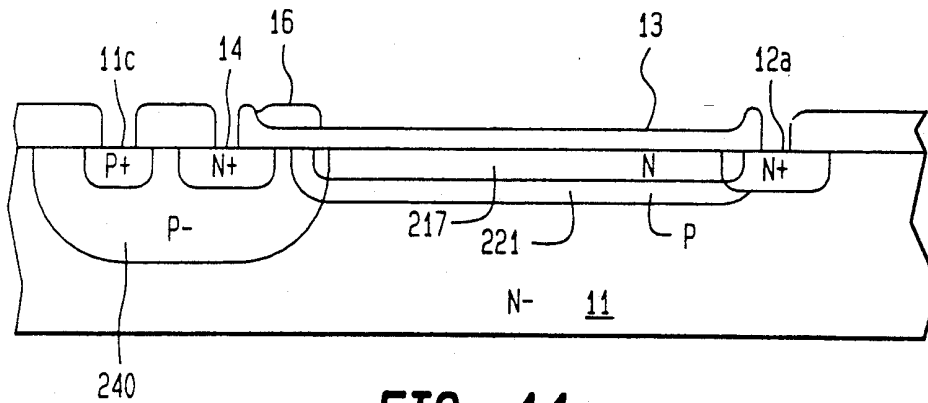


FIG. 14

HIGH VOLTAGE LATERAL SEMICONDUCTOR DEVICE

This is a continuation of application, Ser. No. 242,405, filed Sep. 8, 1988, now abandoned which, in turn, is a continuation-in-part of application, Ser. No. 831,384, filed Jan. 7, 1986, now U.S. Pat. No. 4,823,173, issued Apr. 18, 1989.

FIELD OF THE INVENTION

The present invention relates to lateral semiconductor devices and an improved method of making lateral semiconductor devices. More specifically, the invention relates to high voltage lateral devices with reduced ON resistance and a method of making such devices.

Previous high voltage lateral devices include both MOS devices and bipolar transistors. For example, FIG. 1 illustrates a known structure which can be used as a high voltage lateral MOS device. This device is known as a lateral drift region MOS device and is dependent upon the drain-to-body junction 15 as the basic high voltage junction of the device. The drift region 17 is a P region along the top surface of the N- substrate 11 and is located so as to lie adjacent the P- drain region 12. The drift region 17 is used to connect the high voltage drain 12 to the gate 16 and source 14. The two contacts, drain contact 12a and body contact 11c, are shown for completeness. In the operation of this circuit, the gate 16 and source 14 never assume large voltages relative to the body 11. The drift region 17 serves as a JFET channel with the portion 11a of body region 11 underlying the channel acting as a JFET gate. The JFET channel 17 is designed to totally deplete when the drain 12 is reverse biased to a voltage less than the voltage necessary to reach critical field in the channel-to-body depletion layer. This design preserves the effective high breakdown voltage of drain body junction 15. Also the source 14 and gate 16 (over the gate oxide 13) are safely shielded from the high drain body voltage by the pinched off JFET channel 17.

The resistance of the lateral drift region JFET channel 17 is in series with the resistance of the MOS channel 11b, consequently the total channel resistance of the device is the sum of these two individual resistances. The JFET channel, which must be quite long to sustain high drain body voltages, is often the larger of the two resistance terms. Thus it is desirable to find ways to reduce the resistance of the drift region so that devices of a given size can be made with smaller channel resistance.

FIG. 2 illustrates a known structure which can be used as a high voltage lateral DMOS (LDMOS) device. In this device, an N+ drain contact 12A is formed in the N- substrate 211 and an N+ source 14 and P+ body contact 11c are formed in a P- body region 240. The drift region 217 is an N- region along the top surface of the N- substrate 211 which connects the drain 12 to the gate 16 and source 14. In this high voltage device, the N- drift region 217 must be lightly doped to obtain high body 240 to drain breakdown.

The ON resistance of the LDMOS is approximately the sum of the channel resistance and the bulk resistance in the N- drift region 217. The lateral distance from the N+ drain 12 to the adjacent edge of the MOS channel 11b underlying the gate on the P- body 240 must be large to allow space for the reverse bias depletion layer which spreads from the body-to-drain junction into the

lightly doped drain. This distance, along with the high N- resistivity contribute to the high drift region resistance, which is often much greater than the channel resistance. Thus, it is desirable to reduce the drift region resistance of the LDMOS device.

FIG. 3 shows a known structure which can be used as a lateral bipolar transistor. Another illustration of such a device is contained in FIG. 7 of U.S. Pat. No. 4,283,236 issued Aug. 11, 1981. Referring to FIG. 3, an N- substrate 11, has an N type emitter shield 121 formed therein and P+ emitter 122 and collector 124 formed as shown. Additionally, a P- drift region 123 is provided along the surface of the substrate between the collector 124 and the emitter shield 121. In the operation of this device, the total collector resistance is equal to the sum of the resistance across the drift region 125 plus the resistance of the P+ collector between the drift region and the collector contact. In order to provide devices of equal size having a lower collector resistance, it is desirable to find ways to reduce the resistance of the drift region.

In the operation of this device, the drift region extends the collector to the edge of the emitter shield, 121, so that the base width is just that small distance between the adjacent edges of the emitter, 121, and the drift region, therefore, providing improved frequency response.

At high base-collector voltages, the drift region, 123, depletes by JFET action with the N-base, 11, and N shield, 121, which is part of the base, acting as gate before critical field is reached just as for the MOS of FIG. 1. This preserves the high breakdown of the structure.

SUMMARY OF THE INVENTION

The present invention provides a structure having a reduced channel resistance and a process capable of efficiently obtaining the structure of the invention. The reduction in channel resistance is accomplished by providing a top gate which is located between the lateral drift region of the prior art and the surface of the channel region and which may be in contact with the high voltage device region. This top gate allows the total channel doping to be increased because the top gate to channel depletion layer holds some additional channel charge when reverse biased in addition to that held by the bottom gate to channel depletion layer of the prior art structure. The ionized channel impurity atoms associated with this additional channel charge causes the reduction in channel resistance.

With respect to providing an improved LDMOS structure having a lower drift region resistance, a second drift region which is separated from the original drift region by a region of opposing conductivity is formed. The second drift region provides a conductive path which is in parallel with the original drift region thereby achieving the desired reduction in resistance. Because of the formation of the second drift region, the first enclosed drift region can now have a much higher doping than the second drift region which it replaces, while achieving the same breakdown voltage.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cross section of a known MOS device having typical ON resistance.

FIG. 2 is a cross section of a known LDMOS device having typical ON resistance.

FIG. 3 is a cross section of a known bipolar transistor having typical collector resistance.

FIG. 4 is a cross section of an MOS device including the improved drift region and top gate of the invention.

FIG. 5 illustrates optimized process steps for obtaining the desired shape of the top gate and drift region of the invention.

FIGS. 6a and 6b are, respectively, a top view and a cutaway perspective view of the body contact extending through the top gate and drift region of the invention.

FIG. 7 is a cross section of a bipolar device made in accordance with one aspect of the invention.

FIG. 8 is a cross section of a bipolar device made in accordance with another aspect of the invention.

FIG. 9 is a cross section of a bipolar device made in accordance with a preferred aspect of the invention.

FIG. 10 is a cross section of an MOS device, including the lateral drift region and top gate of the invention, in a preferred embodiment.

FIG. 11 is a cross section of a LDMOS device made in accordance with a preferred embodiment of the invention.

FIG. 12 is a top view of the LDMOS device of FIG. 11.

FIG. 13 is a cross section of a LDMOS device made in accordance with another preferred embodiment of the invention.

FIG. 14 is a cross section of a LDMOS device made in accordance with still another preferred embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

The present invention is described herein with reference to the drawings for both MOS and bipolar applications. FIG. 4 shows an MOS device where P⁺ drain contact 12_a is formed in P⁻ type drain 12, P⁺ source 14 is formed in the N⁻ body 11 and N⁺ body contact 11_c is provided in the N⁺ body 11. The MOS channel region 11_b is in the N⁻ body 11 below the MOS gate 16. The N type top gate 21 is provided along the surface 11_s of the body 11 above the P type drift region 17 which acts as a JFET channel. The lateral edge or peripheral edge of both the top gate 21 and drift region 17 extend to the drain-to-body junction 15 and preferably terminate at the junction 15. It is noted that situations may exist where the doping level in the top gate may be sufficiently high so as to render it desirable to provide a shorter top gate having a lateral extension which stops short of contacting the junction 15. In this case care should be taken to insure that any nondepleted portion of the top gate does not result in a breakdown of the top gate-to-drift region junction 17A. Proper doping of the top gate 21 will generally be a sufficient preventative step. Dashed line 21_p designates the peripheral edge of top gate 21 in an embodiment where the top gate does not extend all the way to the junction 15.

The structure of FIG. 4 provides reduced ON resistance in the JFET channel 17 relative to the prior art lateral drift MOS device as shown in FIG. 1. The reduction in ON resistance is accomplished by providing a structure which can accommodate increased drift region doping without suffering from reduced body-to-drain breakdown. This is possible because of the provision of the top gate 21. The top gate-to-channel depletion layer which holds some channel charge when reverse biased, is in addition to the channel charge held by

the bottom gate to channel depletion layer of the prior art. This additional channel charge, in the form of ionized channel impurity atoms, causes the reduction in channel resistance. It is possible to provide more than twice the doping level previously acceptable due to the additional ability to hold channel charge. Thus, for a drift region 17 having a doping of 1×10^{12} boron atoms per square centimeter in a bottom gate arrangement, the present invention will permit 2×10^{12} boron atoms per square centimeter. Thus, the ON resistance will be only half the ON resistance of the prior arrangement.

In order to optimize performance of the structure of the invention, the top gate 21 must be designed differently than an ordinary JFET gate. Top gate 21 should become totally depleted at a body-to-drain voltage of less than the breakdown voltage of the top gate-to-drain junction 15. Since top gate 21 is connected to body 11 (as shown in FIGS. 6A, 6B to be described below), the voltage at the top gate-to-drain junction 15_a will equal the voltage of the body-to-drain junction 15 voltage and the top gate-to-drain breakdown voltage should be greater than the voltage at which top gate 21 becomes totally depleted. Additionally, the top gate 21 must totally deplete before the body 11 to channel 17 depletion layer reaches the top gate 21 to channel 17 depletion layer to thereby assure that a large top gate 21 to drain 12 voltage is not developed by punch-through action from the body 11. An ordinary JFET gate never totally depletes regardless of operating conditions.

In addition to the above described characteristics of the device of the invention, it is also necessary to insure that the channel of the JFET drift region 17 contacts the inversion layer MOS surface channel. This can be accomplished as shown in FIG. 5 where an implant mask 50 having a tapered edge 51 is provided over the body 11. An implant aperture 52 is provided in mask 50 at the location where the P drift region 17 and N top gate 21 are to be formed. The aperture 52 is shown as exposing the protective oxide 53. Ion implantation is not substantially affected by the oxide 53 due to the oxide thickness of only about 0.1–0.2 micrometers, yet the oxide provides surface passivation for the underlying body 11.

The drift region 17 is ion implanted and, because of the graduated thickness of the implant mask 50 (along the edge 51), the depth of the implanted drift region 17 is graduated or tapered. In the illustration, a fairly good rounding of the drift region 17 occurs at the peripheral edges or extremities 17_a, 17_b of the region 17. The curved extremity 17_a is of interest because at this location the channel of the JFET drift region 17 contacts the surface 11_s of body 11 beyond the end 21_a of top gate 21 and is desirably beneath the gate 16 of the MOS device. The top gate 21 may be ion-implanted using the implant mask 50 but at an energy level which results in a shallower implantation. This tapered profile, particularly if curved, provides improved performance.

In a variation of this method, a diffusion process can be used to bring the JFET channel into contact with the surface of body 11, and hence insure that the JFET channel 17 will contact the inversion layer MOS surface channel (lateral drift region 17 and top gate 21 are diffused after initial introduction by ion implant). The doping levels and diffusion times are chosen such that the extremity 17_a of JFET channel 17 diffuses beyond the end 21_a of the top gate 21 and so that the end 17_a reaches the surface 11_s of body 11. In practice, this approach can be facilitated by choosing a top gate dop-

ant which has a lower diffusion coefficient than that of the drift region dopant.

The formation of the drift region 17 and top gate 21 may be conveniently carried out by forming a mask over the gate oxide which is present in a lateral MOS application. The MOS gate may be utilized as one delineating edge of the implant for the drift region and top gate and a thick oxide portion surrounding a thinner oxide portion may form the remainder of the implant mask. The thinner oxide portion shall be located such that it extends from beneath the MOS gate to the drain and preferably overlaps the drain. The implant mask 50 illustrated in FIG. 5 is shown as having thin oxide portion 53 being surrounded by the implant mask 50. If the MOS gate 16 shown in dashed lines were used as a portion of the mask 50, the edge of the drift region and top gate would be self-aligned with the MOS gate as shown in dashed lines. Then, when diffused, the drift region will extend laterally to a point beneath the MOS gate, while the top gate 21 may be formed such that there is little or no lateral overlap with the MOS gate. The extent of lateral diffusion of the top gate is dependent upon the dopant material and processing temperatures following top gate implant. It is noted that there is a separation between the drift region and the source. This separation zone is the location where the MOS channel is located.

The top gate 21 will perform as previously described if it is tied to the body 11. Thus, the top gate 21 and the body which operates as the bottom gate of the JFET channel will be at equal potential. According to the invention, this may be accomplished in a particularly effective manner if the drift region 17 is widened to overlap with the body contact region 11_c. This is shown in FIG. 6a which shows the overlapping of the top gate 21 and the body contact 11_c at the overlap regions 21_c, 21_d. In order for this arrangement to be effective, it is necessary that the body contact 11_c have a higher dopant concentration than the JFET channel (or drift region) 17, as shown in FIG. 6b to insure that the body contact 11_c forms a continuous region horizontally and/or vertically through the JFET channel and to the body region 11 from the top gate, 21.

FIG. 6b shows a cross section of the structure of FIG. 6a taken along dashed line A—A. The body 11 is provided with body contact 11_c which is located such that the top gate 21 and drift region 17 can be conveniently extended to overlap the body contact 11_c. The depth of body contact 11_c may be made greater than the depth of region 17 such that a portion of the body contact 11_c extends below region 17 and provides contact with the body 11. This arrangement provides a contact portion 21_c where the top gate 21 is in contact with body contact 11_c. Thus, as long as the body contact doping concentration in region 21_b is sufficiently high to overcome the opposite doping in region 17, then a good connection of uniform conductivity type will be provided between the top gate 21 and the body 11, via contact region 11_c. It is also noted that the body contact 11_c extends laterally beyond the end of both of the top gate 21 and the drift region 17. The lateral extension of the contact 11_c will also provide a structure which results in a good connection of uniform conductivity type from the top gate 21 to the body 11, again, provided that the doping of body contact 11_c converts region 21_b.

Another area where the present invention finds application is in lateral bipolar transistors which employ a lateral drift region. The known structure of FIG. 3 may

be improved by providing an N type top gate 126 as shown in FIG. 7. In this arrangement the N type gate 126 extends from the collector 124 to the emitter shield 121 along the surface of body 11. The operation of this device is enhanced by the same phenomenon as the lateral drift region of the previously described MOS device. As the base 11 becomes positive relative to the collector 124, the top gate-to-drift region depletion layer facilitates pinch-off of the drift region 123. However, as the base 11 becomes more negative, the top gate 126 contributes additional surface exposure to the drift region 123 and further enhances carrier transportation.

FIG. 8 shows an improvement over the arrangement shown in FIG. 7. In FIG. 8 the drift region 123 does not extend all the way over to the emitter shield 121. The curved end 123_a of the drift region 123 contacts the top surface of body 11. It is noted that in this arrangement, the emitter shield 121 may be omitted.

An additional improvement shown in FIG. 8 is the use of a deep diffusion to form the collector 124 resulting in a significantly increased breakdown voltage. The deep diffusion step may be the same step used for forming the emitter, in which case the collector 124 shown in FIG. 7 would be deeper, or a separate collector implant and diffusion step may be employed and the collector contact 127 may then be formed simultaneously with the formation of the emitter 122. This improvement in junction breakdown voltage is equally obtainable, for example, at the body to drain junction in the MOS devices described previously.

A further extension of the invention which may be used to increase base-to-collector breakdown voltage for a PNP device is shown in FIG. 9. In addition to the provision of the N type top gate 126_a over the P- drift region 123_a, the top gate 126_a and drift region 123_a are enlarged to surround the collector 124 and a curved edge 123_b is provided at the periphery of the enlarged portion 123_b of the drift region 123_a. This enlarged portion is designated by reference numerals 123_b for the drift region and 126_b for the top gate. The collector 124 to base 11 breakdown voltage is increased relative to alternative arrangements because of mitigation of the breakdown reduction due to the junction curvature. The top gate 126_a extends to the emitter shield 121 as does the drift region 123_a. The P+ emitter 122 is formed in the N+ type emitter shield 121.

FIG. 10 illustrates an extension of the invention with respect to a P channel MOS device similar to the improvement described with respect to the bipolar device shown in FIG. 9. For the MOS device, the drain 12 is surrounded by the P- drift region 17 and N type top gate 21. Around the entire periphery of the drift region 17 there is a curved portion 17_e which rounds up to the surface of the N- substrate 11 to insure that the JFET channel in the drift region 17 contacts the MOS channel 11_b under the MOS gate 16. The drift region 17 extends outward from the entire perimeter of the drain 12. This arrangement mitigates the breakdown reduction due to junction curvature. The P+ source 14 and N+ body contact 11_c are shown as is the dielectric 13 which serves as the gate oxide 13_g beneath the MOS gate 16.

In both the arrangements shown in FIG. 9 and FIG. 10, the planar diode breakdown improvement created by the drift region acting as a surface layer of the same conductivity type as the collector in FIG. 9 and drain in FIG. 10 and extending out from the perimeter of the collector and drain can be implemented by a single series of process steps. According to the invention, a

common set of process steps produces both a suitable breakdown improvement layer and an improved drift region. The breakdown improvement layer is a two layer component.

A further extension of the invention is illustrated in FIG. 11 which shows an LDMOS device where N⁺ drain contact 12_a is formed in an N⁻ type substrate and an N⁺ source 14 and P⁺ body contact 11_a are formed in a P⁻ type body region 240. The DMOS channel region 11_b is in the P⁻ body 240 below the DMOS gate 16. The N type first drift region 217 is provided along the surface 11_c of the substrate 11 above a P⁻ type separation region 250. A second drift region 217_a exists in the substrate 11 underneath the P⁻ type separation region. The lateral edge of both the first drift region 217 and the separation region 250 extend from the gate 16 to the N⁺ drain contact 12_a.

The structure in FIG. 11 provides reduced ON resistance by way of the second (surface) drift region 217_a relative to the (deeper) prior art lateral first drift region 217_a device, refer to above in FIG. 2. To illustrate this, consider an example in which the N⁻ region 11 has a doping of 1×10^{14} ions cm⁻³. The top gate layer 217 has an integrated doping of about 1×10^{12} ions cm⁻² and is preferably not more than two microns thick while maintaining full breakdown. The thickness of the N and P layers 217, 250 together is preferably less than ten microns and can be less than one micron. The same integrated doping in the N⁻ body 11 requires a thickness of 100 microns. Thus, the N and P layers 217, 250 respectively consume only a small fraction of the N⁻ thickness required to provide doping equal to that portion of the N layer of the prior art device.

The lateral spacing between the drain contact 12_a and the channel 11_b in the device described above would be approximately 30 microns. In such a device, even if a full 100 micron thick N⁻ body 11 were provided, it would have a higher resistance than the N⁻ first drift region 217 provided according to the invention. This is because the average path length of current flowing from the drain contact 12A down through the thick N⁻ body 11 and back up to the surface edge of the channel at the drain-to-body junction would be greater than the direct path through the N⁻ first drift region.

Maximum breakdown is achieved in the invention by providing doping densities of the N and P layers 217, 250 such that they become totally depleted before breakdown is reached at any point along the junctions which they form with adjoining regions and before breakdown is reached at the junction between them. To insure that this occurs, the N region 217 should have an integrated doping not exceeding approximately 1×10^{12} ions cm⁻² and the P region 250 should have a higher integrated doping not exceeding about 1.5 to 2×10^{12} ions cm⁻².

To insure proper depletion of the P and N regions 250, 217, they must have the proper voltages applied. The N layer bias is achieved by connecting the N first drift region 217 to the higher concentration N⁺ drain contact 12_a by overlapping the N first drift region 217 and drain contact 12_a. The P region 250 bias is achieved by overlapping the P region 250 with the P⁻ body 240 at least at one end of the channel, thereby applying the body voltage to the P layer 250. This is illustrated in FIG. 12.

With this structure and choice of doping levels, the desired results are achieved. When a reverse bias voltage is applied to the drain-to-body junction 15, the same

reverse bias appears on both the PN⁻ junction 260 and the PN junction 270. Depletion layers spread up into the N first drift region 217 and down into the N⁻ body 11 from the P layer 250. In a preferred embodiment, the P and N first drift region dopings are chosen such that the N layer 217 becomes totally depleted at a lower voltage than that at which the P layer 250 becomes totally depleted. This insures that no residual undepleted portion of the N layer 217 is present which could reduce breakdown voltage.

As a result of the invention, the improved DMOS device provides a reduced resistance current path in the drain which does not depend on the N⁻ doping. This allows the N⁻ doping to be reduced to achieve a desired breakdown voltage with good manufacturing margin, while maintaining desirable low drift region resistance. In a multi-device process which includes LDMOS devices, the N⁻ region can be adjusted to achieve the desired characteristics of one or more of the other device types, while the N first drift region 217 sets the drift region 217 resistance of the LDMOS.

Another embodiment of the DMOS invention is illustrated in FIG. 13, where the N and P regions 217, 221 are self-aligned to the gate 16 by using the gate 16 as a mask. An advantage of this structure is that N and P regions can be defined by the uncovered thin oxide area which extends from gate edge to overlap the drain contact. This embodiment requires no explicit mask step to delineate the location where the N and P regions are formed.

Still another embodiment, as illustrated in FIG. 14, provides no gap between the P⁻ body 240 and the P region 221 adjacent to the channel edge. The absence of the gap prevents current from flowing in the N⁻ body 11; so the entire drift region current path is in the N first drift region 217. Elimination of the gap also allows the device structure to be made smaller. As with the other structure, the N and P regions may be self-aligned to the gate edge, as illustrated in FIG. 14, or not self-aligned. They may also be covered by thick or thin oxide as a design option.

A preferred feature of the present invention provides that the body or substrate regions 11 shown in the FIGS. 3, 4, 6, 7, 8, 9, 11, 13 and 14 are designed to be dielectrically or self-isolated regions. In contrast with the typical RESERF type of devices in which the bottom isolation junction plays a central role in the action of the device, the present invention contemplates that the isolation junction does not contribute to the depletion of the drift or top gate regions which are taught to be totally depleted. Prior art RESERF devices such as that described in U.S. Pat. No. 4,300,150 to Colak always require the substrate to be part of such depletion whereby the substrate must assume the most negative voltage in the device because of its role as one side of the isolation junction. As a result of this bias on the substrate or body region, the prior art RESERF type devices are susceptible to punch through from the device region through the epitaxial layer to the substrate. As a result of the present invention not having the substrate as part of the depletion mechanism, the invention can more effectively provide high voltage protection while not increasing the resistance of the channel path. Although the figures illustrate a nonisolating structure or self-isolated structure, it is understood that the invention applies equally well to dielectrically or junction isolated substrates.

While the present invention has been described with respect to several preferred manners of implementing the invention, it is to be understood that the claims appended hereto are intended to cover the invention in its broadest sense and are not to be limited to the specific implementations disclosed.

What is claimed is:

1. A semiconductor device comprising:

- a semiconductor body of a first conductivity type having a first surface;
- a first semiconductor region of a second conductivity type formed in a first portion of said first surface of said semiconductor body, and defining a first PN junction with said semiconductor body;
- a second semiconductor region of said first conductivity type formed in a surface portion of said first semiconductor region and defining therewith a second PN junction, said second PN junction being spaced apart from said first PN junction by material of said first semiconductor region therebetween;
- a third semiconductor region of said first conductivity type formed in a second surface portion of said semiconductor body, spaced apart from said first surface portion by a third surface portion thereof;
- a fourth semiconductor region of said second conductivity type formed in a first surface part of said third surface portion of said semiconductor body spaced apart from said first surface portion of said semiconductor body by a second surface part of said third surface portion thereof and defining with said semiconductor body a third PN junction, said fourth semiconductor region being connected to said first semiconductor region and being contiguous with said third semiconductor region;
- a fifth semiconductor region of said first conductivity type, and having an impurity concentration greater than that of said semiconductor body, formed in said fourth semiconductor region and defining therewith a fourth PN junction, said fifth semiconductor region being contiguous with said third semiconductor region;
- an insulator layer formed on said first surface of said semiconductor body; and
- a gate electrode formed on said insulator layer so as to overlie said second surface part of said third surface portion of said semiconductor body and material of said first and fourth semiconductor regions, that portion of said first semiconductor region lying beneath said gate electrode serving as a channel region of said device, said gate electrode having a gate voltage applied to induce a conductive channel through said first semiconductor region therebeneath; and wherein
- when said device is reverse-biased, a first depletion region extends from said fourth PN junction into said fourth semiconductor region and said semiconductor body, and a second depletion region extends from said fifth PN junction into said fifth semiconductor region and said fourth semiconductor region;
- said semiconductor body having a first ON resistance in a first current flow path therethrough between said second and third semiconductor regions, and said fifth semiconductor region providing a second ON resistance in a second current flow path along the surface of said semiconductor body from said second semiconductor region through said channel

and said fourth and fifth semiconductor regions to said third semiconductor region, so that said fifth semiconductor region serves to provide a current flow path in parallel with said first current flow path, thereby effectively reducing the total ON resistance of the overall current flow path between said second and third semiconductor regions.

2. A semiconductor device according to claim 1, wherein a peripheral edge of said gate electrode is aligned with a peripheral edge of said fifth semiconductor region.

3. A semiconductor device according to claim 1, wherein said fourth semiconductor region overlaps said first semiconductor region.

4. A semiconductor device according to claim 1, wherein the impurity concentration said fifth semiconductor region is such that said fifth semiconductor region is completely depleted by said second depletion region at a reverse bias less than that at which said first and second depletion regions come together within and punch through said fourth semiconductor region.

5. A semiconductor device comprising:

- a semiconductor body of a first conductivity type having a first surface;
- a first semiconductor region of a second conductivity type formed in a first portion of said first surface of said semiconductor body, and defining a first PN junction with said semiconductor body;
- a second semiconductor region of said first conductivity type formed in a surface portion of said first semiconductor region and defining therewith a second PN junction, said second PN junction being spaced apart from said first PN junction by material of said first semiconductor region therebetween;
- a third semiconductor region of said first conductivity type formed in a second surface portion of said semiconductor body, spaced apart from said first surface portion by a third surface portion thereof;
- a fourth semiconductor region of said second conductivity type formed in said third surface portion of said semiconductor body and defining with said semiconductor body a third PN junction, said fourth semiconductor region being connected to said first semiconductor region and being contiguous with said first and third semiconductor regions;
- a fifth semiconductor region of said first conductivity type, and having an impurity concentration greater than that of said semiconductor body, formed in said fourth semiconductor region and defining therewith a fourth PN junction, said fifth semiconductor region being contiguous with said first and third semiconductor regions;
- an insulator layer formed on said first surface of said semiconductor body; and
- a gate electrode formed on said insulator layer so as to overlie material of said first and fourth semiconductor regions, that portion of said first semiconductor region lying beneath said gate electrode serving as a channel region of said device, said gate electrode having a gate voltage applied to induce a conductive channel through said first semiconductor region therebeneath; and wherein
- when said device is reverse-biased, a first depletion region extends from said fourth PN junction into said fourth semiconductor region and said semiconductor body, and a second depletion region extends from said fifth PN junction into said fifth semiconductor

5,264,719

11

ductor region and said fourth semiconductor region.

6. A semiconductor device according to claim 5, wherein the impurity concentration said fifth semiconductor region is such that said fifth semiconductor region is completely depleted by said second depletion region at a reverse bias less than that at which said first and second depletion regions come together within and punch through said fourth semiconductor region.

7. A semiconductor device comprising:
a semiconductor body of a first conductivity type having a first surface;
a first semiconductor region of a second conductivity type formed in a first portion of said first surface of said semiconductor body, and defining a first PN junction with said semiconductor body;
a second semiconductor region of said second conductivity type formed in a second surface portion of said semiconductor body, spaced apart from said first surface portion by a third surface portion thereof and defining a second PN junction with said semiconductor body;
a third semiconductor region of said second conductivity type formed in a first surface part of said third surface portion of said semiconductor body spaced apart from said first surface portion of said semiconductor body by a second surface part of said third surface portion thereof and defining with said semiconductor body a third PN junction, said third semiconductor region being contiguous with said second semiconductor region;
a fourth semiconductor region of said first conductivity type, and having an impurity concentration greater than that of said semiconductor body, formed in said third semiconductor region and defining therewith a fourth PN junction;
an insulating layer formed on said first surface of said semiconductor body; and
a gate electrode formed on said insulator layer so as to overlie said second surface part of said third surface portion of said semiconductor body, that portion of said semiconductor body lying beneath said gate electrode serving as a channel region of said device, said gate electrode being applied with a gate voltage for inducing a conductive channel through said channel region;

said device being reverse-biased, so that a first depletion region extends from said third PN junction into said third semiconductor region and said semiconductor body and a second depletion region extends from said fourth PN junction into said third semiconductor region and said fourth semiconductor region;

said semiconductor body having a first ON resistance in a first current flow path therethrough between said first and second semiconductor regions, and said fourth semiconductor region providing a second ON resistance, less than said first ON resistance, in a second current flow path along the surface of said semiconductor body from said first semiconductor region through said channel and said third and fourth semiconductor regions to said second semiconductor region, so that said fourth semiconductor region serves to provide a reduced resistance current flow path in parallel with said first current flow path, thereby effectively reducing the total ON resistance of the overall current

12

flow path between said first and second semiconductor regions; and

wherein the impurity concentration said fourth semiconductor region is such that said fourth semiconductor is completely depleted by said second depletion region at a reverse bias less than that at which said first and second depletion regions come together within and punch through said third semiconductor region.

8. A high voltage MOS transistor comprising:
a semiconductor substrate of a first conductivity type having a surface,
a pair of laterally spaced source and drain pockets of semiconductor material of a second conductivity type within the substrate and adjoining the substrate surface,
an extended drain region of the second conductivity type extending laterally each way from said drain pocket to surface-adjoining positions,
a surface adjoining, top layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain pocket and the surface-adjoining positions,
said top layer of material and said substrate being subject to application of a reverse-bias voltage,
an insulating layer on the surface of the substrate and covering at least that portion between the source pocket and the nearest surface-adjoining position of the extended drain region, and
a gate electrode on the insulating layer and electrically isolated from the substrate region thereunder which forms a channel laterally between the source pocket and the nearest surface-adjoining position of the extended drain region, said gate electrode controlling by field-effect the flow of current thereunder through the channel.

9. A high voltage MOS transistor according to claim 8, wherein said extended drain region has an impurity concentration greater than $1 \times 10^{12} \text{ cm}^{-2}$.

10. A high voltage MOS transistor according to claim 8, further including an ohmic contact region of said first conductivity type formed in a surface adjoining portion of said semiconductor substrate, said ohmic contact region overlapping said top layer of material.

11. A high voltage MOS transistor comprising:
semiconductor material of a first conductivity type having a surface,
a pair of laterally spaced source and drain pockets of semiconductor material of a second conductivity type within the substrate and adjoining the surface of said semiconductor material,
an extended drain region of the second conductivity type extending laterally from said drain pocket to a surface-adjoining position,
a surface adjoining top layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain pocket and said surface-adjoining position,
said top layer of material and said semiconductor material being subject to application of a reverse-bias voltage,
an insulating layer on the surface of said semiconductor material and covering at least that portion between the source pocket and the nearest surface-adjoining position of the extended drain region, and
a gate electrode on the insulating layer and electrically isolated from a semiconductor material re-

gion thereunder containing a channel that extends laterally between the source pocket and the nearest surface-adjointing position of the extended drain region, said gate electrode controlling by field-effect the flow of current thereunder through the channel.

12. A high voltage MOS transistor according to claim 11, wherein said extended drain region extends in a plurality of different directions from said drain pocket to respective plural surface adjoining positions.

13. A high voltage MOS transistor according to claim 11, wherein said extended drain region surrounds said drain pocket and extends to a surrounding surface adjoining position.

14. A high voltage MOS transistor according to claim 11, wherein said drain pocket comprises a first relatively deep pocket of a first impurity concentration and a second relatively shallow pocket formed in a surface portion of said first relatively deep pocket and having a second impurity concentration greater than said first impurity concentration and providing a drain contact region.

15. A high voltage MOS transistor according to claim 11, wherein said extended drain region has an impurity concentration greater than $1 \times 10^{12} \text{ cm}^{-2}$.

16. A high voltage MOS transistor according to claim 11, further including an ohmic contact region of said first conductivity type formed in a surface adjoining portion of said semiconductor material, said ohmic contact region overlapping said top layer of material.

17. A high voltage field effect transistor device comprising:
 semiconductor material of a first conductivity type having a surface;
 a source region of a second conductivity type formed in a first surface portion of said semiconductor material;
 a drain region of said second conductivity type formed in a second surface portion of said semiconductor material spaced apart from said first surface portion by a third surface portion therebetween;
 an extended drain region of said second conductivity type extending from said drain region beneath a first portion of said third surface portion of said semiconductor material, to adjoin a second portion of said third surface portion of said semiconductor material, spaced apart from said said second surface portion of said semiconductor material, by said first portion of said third surface portion of said semiconductor material;
 a surface region of said first conductivity type formed in said first portion of said third surface portion of said semiconductor material;
 an insulating layer disposed on said surface of said semiconductor material, so as to overlie a third portion of said third surface portion of said semiconductor material between the second portion of said third surface portion of said semiconductor material and said first surface portion of said semiconductor material; and
 a gate electrode disposed on that portion of said insulating layer overlying said third portion of said third surface portion of said semiconductor material, and wherein said surface region and said semiconductor material are subject to the application of a reverse bias voltage.

18. A high voltage field effect transistor device according to claim 17, wherein said extended drain region

extends laterally in a plurality of different directions from said drain region to adjoin said second portion of said third surface portion of said semiconductor material and to adjoin a fifth surface portion of said semiconductor material.

19. A high voltage field effect transistor device according to claim 17, wherein said extended drain region surrounds said drain region and extends to a surrounding surface-adjointing portion of said semiconductor material.

20. A high voltage field effect transistor device according to claim 17, wherein said drain region comprises a first relatively deep region of a first impurity concentration and a second relatively shallow region formed in a surface portion of said first relatively deep region and having a second impurity concentration greater than said first impurity concentration and providing a drain contact region.

21. A high voltage field effect transistor device according to claim 17, wherein said extended drain region has an impurity concentration greater than $1 \times 10^{12} \text{ cm}^{-2}$.

22. A high voltage field effect transistor device according to claim 17, further including an ohmic contact region of said first conductivity type formed in a surface adjoining portion of said semiconductor material, said ohmic contact region overlapping said surface region.

23. An integrated MOS/JFET transistor device comprising an insulated gate field effect transistor and a double-sided junction field effect transistor integrated together in semiconductor substrate which contains a source region, and a drain region, and a dual channel path formed in said semiconductor material between said source and drain regions, said dual channel path comprising an insulated gate-controlled channel region having a first conductivity type in the presence of a channel-inducing gate voltage, said insulated gate-controlled channel region being contiguous with a double-sided junction channel region of said first conductivity type, and wherein said source region adjoins said insulated gate-controlled channel region and said drain region adjoins said double-sided channel region.

24. An integrated MOS/JFET transistor device according to claim 23, wherein said insulated gate-controlled channel region comprises a surface portion of said semiconductor material adjoining said source region, and wherein said double-sided junction channel region comprises an extended drain region extending laterally from said drain region beneath a top gate region to said surface portion of said semiconductor material, an underlying portion of said semiconductor material extending beneath and adjoining said extended drain region and forming a bottom gate, said top gate region and said bottom gate forming respective PN junctions with said double-sided junction channel region.

25. An integrated MOS/JFET transistor device according to claim 23, wherein said extended drain region and said double-sided junction channel region surround said drain region and extend to a surrounding surface-adjointing position.

26. An integrated MOS/JFET transistor device according to claim 23, wherein said extended drain region and said double, wherein said drain region comprises a first relatively deep region of a first impurity concentration and a second relatively shallow region formed in a surface portion of said first relatively deep region and having a second impurity concentration greater than

5,264,719

15

said first impurity concentration and providing a drain contact region.

27. An integrated MOS/JFET transistor device according to claim 23, wherein said extended drain region and said double, further including an ohmic contact region of said first conductivity type formed in a surface adjoining portion of said semiconductor material, said ohmic contact region overlapping said top gate.

28. An integrated MOS/JFET transistor device according to claim 23, wherein said extended drain region has an impurity concentration greater than $1 \times 10^{12} \text{ cm}^{-2}$.

29. A high voltage MOS transistor comprising: semiconductor material of a first conductivity type having a surface;

source and drain regions of a second conductivity type adjoining spaced apart portions of the surface of said semiconductor material;

an extended drain region of said second conductivity type extending laterally from said drain region through said semiconductor material to a surface-adjoining portion of the surface of said semiconductor material;

a top gate semiconductor layer of said first conductivity type adjoining said drain region and adjoining said extended drain region along the surface of said semiconductor material to said surface-adjoining portion of the surface of said semiconductor material, said top gate semiconductor layer and said semiconductor material being subject to the application of a reverse-bias voltage;

an insulating layer on the surface of the semiconductor material and covering at least that portion of the surface of said semiconductor material between said source region and said surface-adjoining portion of said extended drain region; and

a gate electrode disposed on said insulating layer and being electrically isolated from that portion of the surface of said semiconductor material thereunder which forms a channel laterally between said source region and said surface-adjoining portion of said extended drain region, said gate electrode controlling, by field-effect, the flow of current thereunder through said channel.

30. A high voltage MOS transistor according to claim 29, wherein said extended drain region extends laterally each way from said drain region to surface-adjoining portions of the surface of said semiconductor material, and wherein said top gate semiconductor layer extends laterally in a plurality of different directions from said drain region and adjoins said extended drain region along the surface of said semiconductor material to said surface-adjoining portions of the surface of said semiconductor material.

31. A high voltage MOS transistor according to claim 29, wherein said extended drain region surrounds said drain region and extends to a surrounding surface adjoining position.

32. A high voltage MOS transistor according to claim 29, wherein said drain region comprises a first relatively deep region of a first impurity concentration and a second relatively shallow region formed in a surface portion of said first relatively deep region and having a second impurity concentration greater than said first impurity concentration and providing a drain contact region.

33. A high voltage MOS transistor according to claim 29, wherein said extended drain region has an impurity concentration greater than $1 \times 10^{12} \text{ cm}^{-2}$.

34. A high voltage MOS transistor according to claim 29, further including an ohmic contact region of said

16

first conductivity type formed in a surface adjoining portion of said semiconductor material, said ohmic contact region overlapping said top gate layer.

35. A high voltage diode comprising:

semiconductor material of a first conductivity type having a surface,

a first, surface-adjoining region of a second conductivity type;

a second surface-adjoining region of said first conductivity type spaced apart from said first, surface-adjoining region;

a third region of said second conductivity type extending laterally from said first, surface-adjoining region; and

a fourth, surface-adjoining region of said first conductivity type overlying an intermediate portion of said third, laterally extending and surface-adjoining region.

36. A high voltage diode according to claim 35, wherein said third region surrounds said first, surface-adjoining region and extends to a surrounding surface adjoining position.

37. A high voltage diode according to claim 35, wherein said first region comprises a first relatively deep region of a first impurity concentration and a second relatively shallow region formed in a surface portion of said first relatively deep region and having a second impurity concentration greater than said first impurity concentration.

38. A high voltage diode according to claim 35, wherein said third region has an impurity concentration greater than $1 \times 10^{12} \text{ cm}^{-2}$.

39. A lateral bipolar transistor having a high voltage base-collector diode comprising:

semiconductor material of a first conductivity type having a surface and forming a base of said bipolar transistor,

a first, surface-adjoining collector region of a second conductivity type forming a base-collector junction with said semiconductor material;

a second surface-adjoining base region of said first conductivity type spaced apart from said first, surface-adjoining collector region;

a third, extended collector region of said second conductivity type extending laterally from said first, surface-adjoining collector region, so that said base-collector junction extends laterally from said first, surface adjoining collector region;

a fourth, surface-adjoining region of said first conductivity type overlying an intermediate portion of said third, laterally extending and surface-adjoining extended collector region; and

a fifth, surface-adjoining emitter region of said second conductivity type formed in said second surface-adjoining base region and defining therewith an emitter-base junction.

40. A lateral bipolar transistor according to claim 39, wherein said third region surrounds said first, surface-adjoining region and extends to a surrounding surface adjoining position.

41. A lateral bipolar transistor according to claim 39, wherein said first region comprises a first relatively deep region of a first impurity concentration and a second relatively shallow region formed in a surface portion of said first relatively deep region and having a second impurity concentration greater than said first impurity concentration.

42. A lateral bipolar transistor according to claim 39, wherein said third, extended collector region has an impurity concentration greater than $1 \times 10^{12} \text{ cm}^{-2}$.

* * * * *

Substitute Form PTO-1595

9-77-96
RECORDATION FORM COVER SHEET
PATENTS ONLY

09-30-1999

Assistant Commissioner for Patents: Please record the attached original document



1. Name of conveying party(ies):
Harris Corporation

2. Name and address of receiving party(ies):
Intersil Corporation
2401 Palm Bay Road, N.E.
Palm Bay, FL 32905

101158628

Additional name(s) attached? ☐ Yes ☒ NoAdditional names/addresses attached? ☐ Yes ☒ No

3. Nature of conveyance:

- ☒ Assignment
☐ Merger
☐ Security Agreement
☐ Change of Name
☐ Other:

CEIVE

EP 27 1999

Execution Date: **August 13, 1999**

4. Application number(s) or patent number(s):

If this document is being filed with a new application, the execution date of the application is:

A. Patent Application No.(s):

B. Patent No.(s):

Additional numbers attached? ☒ Yes ☐ No

4236231

5. Name/address of party to whom correspondence concerning document should be mailed:

Timothy A. French
Fish & Richardson P.C.
225 Franklin Street
Boston, MA 02110-2804

6. Total number of applications/patents involved: **806**7. Total fee (37 CFR 3.41): **\$32,240.00**

- ☒ Enclosed
☐ Authorized to charge deposit account

8. Deposit account number: **06-1050**

If the fee above is being charged to deposit account, a duplicate copy of this cover sheet is attached. Please apply any additional charges, or any credits, to our Deposit Account No. 06-1050.

09/29/1999 JSWDAZZ 00000025 4236231

DO NOT USE THIS SPACE

01 FC:581

32240.00 DP

9. Statement and signature: *To the best of my knowledge and belief, the foregoing information is true and correct and the attached is the original document.***Timothy A. French**

Name of Person Signing

Signature

Date

Total number of pages including cover sheet, attachments, and document: **1**Date of Deposit Sept 21 1999

I hereby certify under 37 CFR 1.8(a) that this correspondence is being deposited with the United States Postal Service as **first class mail** with sufficient postage on the date indicated above and is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

PATENT**REEL: 010247 FRAME: 0043**

HARRIS PATENT ASSIGNMENT

FOR VALUE RECEIVED, the receipt and sufficiency of which is hereby acknowledged, the undersigned Harris Corporation, a corporation of Delaware having a place of business at 1025 West NASA Blvd., Melbourne, Florida 32919 ("Harris"), does hereby assign, transfer and set over to Intersil Corporation, a corporation of Delaware having a place of business at 2401 Palm Bay Road, N.E., Melbourne, Florida 32905, its successors, legal representatives and assigns (hereinafter "Assignee") the entire right, title and interest in and to each of the United States patents and patent applications listed in the attached Appendix A, together with the inventions disclosed and/or claimed therein, as well as all applications for patent and any Letters Patent which may be granted therefor, in the United States of America and in all foreign countries, and in and to any and all divisions, continuations, continuations-in-part of said applications, or re-issues or extensions of said patents or Letters Patent, and all rights under the International Convention for the Protection of Industrial Property and similar agreements (hereinafter individually and collectively "Patents").

Harris hereby appoints Assignee as its agent and attorney-in-fact to conduct all business before the United States Patent & Trademark Office and the patent offices in all foreign countries in the name of Harris in connection with said Patents.

Harris hereby authorizes and requests that the United States Patent & Trademark Office, and the patent offices of all foreign countries, to issue any and all Letters Patent of the United States and patents in all foreign countries resulting from said application or any division or divisions or continuing applications thereof in the United States and all foreign countries to Assignee, as assignee of the entire interest, and Harris hereby covenants that it has full right to convey the entire interest herein assigned, and that it has not executed and will not execute, any agreement in conflict herewith.

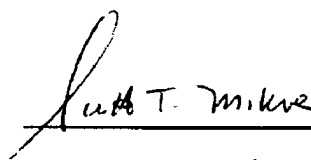
Harris further agrees to cooperate with the Assignee in every way possible and to do all affirmative acts, and to execute all papers which counsel for Assignee shall advise are necessary and/or desirable without charge to Assignee in connection with said Patents including, without limitation, the execution of separate assignments for filing in the United States Patent & Trademark Office and the patent offices of all foreign countries in connection with said Patents.

The undersigned Harris hereby grants to Howard Rothman; John DeAngelis, Reg. No. 30,622; Ferdinand M. Romano, Reg. No. 32,752; and L. Lawton Rogers, III, Reg. No. 24,302 the power to insert on this assignment any further identification which may be necessary or desirable in order to comply with the rules of the United States Patent Office for recordation of this document.

IN WITNESS WHEREOF,

Date August 13, 1999

HARRIS CORPORATION

By:  (Signature)
Scott T. Mikuen (Printed Name)
Assistant Secretary (Title)

ATTEST:

[SEAL]


Secretary

Date August 13, 1999

APPENDIX A

HARRIS CORPORATION

ISSUED PATENTS

Patent Number	Issue Date
4236231	25-Nov-1980
4260431	07-Apr-1981
4272833	09-Jun-1981
4281449	04-Aug-1981
4283236	11-Aug-1981
4288911	15-Sep-1981
4290831	22-Sep-1981
4292730	06-Oct-1981
4299024	10-Nov-1981
4301383	17-Nov-1981
4305106	08-Dec-1981
4309813	12-Jan-1982
4312046	19-Jan-1982
4319257	09-Mar-1982
4334646	15-Jun-1982
4368395	11-Jan-1983
4380710	19-Apr-1983
4389721	21-Jun-1983
4398142	09-Aug-1983
4401940	30-Aug-1983
4402002	30-Aug-1983
4402065	30-Aug-1983
4403399	13-Sep-1983
4409686	11-Oct-1983
4420766	13-Dec-1983
4446444	01-May-1984
4450414	22-May-1984
4454432	12-Jun-1984
4456918	26-Jun-1984
4461000	17-Jul-1984
4462020	24-Jul-1984
4464631	07-Aug-1984
4464825	14-Aug-1984
4466179	21-Aug-1984
4468414	28-Aug-1984
4471236	11-Sep-1984
4471376	11-Sep-1984
4472648	18-Sep-1984
4480219	30-Oct-1984
4495537	22-Jan-1985
4495694	29-Jan-1985
4503387	05-Mar-1985
4514802	30-Apr-1985
4524246	18-Jun-1985
4528461	09-Jul-1985
4528462	09-Jul-1985
4528504	09-Jul-1985
4532003	30-Jul-1985
4532481	30-Jul-1985
4536231	20-Aug-1985
4546539	15-Oct-1985
4554059	19-Nov-1985
4559608	17-Dec-1985

Patent Number	Issue Date
4560948	24-Dec-1985
4566796	28-Jan-1986
4567385	28-Jan-1986
4567578	28-Jan-1986
4578859	01-Apr-1986
4580131	01-Apr-1986
4581548	08-Apr-1986
4584660	22-Apr-1986
4586193	29-Apr-1986
4590664	27-May-1986
4591826	27-May-1986
4594265	10-Jun-1986
4595608	17-Jun-1986
4596068	24-Jun-1986
4599789	15-Jul-1986
4606936	19-Aug-1986
4608530	26-Aug-1986
4613772	23-Sep-1986
4616178	07-Oct-1986
4618743	21-Oct-1986
4620179	28-Oct-1986
4624749	25-Nov-1986
4631636	23-Dec-1986
4632557	30-Dec-1986
4633107	30-Dec-1986
4636743	13-Jan-1987
4636744	13-Jan-1987
4639684	27-Jan-1987
4639896	27-Jan-1987
4644191	17-Feb-1987
4644192	17-Feb-1987
4644383	17-Feb-1987
4650696	17-Mar-1987
4652895	24-Mar-1987
4658253	14-Apr-1987
4665327	12-May-1987
4665425	12-May-1987
4666737	19-May-1987
4669884	02-Jun-1987
4670769	02-Jun-1987
4675798	23-Jun-1987
4677321	30-Jun-1987
4682057	21-Jul-1987
4682059	21-Jul-1987
4683485	28-Jul-1987
4684055	04-Aug-1987
4686384	11-Aug-1987
4694313	15-Sep-1987
4698589	06-Oct-1987
4701644	20-Oct-1987
4702000	27-Oct-1987
4702967	27-Oct-1987
4703505	27-Oct-1987
4703566	03-Nov-1987
4705596	10-Nov-1987
4705597	10-Nov-1987
4708747	24-Nov-1987
4713260	15-Dec-1987

58

Patent Number	Issue Date
4713681	15-Dec-1987
4716071	29-Dec-1987
4717680	05-Jan-1988
4717847	05-Jan-1988
4719598	12-Jan-1988
4720739	19-Jan-1988
4728820	01-Mar-1988
4729008	01-Mar-1988
4733168	22-Mar-1988
4734885	29-Mar-1988
4734886	29-Mar-1988
4752591	21-Jun-1988
4753851	28-Jun-1988
4754388	28-Jun-1988
4755770	05-Jul-1988
4757363	12-Jul-1988
4757528	12-Jul-1988
4760433	26-Jul-1988
4761570	02-Aug-1988
4771016	13-Sep-1988
4780688	25-Oct-1988
4781853	01-Nov-1988
4783637	08-Nov-1988
4786608	22-Nov-1988
4789426	06-Dec-1988
4795718	03-Jan-1989
4801065	31-Jan-1989
4804865	14-Feb-1989
4807012	21-Feb-1989
4808547	28-Feb-1989
4812962	14-Mar-1989
4814285	21-Mar-1989
4818725	04-Apr-1989
4818901	04-Apr-1989
4820968	11-Apr-1989
4823173	18-Apr-1989
4823300	18-Apr-1989
4839711	13-Jun-1989
4845052	04-Jul-1989
4851078	25-Jul-1989
4851257	25-Jul-1989
4854986	08-Aug-1989
4855625	08-Aug-1989
4857764	15-Aug-1989
4859280	22-Aug-1989
4862231	29-Aug-1989
4868778	19-Sep-1989
4873564	10-Oct-1989
4876579	24-Oct-1989
4879520	07-Nov-1989
4879523	07-Nov-1989
4881111	14-Nov-1989
4882698	21-Nov-1989
4888741	19-Dec-1989
4891604	02-Jan-1990
4891606	02-Jan-1990
4893088	09-Jan-1990
4897362	30-Jan-1990

Patent Number	Issue Date
4897366	30-Jan-1990
4897567	30-Jan-1990
4900689	13-Feb-1990
4908566	13-Mar-1990
4908683	13-Mar-1990
4912053	27-Mar-1990
4914501	03-Apr-1990
4916497	10-Apr-1990
4923820	08-May-1990
4923826	08-May-1990
4927777	22-May-1990
4929566	29-May-1990
4929568	29-May-1990
4929923	29-May-1990
4937774	26-Jun-1990
4941027	10-Jul-1990
4945070	31-Jul-1990
4945262	31-Jul-1990
4948746	14-Aug-1990
4949296	14-Aug-1990
4951102	21-Aug-1990
4956306	11-Sep-1990
4968628	06-Nov-1990
4968900	06-Nov-1990
4970573	13-Nov-1990
4970677	13-Nov-1990
4975751	04-Dec-1990
4978868	18-Dec-1990
4978925	18-Dec-1990
4979011	18-Dec-1990
4980651	25-Dec-1990
4982194	01-Jan-1991
4988902	29-Jan-1991
5008719	16-Apr-1991
5010377	23-Apr-1991
5014055	07-May-1991
5014108	07-May-1991
5015877	14-May-1991
5015887	14-May-1991
5021359	04-Jun-1991
5028824	02-Jul-1991
5028973	02-Jul-1991
5030862	09-Jul-1991
5032529	16-Jul-1991
5034343	23-Jul-1991
5034789	23-Jul-1991
5036219	30-Jul-1991
5037765	06-Aug-1991
5038248	06-Aug-1991
5039888	13-Aug-1991
5047974	10-Sep-1991
5051619	24-Sep-1991
5051949	24-Sep-1991
5053345	01-Oct-1991
5053353	01-Oct-1991
5057895	15-Oct-1991
5059982	22-Oct-1991
5060192	22-Oct-1991

58

Patent Number	Issue Date
5066995	19-Nov-1991
5070388	03-Dec-1991
5070451	03-Dec-1991
5070596	10-Dec-1991
5079176	07-Jan-1992
5079608	07-Jan-1992
5079734	07-Jan-1992
5081061	14-Jan-1992
5081063	14-Jan-1992
5081410	14-Jan-1992
5084839	28-Jan-1992
5085084	04-Feb-1992
5086242	04-Feb-1992
5091331	25-Feb-1992
5091336	25-Feb-1992
5095343	10-Mar-1992
5096850	17-Mar-1992
5097319	17-Mar-1992
5105099	14-Apr-1992
5107312	21-Apr-1992
5111268	05-May-1992
5113361	12-May-1992
5117282	26-May-1992
5118632	02-Jun-1992
5119321	02-Jun-1992
5120669	09-Jun-1992
5130569	14-Jul-1992
5134321	28-Jul-1992
5138319	11-Aug-1992
5138413	11-Aug-1992
5140326	18-Aug-1992
5142244	25-Aug-1992
5148475	15-Sep-1992
5150120	22-Sep-1992
5151953	29-Sep-1992
5164802	17-Nov-1992
5184128	02-Feb-1993
5185292	09-Feb-1993
5194867	16-Mar-1993
5196373	23-Mar-1993
5196737	23-Mar-1993
5198385	30-Mar-1993
5200733	06-Apr-1993
5206821	27-Apr-1993
5214329	25-May-1993
5217919	08-Jun-1993
5218213	08-Jun-1993
5218220	08-Jun-1993
5218321	08-Jun-1993
5220868	22-Jun-1993
5228192	20-Jul-1993
5228330	20-Jul-1993
5229661	20-Jul-1993
5233289	03-Aug-1993
5235205	10-Aug-1993
5240876	31-Aug-1993
5241213	31-Aug-1993
5243211	07-Sep-1993

58

Patent Number	Issue Date
5247199	21-Sep-1993
5248894	28-Sep-1993
5248901	28-Sep-1993
5248932	28-Sep-1993
5258939	02-Nov-1993
5260590	09-Nov-1993
5262689	16-Nov-1993
5262976	16-Nov-1993
5264719	23-Nov-1993
5265225	23-Nov-1993
5266135	30-Nov-1993
5270265	14-Dec-1993
5270569	14-Dec-1993
5272104	21-Dec-1993
5276633	04-Jan-1994
5279850	18-Jan-1994
5283461	01-Feb-1994
5287068	15-Feb-1994
5287071	15-Feb-1994
5289336	22-Feb-1994
5293052	08-Mar-1994
5298434	29-Mar-1994
5300877	05-Apr-1994
5302859	12-Apr-1994
5306650	26-Apr-1994
5306944	26-Apr-1994
5307023	26-Apr-1994
5311054	10-May-1994
5311070	10-May-1994
5312262	17-May-1994
5315144	24-May-1994
5317184	31-May-1994
5319757	07-Jun-1994
5322804	21-Jun-1994
5323036	21-Jun-1994
5327006	05-Jul-1994
5329187	12-Jul-1994
5332931	26-Jul-1994
5334273	02-Aug-1994
5334929	02-Aug-1994
5335132	02-Aug-1994
5338960	16-Aug-1994
5341009	23-Aug-1994
5341335	23-Aug-1994
5345236	06-Sep-1994
5347169	13-Sep-1994
5350935	27-Sep-1994
5352327	04-Oct-1994
5357089	18-Oct-1994
5359211	25-Oct-1994
5359236	25-Oct-1994
5362667	08-Nov-1994
5366932	22-Nov-1994
5367211	22-Nov-1994
5369309	29-Nov-1994
5370568	06-Dec-1994
5373183	13-Dec-1994
5382541	17-Jan-1995

58

Patent Number	Issue Date
5382825	17-Jan-1995
5382916	17-Jan-1995
5387555	07-Feb-1995
5391903	21-Feb-1995
5395774	07-Mar-1995
5397714	14-Mar-1995
5399892	21-Mar-1995
5406223	11-Apr-1995
5416351	16-May-1995
5418002	23-May-1995
5420499	30-May-1995
5422288	06-Jun-1995
5423889	13-Jun-1995
5424563	13-Jun-1995
5428492	27-Jun-1995
5429958	04-Jul-1995
5429993	04-Jul-1995
5434357	18-Jul-1995
5436189	25-Jul-1995
5438221	01-Aug-1995
5440506	08-Aug-1995
5446316	29-Aug-1995
5446368	29-Aug-1995
5448100	05-Sep-1995
5448102	05-Sep-1995
5450326	12-Sep-1995
5450339	12-Sep-1995
5451263	19-Sep-1995
5455442	03-Oct-1995
5455782	03-Oct-1995
5463344	31-Oct-1995
5466963	14-Nov-1995
5468668	21-Nov-1995
5469556	21-Nov-1995
5471131	28-Nov-1995
5473193	05-Dec-1995
5481129	02-Jan-1996
5493207	20-Feb-1996
5493581	20-Feb-1996
5497013	05-Mar-1996
5504033	02-Apr-1996
5504449	02-Apr-1996
5508551	16-Apr-1996
5515402	07-May-1996
5515417	07-May-1996
5515434	07-May-1996
5516625	14-May-1996
5517047	14-May-1996
5517058	14-May-1996
5517565	14-May-1996
5519732	21-May-1996
5521436	28-May-1996
5525869	11-Jun-1996
5526392	11-Jun-1996
5526768	18-Jun-1996
5528682	18-Jun-1996
5532635	02-Jul-1996
5539707	23-Jul-1996

56

Patent Number	Issue Date
5541435	30-Jul-1996
5541538	30-Jul-1996
5544095	06-Aug-1996
5546038	13-Aug-1996
5547896	20-Aug-1996
5548542	20-Aug-1996
5552345	03-Sep-1996
5557175	17-Sep-1996
5561303	01-Oct-1996
5561607	01-Oct-1996
5563834	08-Oct-1996
5567978	22-Oct-1996
5569620	29-Oct-1996
5569957	29-Oct-1996
5570392	29-Oct-1996
5570407	29-Oct-1996
5572161	05-Nov-1996
5572162	05-Nov-1996
5574572	12-Nov-1996
5574609	12-Nov-1996
5574618	12-Nov-1996
5574671	12-Nov-1996
5576654	19-Nov-1996
5576695	19-Nov-1996
5577656	26-Nov-1996
5580816	03-Dec-1996
5581444	03-Dec-1996
5581475	03-Dec-1996
5583442	10-Dec-1996
5585310	17-Dec-1996
5585661	17-Dec-1996
5586072	17-Dec-1996
5587103	24-Dec-1996
5594261	14-Jan-1997
5598157	28-Jan-1997
5602052	11-Feb-1997
5602054	11-Feb-1997
5603779	18-Feb-1997
5606288	25-Feb-1997
5608259	04-Mar-1997
5608264	04-Mar-1997
5610093	11-Mar-1997
5610792	11-Mar-1997
5614422	25-Mar-1997
5614852	25-Mar-1997
5614867	25-Mar-1997
5617090	01-Apr-1997
5617344	01-Apr-1997
5617473	01-Apr-1997
5618752	08-Apr-1997
5619270	08-Apr-1997
5621307	15-Apr-1997
5621355	15-Apr-1997
5621477	15-Apr-1997
5621478	15-Apr-1997
5622878	22-Apr-1997
5622890	22-Apr-1997
5625566	29-Apr-1997

Patent Number	Issue Date
5627489	06-May-1997
5631599	20-May-1997
5633180	27-May-1997
5633815	27-May-1997
5636274	03-Jun-1997
5637908	10-Jun-1997
5639688	17-Jun-1997
5640300	17-Jun-1997
5640346	17-Jun-1997
5642247	24-Jun-1997
5643821	01-Jul-1997
5644309	01-Jul-1997
5646067	08-Jul-1997
5648678	15-Jul-1997
5649009	15-Jul-1997
5650344	22-Jul-1997
5650639	22-Jul-1997
5650658	22-Jul-1997
5650971	22-Jul-1997
5652153	29-Jul-1997
5654226	05-Aug-1997
5654662	05-Aug-1997
5654991	05-Aug-1997
5656512	12-Aug-1997
5659261	19-Aug-1997
5659269	19-Aug-1997
5659570	19-Aug-1997
5661736	26-Aug-1997
5663860	02-Sep-1997
5665634	09-Sep-1997
5666083	09-Sep-1997
5668397	16-Sep-1997
5668409	16-Sep-1997
5668468	16-Sep-1997
5669599	23-Sep-1997
5670413	23-Sep-1997
5670799	23-Sep-1997
5671272	23-Sep-1997
5672998	30-Sep-1997
5675281	07-Oct-1997
5675339	07-Oct-1997
5677599	14-Oct-1997
5678030	14-Oct-1997
5680072	21-Oct-1997
5682062	28-Oct-1997
5682111	28-Oct-1997
5682336	28-Oct-1997
5683075	04-Nov-1997
5683939	04-Nov-1997
5684305	04-Nov-1997
5686322	11-Nov-1997
5686822	11-Nov-1997
5689129	18-Nov-1997
5694417	02-Dec-1997
5696452	09-Dec-1997
5701097	23-Dec-1997
5708549	13-Jan-1998
5712870	27-Jan-1998

Patent Number	Issue Date
5717243	10-Feb-1998
5717322	10-Feb-1998
5717617	10-Feb-1998
5717736	10-Feb-1998
5719326	17-Feb-1998
5724370	03-Mar-1998
5728624	17-Mar-1998
5729038	17-Mar-1998
5732105	24-Mar-1998
5736885	07-Apr-1998
5736903	07-Apr-1998
5742204	21-Apr-1998
5744851	28-Apr-1998
5744852	28-Apr-1998
5745563	28-Apr-1998
5750432	12-May-1998
5757036	26-May-1998
5757794	26-May-1998
5764113	09-Jun-1998
5767740	16-Jun-1998
5767757	16-Jun-1998
5770878	23-Jun-1998
5770880	23-Jun-1998
5771012	23-Jun-1998
5773151	30-Jun-1998
5773891	30-Jun-1998
5776814	07-Jul-1998
5777346	07-Jul-1998
5777362	07-Jul-1998
5780311	14-Jun-1998
5782975	21-Jul-1998
5789949	04-Aug-1998
5789982	04-Aug-1998
5790060	04-Aug-1998
5793193	11-Aug-1998
5798557	25-Aug-1998
5798724	29-Aug-1998
5801084	01-Sep-1998
5804846	08-Sep-1998
5805020	08-Sep-1998
5807780	15-Sep-1998
5807783	15-Sep-1998
5808348	15-Sep-1998
5808353	15-Sep-1998
5808489	15-Sep-1998
5808883	15-Sep-1998
5809410	15-Sep-1998
5812029	22-Sep-1998
5812658	22-Sep-1998
5814889	29-Sep-1998
5817564	06-Oct-1998
5821740	13-Oct-1998
5825092	20-Oct-1998
5830048	03-Nov-1998
5830279	03-Nov-1998
5831423	03-Nov-1998
5833758	10-Nov-1998
5837553	17-Nov-1998

Patent Number	Issue Date
5837603	17-Nov-1998
5841169	24-Nov-1998
5841182	24-Nov-1998
5841324	24-Nov-1998
5849627	15-Dec-1998
5851864	22-Dec-1998
5856695	05-Jan-1999
5856700	05-Jan-1999
5856742	05-Jan-1999
5861826	19-Jan-1999
5870266	09-Feb-1999
5872028	16-Feb-1999
5872044	16-Feb-1999
5877041	02-Mar-1999
5877044	02-Mar-1999
5880513	09-Mar-1999
5882423	16-Mar-1999
5883414	16-Mar-1999
5883565	16-Mar-1999
5883921	16-Mar-1999
5892223	06-Apr-1999
5892264	06-Apr-1999
5892375	06-Apr-1999
5892472	06-Apr-1999
5894141	13-Apr-1999
5895953	20-Apr-1999
5896053	20-Apr-1999
5900643	04-May-1999
5913130	15-Jun-1999
5914280	22-Jun-1999
5915168	22-Jun-1999
5920108	06-Jul-1999
5920219	06-Jul-1999
5920224	06-Jul-1999
5920452	06-Jul-1999
5923207	13-Jul-1999
5923209	13-Jul-1999
B1 5051619	02-Mar-1993

PATENT ASSIGNMENT

Electronic Version v1.1
Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	CHANGE OF NAME
CONVEYING PARTY DATA	
Name	Execution Date
INTERSIL CORPORATION	05/25/2001
RECEIVING PARTY DATA	
Name:	INTERSIL COMMUNICATIONS, INC.
Street Address:	1001 Murphy Ranch Road
City:	Milpitas
State/Country:	CALIFORNIA
Postal Code:	95035
PROPERTY NUMBERS Total: 2	
Property Type	Number
Patent Number:	4823173
Patent Number:	5264719
CORRESPONDENCE DATA	
Fax Number:	(703)931-6037
<i>Correspondence will be sent via US Mail when the fax attempt is unsuccessful.</i>	
Phone:	2022363707
Email:	wgwalter@aol.com
Correspondent Name:	Wallace G. Walter
Address Line 1:	5726 Clarence Ave
Address Line 4:	Alexandria, VIRGINIA 22311
NAME OF SUBMITTER:	Wallace G. Walter
Total Attachments: 4 source=IntersilNameChange#page1.tif source=IntersilNameChange#page2.tif source=IntersilNameChange#page3.tif source=IntersilNameChange#page4.tif	

CH 4823173 \$80.00

Delaware

PAGE 1

The First State

I, HARRIET SMITH WINDSOR, SECRETARY OF STATE OF THE STATE OF DELAWARE, DO HEREBY CERTIFY THE ATTACHED IS A TRUE AND CORRECT COPY OF THE RESTATED CERTIFICATE OF "INTERSIL CORPORATION", CHANGING ITS NAME FROM "INTERSIL CORPORATION" TO "INTERSIL COMMUNICATIONS, INC.", FILED IN THIS OFFICE ON THE TWENTY-FIFTH DAY OF MAY, A.D. 2001, AT 4:15 O'CLOCK P.M.



Harriet Smith Windsor

3050122 8100

050839147

DATE: 10-13-05

PATENT

REEL: 017468 FRAME: 0603

**AMENDED AND RESTATED CERTIFICATE OF INCORPORATION
OF
INTERSIL CORPORATION**

INTERSIL CORPORATION, a corporation organized and existing under the laws of the State of Delaware, hereby certifies as follows:

FIRST: The present name of the corporation is INTERSIL CORPORATION and the name under which the corporation was originally incorporated is HSS Operating Corporation. The date of filing of its original Certificate of Incorporation with the Secretary of State of the State of Delaware was June 2, 1999.


SECOND: This Amended and Restated Certificate of Incorporation (the "Certificate") restates and integrates and further amends in its entirety the Certificate of Incorporation of this corporation. This Certificate was duly adopted by a majority vote of the stockholders of the corporation in accordance with Sections 228, 242 and 245 of the General Corporation Law of the State of Delaware.

THIRD: This Certificate shall become effective immediately upon its filing with the Secretary of State of the State of Delaware.

FOURTH: Upon the filing of the Certificate with the Secretary of State of the State of Delaware, the Certificate of Incorporation of the corporation shall be amended and restated in its entirety to read as set forth on Exhibit A attached hereto.

IN WITNESS WHEREOF, said corporation has caused this Certificate to be executed by a duly authorized officer this 23rd day of May, 2001.

By:


Gregory Williams
Chief Executive Officer

740322.2.01 5/24/2001 3:35 PM

STATE OF DELAWARE
SECRETARY OF STATE
DIVISION OF CORPORATIONS
FILED 04:15 PM 05/25/2001
010253080 - 3050122

**PATENT
REEL: 017468 FRAME: 0604**

EXHIBIT A


**AMENDED AND RESTATED CERTIFICATE OF INCORPORATION
OF
INTERSIL COMMUNICATIONS, INC.**

1. **Name.** The name of the Corporation is **Intersil Communications, Inc.**
2. **Registered Office and Agent.** The address of the Corporation's registered office in the State of Delaware is 1209 Orange Street, in the City of Wilmington, County of New Castle. The name of the Corporation's registered agent at such address is The Corporation Trust Company.
3. **Purpose.** The purposes for which the Corporation is formed are to engage in any lawful act or activity, including, without limitation, forming and/or acquiring foreign subsidiaries, for which corporations may be organized under the General Corporation Law of the State of Delaware ("DGCL") and to possess and exercise all of the powers and privileges granted by such law and any other law of Delaware.
4. **Authorized Capital.** The aggregate number of shares of stock which the Corporation shall have authority to issue is One Thousand (1,000) shares, all of which are of one class and are designated as Common Stock, par value \$.01 per share.
5. **Incorporator.** The name and mailing address of the incorporator are Marian T. Ryan, 4000 Bell Atlantic Tower, 1717 Arch Street, Philadelphia, Pennsylvania 19103-2793.
6. **Bylaws.** In furtherance and not in limitation of the powers conferred by law, the board of directors of the Corporation is authorized to adopt, amend or repeal the bylaws of the Corporation, except as otherwise specifically provided therein, subject to the powers of the stockholders of the Corporation to amend or repeal any bylaws adopted by the board of directors.
7. **Elections of Directors.** Elections of directors need not be by written ballot unless and except to the extent the bylaws of the Corporation shall so provide.
8. **Right to Amend.** The corporation reserves the right to amend or repeal any provision contained in this Certificate as the same may from time to time be in effect in the manner now or hereafter prescribed by law, and all rights, preferences and privileges conferred on stockholders, director or others hereunder are subject to such reservation.
9. **Unanimous Written Consent Required.** If any action is to be taken by stockholders without a meeting, such action must be authorized by unanimous written consent signed by a l of the holders of outstanding voting stock.

10. *Limitation on Liability.* The directors of the Corporation shall be entitled to the benefits of all limitations on the liability of directors generally that are now or hereafter become available under the DGCL. Without limiting the generality of the foregoing, to the fullest extent permitted by the DGCL, as it exists on the date hereof or as it may hereafter be amended, no director of the Corporation shall be personally liable to the Corporation or its stockholders for monetary damages for breach of fiduciary duty as a director, except for liability (i) for any breach of the director's duty of loyalty to the Corporation or its stockholders, (ii) for acts or omissions not in good faith or which involve intentional misconduct or a knowing violation of law, (iii) under Section 174 of the DGCL, or (iv) for any transaction from which the director derived an improper personal benefit. Any repeal or modification of this Section 10 shall be prospective only, and shall not affect, to the detriment of any director, any limitation on the personal liability of a director of the Corporation existing at the time of such repeal, modification or adoption.

Dated: May 23, 2001

By:



Gregory L. Williams
Chief Executive Officer

PATENT ASSIGNMENT

Electronic Version v1.1
Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT
CONVEYING PARTY DATA	
Name	Execution Date
INTERSIL COMMUNICATIONS, INC.	12/21/2001
RECEIVING PARTY DATA	
Name:	INTERSIL AMERICAS, INC.
Street Address:	1001 MURPHY RANCH ROAD
City:	MILPITAS
State/Country:	CALIFORNIA
Postal Code:	95035
PROPERTY NUMBERS Total: 2	
Property Type	Number
Patent Number:	4823173
Patent Number:	5264719
CORRESPONDENCE DATA	
Fax Number:	(703)931-6037
<i>Correspondence will be sent via US Mail when the fax attempt is unsuccessful.</i>	
Phone:	2022363707
Email:	wgwalter@aol.com
Correspondent Name:	Wallace G. Walter
Address Line 1:	5726 Clarence Ave.
Address Line 4:	Alexandria, VIRGINIA 22311
NAME OF SUBMITTER:	Wallace G. Walter
Total Attachments: 4 source=IntersilContribAgmt#page1.tif source=IntersilContribAgmt#page2.tif source=IntersilContribAgmt#page3.tif source=IntersilContribAgmt#page4.tif	

CH \$80.00 4823173

CONTRIBUTION AGREEMENT

This Contribution Agreement (the "Agreement") is effective as of December 31, 2001 (the "Effective Date") at 11:59 PM United States of America EST (the "Effective Time") by and between Intersil Communications, Inc., a Delaware corporation ("Intersil"), and Intersil Americas Inc., a Delaware corporation ("Intersil Americas").

Background

To promote greater efficiency and economy in the management of the businesses carried on by the parties to this Agreement, Intersil desires to make a capital contribution to Intersil Americas of certain intellectual property and other assets used in the business of Intersil and its affiliates.

Terms

Intending to be legally bound, the parties to this Agreement agree as follows:

1. Effective as of the date first written above, Intersil shall contribute the following to Intersil Americas, in deemed exchange for stock of Intersil Americas in a non-recognition transaction as described in Section 351 of the Internal Revenue Code of 1986, as amended:

(i) all right, title and interest in and to the trademarks shown in Schedule A and all slogans, logotypes, designs, and trade dress associated therewith (the "Trademarks"), together with the U.S. federal registrations and applications for registration of the Trademarks, in and to all income, royalties, damages and payments now or hereafter due or payable with respect thereto and in and to all rights of action arising from the Trademarks, to be held and enjoyed by Intersil Americas for its own use and benefit and for its successors and assigns as the same would have been held by Intersil had this contribution not been made, and the goodwill of the business symbolized by the Trademarks;

(ii) all right, title and interest in and to the U.S. patents and patent applications shown in Schedule A (the "Patents"), including all reissues, divisions, continuations, continuations-in-part, and extensions thereof, to be held and enjoyed by Intersil Americas as fully and entirely as they would have been held and enjoyed by Intersil if this contribution had not been made, including all licenses of and proceeds from the Patents, all claims, demands and rights to recovery that Intersil has or may have in profits and damages for past and future infringements, if any, and all rights to compromise, sue for, and collect such profits and damages;

(iii) all right, title, and interest in and to all inventions shown in Schedule A (the "Inventions"), and all intellectual property rights relating thereto, including, without limitation, trade secret rights in the Inventions, and all rights of action arising from the Inventions, to be held and enjoyed by Intersil Americas for its own use and benefit and for its successors and assigns as the same would have been held by Intersil had this contribution not been made; and

(iv) all right, title, and interest in and to all copyrights owned by Intersil as of the date first written above that are not otherwise excluded from contribution under the terms of this Agreement, whether or not such copyrights have been registered (collectively, the "Copyrights")

including, without limitation, all U.S. registrations and applications for registration of the Copyrights, all licenses of and proceeds from the Copyrights, all publishing, electronic publishing, and other proprietary rights arising from or related to the Copyrights, all causes of action relating to the Copyrights that may have arisen prior to this contribution, and any recovery resulting from such causes of action.

Notwithstanding the foregoing or any specific item listed on Schedule A, the intellectual property used in connection with providing products or services that are regulated by the United States Department of State shall not be contributed to Intersil Americas.

2. Intersil and Intersil Americas shall each take any and all additional actions as may be necessary or appropriate to effect the transactions contemplated by this Agreement. Such actions may include, without limitation, the execution of additional documents to record the contribution made in this Agreement and the filing of such documents with the appropriate governmental authorities.

[Signatures commence on the following page]

IN WITNESS WHEREOF, the parties have caused this Agreement to be executed as of the date below to be effective as of the Effective Date and Effective Time.

INTERSIL COMMUNICATIONS, INC.
a Delaware corporation

By: Paul A. Bernkopf Date: 12/21/01
Name: PAUL A. BERNKOPF
Title: ASST. SECRETARY

INTERSIL AMERICAS INC.
a Delaware Corporation

By: Paul A. Bernkopf Date: 12/21/01
Name: PAUL A. BERNKOPF
Title: ASST. SECRETARY

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

ClientRef	SubCase	Status	Appl #	FileDate	Pat#	IssDate	Title
SE-358		Granted	774474	10-Sep-1985	4677321	30-Jun-1987	A TTL COMPATIBLE INPUT BUFFER
SE-352		Granted	793316	31-Oct-1985	4682059	21-Jul-1987	A COMPARATOR INPUT STAGE FOR INTERFACE WITH SIGNAL CURRENT
SE-359		Granted	782691	01-Oct-1985	4650896	17-Mar-1987	PROCESS USING TUNGSTEN FOR MULTILEVEL METALIZATION
SE-363		Granted	936609	01-Dec-1986	4781853	01-Nov-1988	METHOD OF ETCH & ENHANCE SILICON ETCHING CAP OF ALKALI HYDROXIDE THROUGH ADD OF POSITIVE VALENCE IMPURITY IONS
SE-363	A	Granted	187268	28-Apr-1988	4859280	22-Aug-1989	METHOD OF ETCH & ENHANCE SILICON ETCHING CAP OF ALKALI HYDROXIDE THROUGH ADD OF POSITIVE VALENCE IMPURITY IONS
SE-370		Granted	723238	15-Apr-1985	4705596	10-Nov-1987	SIMULTANEOUS PLASMA SCULPTURING AND DUAL TAPERED VIA ETCH
SE-377		Granted	782689	01-Oct-1985	4636744	13-Jan-1987	FRONT END OF AN OPERATIONAL AMPLIFIER
SE-704		Granted	771712	03-Sep-1985	4624749	25-Nov-1986	ELECTRODEPOSITION OF SUBMICROMETER METALLIC INTERCONNECT FOR INTEGRATED CIRCUITS
SE-705		Granted	768328	22-Aug-1985	4716071	29-Dec-1987	METHOD FOR ENSURING ADHESION OF CHEMICALLY VAPOR DEPOSITED OXIDE TO GOLD INTEGRATED CIRCUIT INTERCONNECT LINES
SE-705	A	Granted	045526	04-May-1987	4713260	15-Dec-1987	METHOD FOR ENSURING ADHESION OF CHEMICALLY VAPOR DEPOSITED OXIDE TO GOLD INTEGRATED CIRCUIT INTERCONNECT LINES
SE-385		Granted	896097	13-Aug-1986	4755770	05-Jul-1988	LOW NOISE CURRENT SPECTRAL DENSITY INPUT BIAS CURRENT CANCEL SCHEME
SE-394		Granted	723239	15-Apr-1985	4705597	10-Nov-1987	PHOTORESIST TAPERING PROCESS
SE-395		Granted	831384	07-Jan-1986	4823173	18-Apr-1989	HIGH VOLTAGE LATERAL MOS STRUCTURE WITH DEPLETED TOP GATE REGION
SE-395	B	Granted	07705509	24-May-1991	5264719	23-Nov-1993	HIGH VOLTAGE LATERAL MOS STRUCTURE WITH DEPLETED TOP GATE REGION

Patent License Agreement

This Patent License Agreement ("PLA") is entered into on this 30th day of March, 2006 by and between Intersil Corporation ("Intersil") and Fairchild Semiconductor Corporation ("Fairchild") (collectively, the "Parties").

1.

REDACTED

1.1

1.2

Power Integrations, Incorporated, including its parents, subsidiaries and consolidated entities (any or all of which, "POWI"). **REDACTED**

United States Patent No. 4,823,173 and/or United States Patent No. 5,264,719, including any and all re-examinations, reissues or certificates of correction relating to such patents (collectively, the "Patents").

1.3

REDACTED

2.

2.1

REDACTED

2.2

3. **Additional Rights Granted Fairchild**

3.1

REDACTED

Intersil

grants to Fairchild the sole and exclusive right, exclusive even as to Intersil, to enforce the Patents against POWI, to assert, litigate and prosecute claims of Infringement under the Patents against POWI, including without limitation in any U.S. federal court or before the International Trade Commission, and to seek all equitable, injunctive, monetary and other relief and to collect for later distribution under Paragraph 1.2 any and all past damages in connection with Infringement of the Patents by POWI, and to settle and compromise any disputes with POWI related to the Patents. Except as provided herein, the Parties agree that only Fairchild shall have the authority to threaten, commence, maintain or settle any claim, suit or proceeding based upon Infringement of the Patents (or other trespass or similar action relating to the Patents and the inventions therein claimed) by POWI.

3.2

3.3

REDACTED

REDACTED

3.4

3.5

REDACTED

3.6

4. **Representations and Warranties**

4.1 Intersil represent and warrants as follows:

A. Intersil has the authority to enter into this PLA and to convey the rights conveyed herein, and that the execution and performance of this PLA does not conflict with Intersil's certificate of incorporation, by-laws or contract obligations.

B. Intersil is the sole owner of the Patents, the Patents have been and will be maintained, and that all inventors of the inventions claimed in the Patents have assigned title and ownership of the inventions to Intersil.

C.

4.2

A.

REDACTED

B.

C.

5. **Confidentiality**

The terms and conditions of this PLA, all communications, discussions and correspondence relating to this PLA, and all actions taken in performance of the PLA, shall be "Common Interest Information" covered by the Joint Defense and Confidentiality Agreement between the Parties, dated March 12, 2001, and shall be maintained in strict confidence in accordance with such Joint Defense and Confidentiality Agreement.

REDACTED

The parties have duly executed this Agreement as of the date first above written.

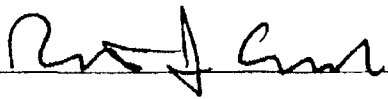
INTERSIL CORPORATION

By: _____

Name: _____

Title: _____

FAIRCHILD SEMICONDUCTOR CORPORATION

By:  _____

Name: Robert J. Conrad

Title: Senior Vice President – Analog Products

The parties have duly executed this Agreement as of the date first above written.

INTERSIL CORPORATION

By: Douglas A. Balog

Name: DOUGLAS A. BALOG

Title: ASST. SECRETARY

FAIRCHILD SEMICONDUCTOR CORPORATION

By: _____

Name: Robert J. Conrad

Title: Senior Vice President – Analog Products

Supplemental Agreement

This Supplemental Agreement amends and, to the extent necessary, modifies *nunc pro tunc* the Patent License Agreement ("PLA") dated March 30, 2006 between Intersil Corporation ("Intersil") and Fairchild Semiconductor Corporation ("Fairchild") (collectively, the "Parties").

Intersil Americas, Inc. ("Intersil Americas"), as title holder of record of United States Patent No. 4,823,173 and United States Patent No. 5,264,719 (the "Patents"), hereby fully ratifies the terms of the March 30, 2006 PLA. Intersil Americas further acknowledges that its parent corporation, Intersil Corporation, was authorized to enter into the PLA on behalf of Intersil Americas, and to agree to the terms stated therein. Intersil Americas agrees to be bound by, and hereby reaffirms, the representations and warranties made by Intersil Corporation in the PLA.

It is the intent of the parties hereto that this Supplemental Agreement shall be retroactive to March 30, 2006, and shall have the effect of assigning and conveying from Intersil Americas to Fairchild, as of March 30, 2006, the specific rights to the Patents as detailed in the PLA as if Intersil Americas – and not Intersil Corporation – was the original party to the PLA. This Supplemental Agreement does not modify the substantive rights of Fairchild under the PLA, and the substantive rights afforded to Intersil Corporation under the PLA remain unchanged, but will be deemed to reside in Intersil Americas. Intersil Corporation shall remain bound under the PLA itself. This Supplemental Agreement does not alter the ongoing obligations, if any, of any Intersil related entity under the Asset Purchase Agreement and the related Intellectual Property Assignment and License Agreement between Intersil Corporation and Fairchild dated January 20, 2001. Intersil Americas assumes no obligations other than as expressly set forth herein and in the body of the PLA.

Executed on May 18, 2006, but effective March 30, 2006.

INTERSil CORPORATION

By: Douglas A. Balog
Name: DOUGLAS A. BALOG
Title: ASST. SECRETARY

INTERSil AMERICAS, INC.

By: Douglas A. Balog
Name: DOUGLAS A. BALOG
Title: ASST. SECRETARY

FAIRCHILD SEMICONDUCTOR CORPORATION

By: Paul D. Deluca
Name: PAUL D. DELUCA
Title: SVP, GENERAL COUNSEL & SECRETARY

IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

FAIRCHILD SEMICONDUCTOR	§	
CORPORATION, a Delaware corporation,	§	
INTERSIL CORPORATION, a Delaware	§	
Corporation, and INTERSIL AMERICAS, INC.,	§	
a Delaware Corporation	§	C.A. No. 2:06cv151 (TJW)
	§	JURY
v.	§	
	§	
POWER INTEGRATIONS, INC. a Delaware	§	
Corporation	§	

**UNOPPOSED MOTION FOR EXTENSION OF TIME TO ANSWER, MOVE
OR OTHERWISE RESPOND TO PLAINTIFFS' AMENDED COMPLAINT**

POWER INTEGRATIONS, INC. moves the Court for an extension of time to answer, move or otherwise respond to FAIRCHILD SEMICONDUCTOR CORPORATION, INTERSIL CORPORATION, and INTERSIL AMERICAS, INC.'s Amended Complaint, and would respectfully show the Court as follows:

1. Plaintiffs, FAIRCHILD SEMICONDUCTOR CORPORATION and INTERSIL CORPORATION, filed their Original Complaint against POWER INTEGRATIONS on or about April 11, 2006 [Dkt. 1].
2. Plaintiffs, FAIRCHILD SEMICONDUCTOR CORPORATION, INTERSIL CORPORATION and INTERSIL AMERICAS, INC. filed their Amended Complaint against POWER INTEGRATIONS on or about May 19, 2006 [Dkt. 8].
3. The issues involved in this case are such that POWER INTEGRATIONS, INC. requires additional time to prepare a response.
4. POWER INTEGRATIONS, INC. respectfully requests an extension of time to answer, move or otherwise respond, in any manner whatsoever, to Plaintiffs' Amended

Complaint, up to and including June 19, 2006, and POWER INTERGRATIONS, INC. agrees not to seek any further extension of time to respond to the Amended Complaint.

5. Plaintiffs, FAIRCHILD SEMICONDUCTOR CORPORATION, INTERSIL CORPORATION and INTERSIL AMERICAS, INC. are not opposed to said extension of time to answer, move or otherwise respond.

WHEREFORE, PREMISES CONSIDERED, POWER INTEGRATIONS, INC. prays that the Court grant this Unopposed Motion for Extension of Time by extending the time period for POWER INTEGRATIONS, INC. to answer or otherwise respond to Plaintiff's Amended Complaint until June 19, 2006.

Respectfully submitted,

/s/ Michael E. Jones
MICHAEL E. JONES
State Bar No. 10929400
POTTER MINTON
A Professional Corporation
110 N. College, Suite 500 (75702)
P. O. Box 359
Tyler, Texas 75710
(903) 597 8311
(903) 593 0846 (Facsimile)
mikejones@potterminton.com

ATTORNEYS FOR DEFENDANT
POWER INTEGRATIONS, INC.

CERTIFICATE OF CONFERENCE

I certify that Michael Headley, counsel for Power Integrations, has conferred with Guy Hopkins and Bas de Blank, counsel for Plaintiffs, and that Bas de Blank states that Plaintiffs are unopposed to the relief sought in this motion.

/s/ Michael E. Jones

CERTIFICATE OF SERVICE

The undersigned hereby certifies that all counsel of record who are deemed to have consented to electronic service are being served with a copy of this document via the Court's CM/ECF system per Local Rule CV-5(a)(3) on June 2, 2006. Any other counsel of record will be served by facsimile transmission and first class mail.

/s/ Michael E. Jones

Michael E. Jones

IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

FAIRCHILD SEMICONDUCTOR	§	
CORPORATION, a Delaware corporation,	§	
INTERSIL CORPORATION, a Delaware	§	
Corporation, and INTERSIL AMERICAS, INC.,	§	
a Delaware Corporation	§	
	§	C.A. No. 2:06cv151 (TJW)
v.	§	JURY
	§	
POWER INTEGRATIONS, INC. a Delaware	§	
Corporation	§	

**ORDER GRANTING POWER INTEGRATIONS' UNOPPOSED MOTION FOR
EXTENSION OF TIME TO ANSWER, MOVE OR OTHERWISE RESPOND TO
PLAINTIFFS' AMENDED COMPLAINT**

ON THIS DAY, came on to be considered the Unopposed Motion for Extension of Time to Answer, Move or Otherwise Respond to the Amended Complaint of Plaintiffs, FAIRCHILD SEMICONDUCTOR CORPORATION, INTERSIL CORPORATION and INTERSIL AMERICAS, INC. in the above-styled and numbered cause up to and including June 19, 2006. After considering said motion, the Court is of the opinion that said motion should be GRANTED.

IT IS THEREFORE ORDERED that POWER INTEGRATIONS shall have up to and including June 19, 2006 to answer, move or otherwise respond in any manner whatsoever to Plaintiffs', FAIRCHILD SEMICONDUCTOR CORPORATION, INTERSIL CORPORATION and INTERSIL AMERICAS, INC.'S Amended Complaint [Dkt. 8].

IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

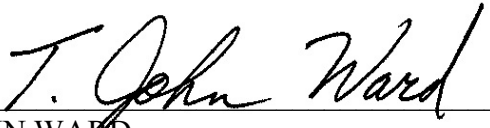
FAIRCHILD SEMICONDUCTOR	§	
CORPORATION, a Delaware corporation,	§	
INTERSIL CORPORATION, a Delaware	§	
Corporation, and INTERSIL AMERICAS, INC.,	§	
a Delaware Corporation	§	
	§	C.A. No. 2:06cv151 (TJW)
v.	§	JURY
	§	
POWER INTEGRATIONS, INC. a Delaware	§	
Corporation	§	

**ORDER GRANTING POWER INTEGRATIONS' UNOPPOSED MOTION FOR
EXTENSION OF TIME TO ANSWER, MOVE OR OTHERWISE RESPOND TO
PLAINTIFFS' AMENDED COMPLAINT**

ON THIS DAY, came on to be considered the Unopposed Motion for Extension of Time to Answer, Move or Otherwise Respond to the Amended Complaint of Plaintiffs, FAIRCHILD SEMICONDUCTOR CORPORATION, INTERSIL CORPORATION and INTERSIL AMERICAS, INC. in the above-styled and numbered cause up to and including June 19, 2006. After considering said motion, the Court is of the opinion that said motion should be GRANTED.

IT IS THEREFORE ORDERED that POWER INTEGRATIONS shall have up to and including June 19, 2006 to answer, move or otherwise respond in any manner whatsoever to Plaintiffs', FAIRCHILD SEMICONDUCTOR CORPORATION, INTERSIL CORPORATION and INTERSIL AMERICAS, INC.'S Amended Complaint [Dkt. 8].

SIGNED this 9th day of June, 2006.



T. JOHN WARD
UNITED STATES DISTRICT JUDGE

**UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS**

FAIRCHILD SEMICONDUCTOR
CORPORATION, a Delaware corporation,
INTERSIL AMERICAS, INC., a Delaware
corporation and INTERSIL CORPORATION,
a Delaware corporation
Plaintiffs,

V.

POWER INTEGRATIONS, INC., a Delaware
corporation.
Defendant

S

2:06cv-151 (TJW)

POWER INTEGRATIONS, INC.'S ANSWER

JURY TRIAL DEMANDED

**POWER INTEGRATIONS, INC.'S ANSWER TO PLAINTIFFS' FIRST AMENDED
COMPLAINT**

Pursuant to Rule 8 of the Federal Rules of Civil Procedure, Defendant Power Integrations, Inc. (“Power Integrations”) hereby responds to the Amended Complaint of Fairchild Semiconductor Corporation (hereinafter, “Fairchild”), Intersil Americas, Inc. (hereinafter, “Intersil Americas”) and Intersil Corporation, (hereinafter, “Intersil”) (collectively, “Plaintiffs”).

Power Integrations denies each and every allegation contained in the Amended Complaint that is not expressly admitted below. Any factual allegation admitted below is admitted only as to the specific admitted facts, not as to any purported conclusions, characterizations, implications, or speculations that arguably follow from the admitted facts. Power Integrations denies that Plaintiffs are entitled to the relief requested or any other.

THE PARTIES

1. On information and belief, Power Integrations admits the allegations of Paragraph 1 of the Amended Complaint.

2. On information and belief, Power Integrations admits the allegations of Paragraph 2 of the Amended Complaint.

3. On information and belief, Power Integrations admits the allegations of Paragraph 3 of the Amended Complaint.

4. Power Integrations admits that it is a Delaware corporation having a principal place of business in San Jose, California.

JURISDICTION AND VENUE

5. In response to Paragraph 5 of the Amended Complaint, Power Integrations admits that the Amended Complaint purports to state a cause of action under the patent laws of the United States, Title 35 U.S.C. § 1 *et seq.*, and that this Court has subject matter jurisdiction over patent cases pursuant to 28 U.S.C. §§ 1331 and 1338(a). Power Integrations denies the remaining allegations of Paragraph 5 of the Amended Complaint.

6. Power Integrations admits this Court has personal jurisdiction over Power Integrations. As Plaintiffs have yet to identify any accused devices, though, Power Integrations lacks sufficient knowledge to admit or deny the remaining allegations of Paragraph 6 of the Amended Complaint, and therefore denies those allegations.

7. Power Integrations denies the allegations of Paragraph 7 of the Amended Complaint; Fairchild lacks standing to sue Power Integrations, and venue is not proper in this District because the parties are already litigating the technology raised in the Amended Complaint in another case in the District of Delaware, C.A. No. 04-1371 JJF. Plaintiffs did not comply with Local Rule SV-42(a) when they failed to identify the Delaware litigation as a related case on the Civil Cover Sheet filed in this matter, but Power Integrations is moving concurrently to dismiss or transfer this matter to Delaware.

CAUSES OF ACTION

8. In reply to paragraph 8 of the Amended Complaint, Power Integrations realleges Paragraphs 1 through 7 above, as though fully set forth herein.

9. Power Integrations admits that U.S. Patent No. 5,264,719 (the “’719 Patent”) is entitled “*High Voltage Lateral Semiconductor Device*,” that the ’719 patent indicates on its face that it issued on November 23, 1993, and that the ’719 patent indicates on its face that it was assigned to Harris Corporation. Otherwise, Power Integrations lacks sufficient knowledge to admit or deny the allegations of Paragraph 9 of the Amended Complaint, and therefore denies those allegations.

10. Power Integrations lacks sufficient knowledge to admit or deny the allegations of Paragraph 10 of the Amended Complaint, and therefore denies those allegations.

11. Power Integrations lacks sufficient knowledge to admit or deny the allegations of Paragraph 11 of the Amended Complaint, and therefore denies those allegations.

12. Power Integrations lacks sufficient knowledge to admit or deny the allegations of Paragraph 12 of the Amended Complaint, and therefore denies those allegations.

13. Power Integrations specifically denies that Fairchild has the right to assert the ’719 patent against Power Integrations. Otherwise, Power Integrations lacks sufficient knowledge to admit or deny the allegations of Paragraph 13 of the Amended Complaint, and therefore denies those allegations.

14. Power Integrations specifically denies that Fairchild has the right to assert the ’719 patent against Power Integrations. Otherwise, Power Integrations lacks sufficient knowledge to admit or deny the allegations of Paragraph 14 of the Amended Complaint, and therefore denies those allegations.

15. Power Integrations denies the allegations in Paragraph 15 of the Amended Complaint.

16. Power Integrations denies the allegations in Paragraph 16 of the Amended Complaint.

17. Power Integrations denies the allegations in Paragraph 17 of the Amended Complaint.

AFFIRMATIVE DEFENSES

18. In addition to any affirmative defenses described below, Power Integrations specifically reserves the right to allege any additional affirmative defenses as they become known through the course of discovery.

First Affirmative Defense **(Non-Infringement)**

19. Power Integrations does not infringe and has not infringed (literally, under the doctrine of equivalents, contributorily, or by inducement) any valid and enforceable claim of the '719 patent.

Second Affirmative Defense **(Invalidity)**

20. The '719 Patent is invalid because each fails to satisfy the conditions for patentability specified in Title 35 of the United States Code, including but not limited to sections 102, 103 and 112.

Third Affirmative Defense **(Unenforceability-Estoppel)**

21. Plaintiffs are barred by the doctrine of equitable estoppel from enforcing the '719 Patent against Power Integrations.

Fourth Affirmative Defense **(Unenforceability-Unclean Hands)**

22. Plaintiffs are barred by Plaintiffs' unclean hands from enforcing the '719 Patent against Power Integrations.

Fifth Affirmative Defense
(Unenforceability-Laches)

23. Plaintiffs are barred by the doctrine of laches from enforcing the '719 Patent against Power Integrations.

Sixth Affirmative Defense
(Unenforceability-Patent Misuse)

24. Plaintiffs' claims against Power Integrations are barred by Plaintiffs' patent misuse.

WHEREFORE, Power Integrations prays for judgment as follows:

1. That Plaintiffs' Amended Complaint be dismissed with prejudice;
2. That Plaintiffs take nothing by reason of their Amended Complaint;
3. That the '719 Patent, and all of its claims, be adjudged and declared invalid, unenforceable, and not infringed by Power Integrations;
4. That Plaintiffs, and all persons acting on their behalf or in concert with them, be permanently enjoined and restrained from charging, orally, or in writing that the '719 Patent is infringed by Power Integrations, directly or indirectly;
5. That the Court find this action exceptional under 35 U.S.C. § 285 and award Power Integrations its costs, expenses and reasonable attorney fees incurred as a result of this action; and
6. That Power Integrations be awarded such other and further relief as the Court may deem appropriate.

JURY DEMAND

Power Integrations demands a trial by jury of any issues triable of right by a jury.

Dated: June 19, 2006

Respectfully submitted,

FISH & RICHARDSON P.C.

By: /s/ Michael E. Jones

Michael E. Jones
State Bar No. 10929400
mikejones@potterminton
POTTER MINTON
A Professional Corporation
110 N. College, Suite 500
Tyler, TX 75702
Telephone: (903) 597-8311
Facsimile: (903) 593-0846

OF COUNSEL
Frank E. Scherkenbach
Scherkenbach@fr.com
FISH & RICHARDSON
225 Franklin Street
Boston, MA 02110-2804
Tel: 617-542-5070
Fax: 617-542-8906

Attorneys for Defendant
POWER INTEGRATIONS, INC.

CERTIFICATE OF SERVICE

The undersigned hereby certifies that all counsel of record who are deemed to have consented to electronic service are being served with a copy of this document via the Court's CM/ECF system per Local Rule CV-5(a)(3) on June 19, 2006. Any other counsel of record will be served by facsimile transmission and first class mail.

/s/ Michael E. Jones

Michael E. Jones

UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

FAIRCHILD SEMICONDUCTOR
CORPORATION, a Delaware corporation,
and INTERSIL CORPORATION, a
Delaware corporation,

Plaintiffs,

v.

POWER INTEGRATIONS, INC., a
Delaware corporation,

Defendants.

C.A. No. 2:06-CV-151 (TJW)

**POWER INTEGRATIONS' MOTION TO DISMISS OR, IN THE ALTERNATIVE, TO
TRANSFER THIS CASE TO DELAWARE**

Fairchild does not have standing to prosecute this case because it does not own U.S. Patent No. 5,264,719 ("the '719 patent") and is not the exclusive licensee of the patent. Fairchild's recent efforts to buy a cause of action on the '719 patent from Intersil are insufficient as a matter of law, and no amount of hand-waving on the part of the plaintiffs can cure that fatal defect. Therefore, pursuant to Rule 12(b)(1) of the Federal Rules of Civil Procedure, Power Integrations hereby moves to dismiss this case for lack of standing.

In the alternative, Power Integrations asks that the Court transfer this action to the District of Delaware, where the parties are already engaged in a dispute regarding the '719 patent. Specifically, the parties are seeking to determine whether the '719 patent was conceived before a Power Integrations patent asserted in the Delaware action. The Delaware case is set for trial this year, and all parties in the present suit are involved in the Delaware matter—Power

Integrations is the Delaware plaintiff, Fairchild Semiconductor is the defendant, and Intersil is a third party alleging prior inventorship and working with Fairchild to attempt to prove prior inventorship. As a result, this District is not the proper venue in which to address the '719 patent.

I. FACTUAL BACKGROUND

On October 20, 2004, Power Integrations, Inc. ("Power Integrations") filed suit against Fairchild Semiconductor International, Inc. and Fairchild Semiconductor Corporation (collectively "Fairchild") in the District Court for the District of Delaware, alleging infringement of four U.S. patents. [See Declaration of Mike Jones ("Jones Decl.") Ex. A.¹] Fairchild claims that one of the four patents, U.S. Patent No. 4,811,075 ("the '075 patent"), is invalid in view of the '719 patent, the only patent asserted in this case. Fairchild and Power Integrations have taken extensive discovery with respect to the '719 patent in the Delaware action, and the dispute in Delaware turns on who was the first to invent the technology in the '075 and '719 patents. A Delaware jury will resolve this critical issue later this year, as the trial on validity issues is set to begin on December 4. [Ex. B (Pretrial Conference Tr.) at 30-31.]

During the course of the Delaware litigation, Fairchild bought a license "to enforce" the '719 patent against a single entity: Power Integrations. [See Fairchild's Amended Complaint ("Amended Complaint") Ex. E.] By the terms of the March 30, 2006 agreement, Intersil granted Fairchild "the sole and exclusive right . . . to assert, litigate and prosecute claims of [i]nfringement under the ['719] patent[] against [Power Integrations]." [Amended Complaint Ex. E (Patent License Agreement of Mar. 30, 2006 ("PLA")) at §§ 1.2, 3.1.] However, Fairchild's hunting license does not provide any underlying right beyond the right to sue—it

¹ All citations are to the accompanying Declaration of Mike Jones, unless noted otherwise.

does not grant Fairchild the exclusive right to make, use, or sell the alleged invention of the '719 patent.²

On April 11, 2006, Fairchild issued a press release announcing the license and the institution of this suit, noting that Fairchild “recently secured exclusive rights to assert the [’719] patent against Power Integrations.” [Ex. C (April 11, 2006 Press Release – *Fairchild Semiconductor Files Patent Infringement Lawsuit Against Power Integrations, Inc.*)] On May 18, 2006, Intersil and Fairchild executed a Supplemental Agreement attempting to modify the PLA to make yet another entity, Intersil Americas, the original party to the PLA. [Amended Complaint Ex. F (Agreement of May 18, 2006).] None of these actions conferred standing on Fairchild.

II. LEGAL AUTHORITY

To have standing to assert patent infringement, “the plaintiff must demonstrate that it held enforceable title to the patent at the inception of the lawsuit.” *Paradise Creations, Inc. v. U V Sales, Inc.*, 315 F.3d 1304, 1308 (Fed. Cir. 2003). Where the plaintiff lacks a cognizable injury at the time it filed suit, such defect in standing cannot be cured after the inception of the lawsuit. *Id.* at 1310. In order to bring an action for damages resulting from infringement, the patentee must not only have legal title to the patent, but must have been its owner at the time of the infringement. *Crown Die & Tool Co. v. Nye Tool & Machine Works*, 261 U.S. 24, 49 (1923); *Arachnid, Inc. v. Merits Indus., Inc.*, 939 F.2d 1574, 1579 (Fed. Cir. 1991) (“[O]ne seeking to recover money damages for infringement of a United States patent . . . must have held legal title to the patent during the time of the infringement.”); *Heidelberg Harris, Inc. v. Loebach*, 145 F.3d 1454, 1458 (Fed. Cir. 1998) (“[A] plaintiff cannot sue for patent infringement occurring prior to

² As part of a broader cross-license with Intersil, Fairchild took a license to practice the '719 patent in certain limited capacities several years ago. But that license is not exclusive and, as Fairchild has implicitly acknowledged by entering into at least two later agreements specific to the '719 and Power

the time the plaintiff actually obtained legal title to the asserted patent.”); *Mas-Hamilton Group v. Lagard, Inc.*, 156 F. 3d 1206, 1210 (Fed. Cir. 1998) (only the holder of legal title to a patent at the time of the infringement can bring an action for damages resulting from that infringement) (dictum).

A patentee may divide its “bundle of rights” and convey, or share, the right to sue infringers. The patentee may, by instrument in writing, assign, grant, convey (1) the entire patent, (2) an undivided part or share of the entire patent, or (3) all rights under the patent in a specified geographical region. *Waterman v. Mackenzie*, 138 U.S. 252, 255 (1891). Such transfers constitute an assignment, and they vest the assignee with title in the patent and a right to sue infringers, either as sole plaintiff or as co-plaintiff depending on the nature and extent of the rights conferred. *Id.* However, a transfer of less than one of these three interests is a mere license, giving the licensee no title in the patent, and no right to sue for infringement in the licensee’s own name. *Id.* Fairchild has none of these three interests.

A narrow exception to the rule that only patentees and successors in interest may sue for infringement applies when a party obtains an exclusive license to a patent and holds “all substantial rights” under the patent. *See Textile Mead Productions, Inc. v. Mead Corp.*, 134 F.3d 1481, 1483-85 (Fed. Cir. 1998); *Vaupel Textilmaschinen KG v. Meccanica Euro Italia S.P.A.*, 944 F.2d 870, 875 (Fed. Cir. 1991). To establish independent standing as an exclusive licensee, though, a party must have received both the right to exclude others from making, using or selling the patented technology and the patent holder’s promise that no other party may practice the patented technology. *Rite-Hite Corp. v. Kelley Co.*, 56 F.3d 1538, 1552 (Fed. Cir. 1995).

Integrations, has no bearing on the instant dispute. Plaintiffs have not asserted—and cannot assert—that the earlier Fairchild-Intersil license in any way confers standing in this case.

However, this narrow exception does not apply to non-exclusive licensees; even if the patent holder is a party to the suit, a non-exclusive licensee does not have independent standing to sue for infringement. *Kalman v. Berlyn Corp.*, 914 F.2d 1473, 1481-82 (Fed. Cir. 1990) (stating a non-exclusive licensee lacks standing to sue for infringement even if joined with the patent holder and further noting that no “licensee who joins the patentee [has] standing to sue an infringer”). Furthermore, a non-exclusive licensee who has not been granted the right to exclude others has no legally recognized interest that would entitle it to bring or join an infringement action. *Abbott Lab. v. Diamedix Corp.*, 47 F.3d 1128, 1131 (Fed. Cir. 1995). A licensee may only bring an infringement suit to protect a property interest it received from the patentee. *See Ortho Pharmaceutical Corp. v. Genetics Institute, Inc.*, 52 F.3d 1026, 1034 (1995) (“[I]t is the licensee’s beneficial ownership of a right to prevent others from making, using, or selling the patented technology that provides the foundation for co-plaintiff standing.”). Thus, a contract clause cannot by itself grant standing to a licensee if the licensee would otherwise not have standing to bring the suit. *Id.* (“[A] right to sue clause cannot negate the requirement that . . . a licensee must have beneficial ownership of some of the patentee’s proprietary rights.”).

II. ARGUMENT

A. Fairchild Does Not Have Standing and Cannot Sue Power Integrations on the ’719 Patent.

Fairchild has no standing to sue for infringement because Fairchild is not, and never was, the patentee or successor in interest to the ’719 patent, and at no time has Fairchild held all substantial rights to the patent. Patent standing rules are strict: a party seeking to recover for alleged patent infringement must either have held legal title to the patent at the time of the alleged infringement, or have been assigned the right to recover for that infringement by the legal

title holder together with an assignment of all substantial rights under the patent. *Crown Die & Tool Co.*, 261 U.S. at 49; *Ortho Pharm.*, 52 F.3d at 1034. Only a patentee may bring an action for patent infringement, and Fairchild is not the patentee. Legal title appears to have been held at all times by Intersil, making Intersil the only party with any right to recover for alleged patent infringement, regardless of Fairchild's purported "license to enforce" the patent against Power Integrations.

To overcome the rule that only patentees and successors in interest may sue for infringement, Fairchild would need an exclusive license and to demonstrate a sufficient proprietary injury to one of the rights that flows from the patent. *Rite-Hite*, 56 F.3d at 1552. In essence, though, Fairchild has a "bare license," because it has no exclusive right to keep others from making, using, or selling products making use of the patented technology, and Fairchild suffers no legally cognizable harm when a third-party makes, uses, or sells the patented technology. *See Abbott*, 47 F.3d at 1131. As noted above, a bare licensee has no standing at all. *See Rite-Hite*, 56 F.3d at 1552; *Ortho Pharm.*, 52 F.3d at 1034. Fairchild therefore has no legally recognized interest that entitles it to bring or join an infringement action.

Intersil's contractual grant of the "exclusive right to sue" is not sufficient to confer standing to Fairchild. "A patentee may not give a right to sue to a party who has no proprietary interest in the patent." *Ortho Pharm.*, 52 F.3d at 1034 (collecting cases describing non-exclusive licensees lack standing to enforce a patent); *Rite-Hite*, 56 F.3d at 1553. *See also Phila. Brief Case Co. v. Specialty Leather Prods. Co.*, 145 F. Supp. 425, 429-30 (D.N.J. 1956), *aff'd*, 242 F.2d 511 (3rd Cir. 1957) (contract clause cannot give right to sue where licensee would otherwise have no such right). The Patent License Agreement attempts to convey to Fairchild "the sole and exclusive right . . . to assert, litigate and prosecute claims of [i]nfringement under

the ['173 and '719] patents against [Power Integrations]" [Amended Complaint Ex. E (Patent License Agreement of Mar. 30, 2006) at §§ 1.2, 3.1], but the license agreement simply cannot supersede the legal requirement that the licensee have all substantial rights in order to have standing to sue for infringement.

Moreover, Intersil's presence in this suit does not overcome Fairchild's lack of independent standing. Adding the patent holder as a co-plaintiff would only defeat a challenge on the grounds of standing if Fairchild had the exclusive rights to make, use and sell the patented technology, *Abbott*, 47 F.3d at 1131, but as Fairchild does not have such exclusive rights, it lacks standing to bring a cause of action for infringement. The Court should therefore dismiss this action for lack of standing.

B. If the Court Does Not Dismiss This Action, It Should Transfer the Case to Delaware to Be Resolved In The Court Which is Already Addressing the Patent-in-Suit.

In the alternative, Power Integrations asks the Court to transfer this action to the United States District Court for the District of Delaware, where a previously filed case involving the same parties and an identical dispute regarding who was first to invent the technology is already pending. As noted above, the parties are already involved in a case pending in the District of Delaware regarding the same patent and technology as the present lawsuit. There is a substantial overlap between this action and the Delaware case set for trial this December, as the outcome of both suits depends on the Delaware case's inventorship findings. Both the Fifth Circuit and the Federal Circuit both follow a first-to-file rule for cases having substantial overlap. Further, the interest of justice suggests transfer under the federal venue statute. Therefore, if the Court does not dismiss this case outright, it should transfer to the matter to Delaware.

1. The Key Issue With Respect to the Sole Patent-in-Suit, an Inventorship Dispute, is Already Before the Delaware Court.

In support of its invalidity claim with respect to the '075 patent in Delaware, Fairchild asserted that the '719 patent, the only patent in this case, is key invalidating prior art to the '075 patent. [Ex. D (Fairchild Rog response).] Fairchild and Power Integrations have taken extensive discovery with respect to the '719 patent, and the dispute in Delaware turns on who was the first to invent the technology in the '075 and '719 patents. The Delaware Jury will resolve this critical issue later this year.

The '719 Patent was filed on May 24, 1991, over four years after the '075 Patent's April 1987 filing date. During prosecution of the '719 patent, the Applicant copied large portions of the claims of the '075 patent into the '719 patent. [Ex. E ("[A]lthough not identically copied, [the claim] is considered to be generic to the invention defined in claim 1 of U.S. Patent No. 4,811,075 to Eklund." (underlining in original)).] A brief comparison of claim 8 of the '719 Patent to claim 1 of the '075 Patent demonstrates this copying of the '075 patent claim language. [Appendix 1; Ex. F-G.] Thus, the same questions regarding conception and inventorship that are central to the Delaware trial would also arise in this suit.

2. The First-To-File Rule Compels the Transfer of This Case.

In patent cases, "the forum of the first-filed case is favored, unless considerations of judicial and litigant economy, and the just and effective disposition of disputes, require otherwise." *Genentech, Inc. v. Eli Lilly & Co.*, 998 F.2d 931, 937 (Fed. Cir. 1993), *overruled on other grounds*, *Wilton v. Seven Falls, Inc.*, 515 U.S. 277 (1995); *accord Save Power Ltd. v. Syntek Fin. Corp.*, 121 F.3d 947, 950 (5th Cir. 1997) ("The Fifth Circuit adheres to the general rule that the court in which an action is first filed is the appropriate court to determine whether

subsequently filed cases involving substantially similar issues should proceed.”) The Federal Circuit regards the application of the first-to-file rule as an issue that “is important to national uniformity in patent practice.” *Genentech*, 998 F.2d at 937. Application of the rule requires a three-part analysis by the court in a later-filed action:

1. The court must confirm that the case before it was filed later than an earlier case in another district. *Genentech*, 998 F.2d at 937; *accord Syntek*, 121 F.3d at 950-51.
2. The court must then determine whether the earlier-filed case is likely to raise issues that substantially overlap with the case on its own docket. *Syntek*, 121 F.3d at 950-51.
3. If so, the court must transfer the action before it to the first-filed court unless it finds that it would be “unjust or inefficient” to do so. *Genentech*, 998 F.2d at 938; *accord Mann Mfg., Inc. v. Hortex, Inc.*, 439 F.2d 403 (5th Cir. 1971) (transfer required absent “compelling” reasons to favor later action).

After the second case is transferred, the first-filed court decides whether that later action “must be dismissed, stayed, or transferred and consolidated.” *Sutter Corp. v. P&P Indus., Inc.*, 125 F.3d 914, 920 (5th Cir. 1997). In favoring transfer of related cases, the rule is designed to avoid the waste and duplication that would result from piecemeal resolution of similar issues. *West Gulf Maritime Assoc. v. ILA Deep Sea Local 24*, 751 F.2d 721, 728-29 (5th Cir. 1985); *cf. Optical Recording Corp. v. Capitol-EMI Music, Inc.*, 803 F. Supp. 971 (D. Del. 1992) (proceeding with later-filed case because the Delaware court was already familiar with the technology and patents at issue in both cases).

a. The Delaware Action Is The First-Filed Action

Power Integrations filed suit against Fairchild on October 20, 2004, in Delaware, over 17 months before the current action was brought. Fairchild has not only answered the complaint in the Delaware case, but the parties have already conducted extensive discovery, are finished with

claim construction, and have completed technical expert discovery. In fact, the parties recently had a pre-trial conference, and the Delaware Court provided trial dates for later this year (September for some issues and December for others). [Ex. B at 30-31.]

b. There Is Substantial Overlap in the Subject Matter of the Patents at Issue.

Cases do not need to have exactly the same subject matter to meet the “substantial overlap” test. “[R]egardless of whether or not the suits . . . are identical, if they overlap on the substantive issues, the cases would be required to be consolidated in . . . the jurisdiction first seized of the issues.” *Mann*, 439 F.2d at 408 n.6; *see also Syntek*, 121 F.3d at 950 (“The rule does not, however, require that cases be identical.”)

The Fifth Circuit has previously addressed the meaning of “substantial overlap” in the context of patent litigation in *Mann Manufacturing, Inc. v. Hortex, Inc.*, 439 F.2d 403 (5th Cir. 1971). There, Mann sued in the Southern District of New York seeking a declaratory judgment that a number of its products did not infringe a patent owned by Hortex. *Id.* at 405. After Mann commenced that action, Hortex sued Mann in the Western District of Texas, alleging that Mann infringed a different patent owned by Hortex. *Id.* at 405-406. The Fifth Circuit acknowledged that these two cases involved distinct patents with unique claims, where the “issues of validity and infringement involving a matching of prior art disclosures and accused practices with the elements of the differing claims of each patent” might differ. *Id.* at 407. Despite the difference in patent claims, the Court held that the cases shared substantial issues, including the questions about the sufficiency of disclosures made to the Patent Office and about the lack of inventorship of the patentee, and found transfer of the later-filed action was warranted. *Id.* at 407-08.

Here, the Delaware and Texas cases bear even more similarities than in *Mann*, as both cases address the same technology and share disputes regarding nearly identical claims. The similarity is particularly evident when comparing claim 8 from the '719 Patent against claim 1 of the '075 Patent (shown side-by-side in Appendix 1). The parties have taken extensive fact and expert discovery on the question of inventorship in the Delaware case, and the Court has already issued a claim construction order in the Delaware case. [Ex. H (Claim Construction Order).] The identical question of inventorship, likely determinative for validity purposes, will be decided at trial in Delaware later this year on the basis of the same fact witnesses, documents, and expert testimony that would apply here. As such, to proceed with both the Texas and Delaware cases separately would result in precisely the kind of wasteful duplication of time and effort that the first-to-file rule is designed to prevent. *West Gulf*, 751 F.2d at 729 (“The concern manifestly is to avoid the waste of duplication . . . and to avoid piecemeal resolution of issues that call for a uniform result.”). Allowing this case to proceed in Texas would also risk conflicting outcomes on a single issue. To avoid this confusion and injustice, Power Integrations asks this Court to transfer the action to Delaware.

c. There Are No Compelling Circumstances That Justify Disregarding the First-To-File Rule

Once the first-to-file rule applies, the issues should be decided in the first-filed suit, unless it would be “unjust or inefficient” to do so. *Genentech*, 998 F.2d at 938. In deciding whether justice and efficiency require disregarding the first-to-file rule, the Federal Circuit considers such factors as: (1) the convenience and availability of witnesses, (2) the absence of jurisdiction over all parties, (3) the possibility of consolidation with related litigation, and (4)

whether the first-filed case involves the real parties in interest. As discussed below, none of these factors weighs against transfer to Delaware.

First, the convenience and availability of witnesses do not favor the Eastern District of Texas. All three parties in this case are Delaware corporations, with their principal places of business alleged to be in either California or Maine. All of the patents in question, including those from the Delaware case, list the inventors' residence as either California or Florida. In fact, Power Integrations is not aware of a single fact witness that is located in the state of Texas.

Second, there are no jurisdictional reasons to disregard the first-to-file rule. Not only are Fairchild and Intersil Delaware corporations, but Fairchild also answered and counterclaimed in the Delaware case without asserting a defense based on a lack of personal jurisdiction or on the inconvenience of that forum. As such, Fairchild has agreed to jurisdiction and waived any right to object. *See Golden v. Cox Furniture Mfg. Co., Inc.*, 683 F.2d 115, 118 (5th Cir. 1982) (party waives right to object to personal jurisdiction if it does not make motion under Rule 12 or assert defense in answer); *see also* Fed. R. Civ. P. 12(h)(1). Intersil responded to subpoenas in the Delaware case and, as a Delaware corporation, cannot contest personal jurisdiction in Delaware.

The third factor also provides no basis for declining this transfer request, as there is no related litigation in the Eastern District of Texas with which the two actions could be consolidated. In fact, the opposite is true. As to the fourth factor, whether the first-filed case involves the real parties in interest, defendants will likely argue that Intersil is not a party to the Delaware action. However, Intersil has been working with Fairchild in Delaware case, shares local counsel with Fairchild in Delaware, and has produced documents and things related to the '719 patent in Delaware. Intersil has also participated in and paid the inventor of the '719 patent to sit for a deposition, in addition to preparing and presenting alleged corroborating witnesses on

the '719 patent. As such, Intersil has been an active participant in the Delaware litigation and is well aware that the inventorship contest between the '075 patent and the '719 patent will be decided in the Delaware case.

3. The Interest of Justice Requires Hearing this Action in Delaware.

Even if this Court does not transfer using the first-to-file rule, it should transfer the case to the District of Delaware because it is a more convenient and cost effective place to resolve the instant dispute. The potential for inconsistent rulings from the Plaintiff's forum shopping imposes significant inconvenience to Power Integrations, and the public at large, in the form of uncertainty. Further, having presided over the Delaware case, the District of Delaware will be intimately familiar with the technology and issues in the present suit, including specifically the inventorship contest, which Plaintiffs apparently want to challenge all over again here. In addition, the need to re-litigate the inventorship contest imposes an inconvenience and burden on Power Integrations.

a. Cases are Transferred at the Court's Discretion, Focusing on Convenience and Justice.

A district court may transfer any civil case "[f]or the convenience of parties and witnesses, in the interest of justice, . . . to any other district or division where it might have been brought." 28 U.S.C. § 1404(a). As the Fifth Circuit has noted, Section 1404(a) is "a statute which codifies (with some amendment) the common law doctrine of forum non conveniens." *Castanho v. Jackson Marine, Inc.*, 650 F.2d 546, 550 (5th Cir.1981). In exercising its discretion to transfer a pending case, courts consider "all relevant factors to determine whether or not on balance the litigation would more conveniently proceed and the interests of justice be better

served by transfer to a different forum.” *Peteet v. Dow Chemical Company*, 868 F.2d 1428, 1436 (5th Cir.) (internal quotations and citations omitted), cert. denied, 439 U.S. 935 (1989).

b. Both Convenience and Justice Favor Transfer to Delaware.

The potential for inconsistent findings imposes a great inconvenience on Power Integrations and the public at large. The Delaware case will proceed to judgment first, and that judgment is *res judicata*. Because the parties can rely on the Delaware court’s findings, in particular the determination on the inventorship issue, all preparations made meanwhile to re-litigate the issues in this District would be wasted. Absent such consistent treatment, it could take years to untangle the various issues presented with multiple constructions and inventorship contentions on these related patents. Indeed, given the stage of the Delaware case, it is likely that issues from that case would be pending on appeal at the same time that plaintiffs ask this Court to decide those same issues. The public would have no idea what it could and could not do in this field.

Moreover, plaintiffs have known for over a year that inventorship would be decided in the Delaware case, and they could have filed a counterclaim asserting the ’719 patent against Power Integrations early in the Delaware case. Instead, they chose to wait until the Delaware case was nearly completed, and then filed this suit in another forum, despite the fact that rulings and findings from the Delaware case are important, and in some cases determinative, in their present suit.

Finally, having presided over the Delaware case, the District of Delaware will be intimately familiar with the technology and issues in the present suit, including specifically claim constructions and the inventorship contest. The Delaware court will also be in the best position to decide evidentiary issues such as what evidence, rulings, and stipulations from the old case

may be employed in what ways in the present suit. This Court should therefore transfer the instant case to Delaware under Section 1404(a), to the extent it does not do so under the first-filed rule or does not dismiss the suit outright for lack of standing.

III. CONCLUSION

For the reasons stated above, this Court should grant Power Integrations' motion to dismiss for lack of standing or, in the alternative, transfer the case to Delaware to be resolved by a Court already dealing with the '719 patent and familiar with the technology at issue in both cases.

Dated: June 19, 2006

Respectfully submitted,

OF COUNSEL

Frank E. Scherkenbach
Fish & Richardson P.C.
225 Franklin Street
Boston, Massachusetts 02110-2804
Telephone: (617) 542-5070
Facsimile: (617) 542-8906

By: /s/ Michael E. Jones
Michael E. Jones
State Bar No. 10929400
mikejones@potterminton
POTTER MINTON
A Professional Corporation
110 N. College, Suite 500
Tyler, TX 75702
Telephone: (903) 597-8311
Facsimile: (903) 593-0846

Attorneys for Defendant
POWER INTEGRATIONS, INC.

CERTIFICATE OF SERVICE

The undersigned hereby certifies that all counsel of record who are deemed to have consented to electronic service are being served with a copy of this document via the Court's CM/ECF system per Local Rule CV-5(a)(3) on June 19, 2006. Any other counsel of record will be served by facsimile transmission and first class mail.

/s/ Michael E. Jones

Michael E. Jones

UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS

FAIRCHILD SEMICONDUCTOR
CORPORATION, a Delaware corporation,
INTERSIL AMERICAS, INC., a Delaware
corporation and INTERSIL CORPORATION,
a Delaware corporation
Plaintiffs,

v.

POWER INTEGRATIONS, INC., a Delaware
corporation.
Defendant

2:06cv-151 (TJW)

**DECLARATION OF MICHAEL E. JONES IN SUPPORT OF POWER
INTEGRATIONS, INC.'S MOTION TO DISMISS, OR IN THER ALTERNATIVE, TO
TRANSFER THIS CASE TO DELAWARE**

I, Michael E. Jones, declare same based upon information and belief:

1. I am a shareholder at Potter Minton PC in Tyler, Texas. I am one of the attorneys representing defendant Power Integrations, Inc. in the above-captioned matter filed by Plaintiffs Fairchild Semiconductor Corporation ("Fairchild"), Intersil Americas, Inc. and Intersil Corporation ("Intersil").

2. Attached hereto as Exhibit "A" is a true and correct copy of the First Amended Complaint for Patent Infringement filed by Power Integrations against Fairchild Semiconductor Corporation and Fairchild Semiconductor International, Inc. in the United States District Court for the District of Delaware on June 30, 2005 ("the Delaware Lawsuit").

3. I am informed and believe that attached hereto as Exhibit "B" is a true and correct copy of the transcript of the Pretrial Conference held on May 31, 2006 in the Delaware Lawsuit.

4. I am informed and believe that attached hereto as Exhibit "C" is a true and correct copy of Fairchild's press release dated April 11, 2006.

5. I am informed and believe that attached hereto as Exhibit "D" is a true and correct copy of a claim chart regarding the '719 patent asserted in this case which is part of Fairchild's invalidity contentions in the Delaware case as set forth in its Supplemental Responses to Power Integrations' First Set of Interrogatories, dated June 30, 2005.

6. I am informed and believe that attached hereto as Exhibit "E" is a true and correct copy of an excerpt from the '719 file history concerning the '075 patent claim language.

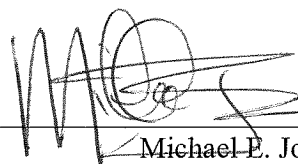
7. I am informed and believe that attached hereto as Exhibit "F" is a true and correct copy of the '719 Patent.

8. I am informed and believe that attached hereto as Exhibit "G" is a true and correct copy of the '075 Patent.

9. I am informed and believe that attached hereto as Exhibit "H" is a true and correct copy of Claim Construction Order issued on March 31, 2006 in the Delaware Lawsuit.

I declare under penalty of perjury that the foregoing is true and correct to the best of my information and belief.

Signed: June 19, 2006



Michael E. Jones

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

POWER INTEGRATIONS, INC., a
Delaware corporation,

Plaintiff,

v.

FAIRCHILD SEMICONDUCTOR
INTERNATIONAL, INC., a Delaware
corporation, and FAIRCHILD
SEMICONDUCTOR CORPORATION, a
Delaware corporation

Defendants.

C.A. No. 047-1371-JJF

JURY TRIAL REQUESTED

FIRST AMENDED COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Power Integrations, Inc. hereby alleges as follows:

THE PARTIES

1. Power Integrations, Inc. (“Power Integrations”) is incorporated under the laws of the state of Delaware, and has a regular and established place of business at 5245 Hellyer Avenue, San Jose, California, 95138.

2. Upon information and belief, defendant Fairchild Semiconductor International, Inc. is incorporated under the laws of the state of Delaware, with its headquarters located at 82 Running Hill Road, South Portland, Maine, 04106. Upon information and belief, defendant Fairchild Semiconductor Corporation is incorporated under the laws of the state of Delaware, with its headquarters located at 82 Running Hill Road, South Portland, Maine, 04106. (Fairchild Semiconductor International, Inc. and Fairchild Semiconductor Corporation hereinafter collectively “Fairchild Semiconductor.”)

JURISDICTION AND VENUE

3. This action arises under the patent laws of the United States, Title 35 U.S.C. § 1 *et seq.* This Court has subject matter jurisdiction under 28 U.S.C. §§ 1331 and 1338(a).

4. Upon information and belief, this Court has personal jurisdiction over defendants because defendants are incorporated, doing business and advertising in this judicial District.

5. Upon information and belief, venue is proper in this Court pursuant to 28 U.S.C. §§ 1391(b), (c) and 1400 because the defendants are subject to personal jurisdiction in this judicial District.

GENERAL ALLEGATIONS

6. Power Integrations' products include its integrated pulse width modulation ("PWM") integrated circuits that are used in power supplies for electronic devices such as cellular telephones, LCD monitors and computers. These products are sold throughout the United States, including Delaware.

7. Upon information and belief, defendants manufacture PWM integrated circuits devices (e.g., devices intended for use in power conversion applications such as LCD monitor power supplies or battery chargers for portable electronics), and directly and through their affiliates, uses, imports, sells, and offers to sell the same throughout the United States, including Delaware.

FIRST CAUSE OF ACTION

INFRINGEMENT OF U.S. PATENT NO. 6,107,851

8. The allegations of paragraphs 1-7 are incorporated as though fully set forth herein.

9. Power Integrations is now, and has been since its issuance, the assignee and sole owner of all right, title, and interest in United States Patent No. 6,107,851, entitled "Offline Converter with Integrated Softstart and Frequency Jitter" ("the '851

patent”), which was duly and legally issued on August 22, 2000. A true and correct copy of the ’851 patent is attached hereto as Exhibit A.

10. Upon information and belief, defendants have been and are now infringing, inducing infringement, and contributing to the infringement of the ’851 patent by making, using, importing, selling, and offering to sell devices, including PWM integrated circuit devices, and/or inducing or contributing to the importation, use, offer for sale and sale by others of such devices covered by one or more claims of the ’851 patent, all to the injury of Power Integrations.

11. Defendants’ acts of infringement have injured and damaged Power Integrations.

12. Defendants’ infringement has caused irreparable injury to Power Integrations and will continue to cause irreparable injury until defendants are enjoined from further infringement by this Court.

13. Upon information and belief, Defendants’ infringement has been, and continues to be, willful so as to warrant enhancement of damages awarded as a result of its infringement.

SECOND CAUSE OF ACTION

INFRINGEMENT OF U.S. PATENT NO. 6,249,876

14. The allegations of paragraphs 1-7 are incorporated as though fully set forth herein.

15. Power Integrations is now, and has been since its issuance, the assignee and sole owner of all right, title, and interest in United States Patent No. 6,249,876, entitled “Frequency Jittering Control for Varying the Switching Frequency of a Power Supply” (“the ’876 patent”), which was duly and legally issued on June 19, 2001. A true and correct copy of the ’876 patent is attached hereto as Exhibit B.

16. Upon information and belief, defendants have been and are now infringing, inducing infringement, and contributing to the infringement of the ’876 patent

by making, using, importing, selling, and offering to sell devices, including PWM integrated circuit devices and/or inducing or contributing to the importation, use, offer for sale and sale by others of such devices covered by one or more claims of the '876 patent, all to the injury of Power Integrations.

17. Defendants' acts of infringement have injured and damaged Power Integrations.

18. Defendants' infringement has caused irreparable injury to Power Integrations and will continue to cause irreparable injury until defendants are enjoined from further infringement by this Court.

19. Upon information and belief, Defendants' infringement has been, and continues to be, willful so as to warrant enhancement of damages awarded as a result of its infringement.

THIRD CAUSE OF ACTION

INFRINGEMENT OF U.S. PATENT NO. 6,229,366

20. The allegations of paragraphs 1-7 are incorporated as though fully set forth herein.

21. Power Integrations is now, and has been since its issuance, the assignee and sole owner of all right, title, and interest in United States Patent No. 6,229,366, entitled "Off-Line Converter with Integrated Softstart and Frequency Jitter" ("the '366 patent"), which was duly and legally issued on May 8, 2001. A true and correct copy of the '366 patent is attached hereto as Exhibit C.

22. Upon information and belief, defendants have been and are now infringing, inducing infringement, and contributing to the infringement of the '366 patent by making, using, importing, selling, and offering to sell devices, including PWM integrated circuit devices and/or inducing or contributing to the importation, use, offer for

sale and sale by others of such devices covered by one or more claims of the '366 patent, all to the injury of Power Integrations.

23. Defendants' acts of infringement have injured and damaged Power Integrations.

24. Defendants' infringement has caused irreparable injury to Power Integrations and will continue to cause irreparable injury until defendants are enjoined from further infringement by this Court.

25. Upon information and belief, Defendants' infringement has been, and continues to be, willful so as to warrant enhancement of damages awarded as a result of its infringement.

FOURTH CAUSE OF ACTION

INFRINGEMENT OF U.S. PATENT NO. 4,811,075

26. The allegations of paragraphs 1-7 are incorporated as though fully set forth herein.

27. Power Integrations is now, and has been since its issuance, the assignee and sole owner of all right, title, and interest in United States Patent No. 4,811,075, entitled "High Voltage MOS Transistors" ("the '075 patent"), which was duly and legally issued on March 7, 1989. A true and correct copy of the '075 patent is attached hereto as Exhibit D.

28. Upon information and belief, defendants have been and are now infringing, inducing infringement, and contributing to the infringement of the '075 patent by making, using, importing, selling, and offering to sell devices, including PWM integrated circuit devices and/or inducing or contributing to the importation, use, offer for sale and sale by others of such devices covered by one or more claims of the '075 patent, all to the injury of Power Integrations.

29. Defendants' acts of infringement have injured and damaged Power Integrations.

30. Defendants' infringement has caused irreparable injury to Power Integrations and will continue to cause irreparable injury until defendants are enjoined from further infringement by this Court.

31. Upon information and belief, Defendants' infringement has been, and continues to be, willful so as to warrant enhancement of damages awarded as a result of its infringement.

PRAYER FOR RELIEF

WHEREFORE, Plaintiff requests the following relief:

- (a) judgment against defendants as to willful infringement of the '851 patent;
- (b) judgment against defendants as to willful infringement of the '876 patent;
- (c) judgment against defendants as to willful infringement of the '366 patent;
- (d) judgment against defendants as to willful infringement of the '075 patent;
- (e) a permanent injunction preventing defendants and their officers, directors, agents, servants, employees, attorneys, licensees, successors, assigns, and customers, and those in active concert or participation with any of them, from making, using, importing, offering to sell or selling any devices that infringe any claim of the '851, '876, '366, or '075 patents;
- (f) judgment against defendants for money damages sustained as a result of defendants' infringement of the '851, '876, '366, and '075 patents;
- (g) that any such money judgment be trebled as a result of the willful nature of Defendants' infringement;
- (h) costs and reasonable attorneys' fees incurred in connection with this action pursuant to 35 U.S.C § 285; and
- (i) such other and further relief as this Court finds just and proper.

JURY DEMAND

Plaintiff requests trial by jury.

Dated: June 30, 2005

FISH & RICHARDSON P.C.

By: */s/ John F. Horvath*

William J. Marsden, Jr. (#2247)
Sean P. Hayes (#4413)
John F. Horvath (#4557)
919 N. Market Street, Suite 1100
P.O. Box 1114
Wilmington, DE 19801
Telephone: (302) 652-5070
Facsimile: (302) 652-0607

Frank E. Scherkenbach
225 Franklin Street
Boston, MA 02110-2804
Telephone: (617) 542-5070
Facsimile: (617) 542-8906

Michael Kane
60 South Sixth Street
3300 Dain Rauscher Plaza
Minneapolis, MN 55402
Telephone: (612) 335-5070
Facsimile: (612) 288-9696

Howard G. Pollack
Gina M. Steele
Michael R. Headley
500 Arguello Street, Suite 500
Redwood City, CA 94063
Telephone: (650) 839-5070
Facsimile: (650) 839-5071

Attorneys for Plaintiff
POWER INTEGRATIONS, INC.

*Power Intergrations, Inc. v.
Fairchild Semiconductor International, Inc.*

*Hearing
May 31, 2006*

*Hawkins Reporting Service
715 N King Street
Suite 3
Wilmington, DE 19801
(302) 658-6697*

*Original File 5PWRIN~1.TXT, 52 Pages
Min-U-Script® File ID: 3175811218*

Word Index included with this Min-U-Script®

Page 1

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE
POWER INTEGRATIONS, INC.,)
Plaintiff,)

v.)
FAIRCHILD SEMICONDUCTOR)
INTERNATIONAL, INC., and)
FAIRCHILD SEMICONDUCTOR)
CORPORATION,)

Defendants.)
United States District Court
844 King Street
Wilmington, Delaware
Wednesday, May 31, 2006
12:30 p.m.

BEFORE: THE HONORABLE JOSEPH J. FARNAN, JR.

United States District Court Judge

APPEARANCES:

SEAN P. HAYES, ESQ.
FRANK SCHERKENBACH, ESQ.
MICHAEL HEADLEY, ESQ.
FISH & RICHARDSON
For Power Integrations
G. HOPKINS GUY, ESQ.
ORRICLE, HERRINGTON

and
BAS DE BLANK, ESQ.
JOHN G. DAY, ESQ.
ASHBY & GEDDES
For Fairchild

Hawkins Reporting Service

715 North King Street - Wilmington, Delaware 19801
(302)658-6697 FAX(302)658-8418

Page 2

(302)658-6697 FAX(302)658-8418

3 1 THE COURT: Be seated, please.

[2] Good afternoon.

[3] (All respond: "Good afternoon.")

[4] THE COURT: I've reviewed the [5] proposed pretrial order, and this afternoon [6] I'll be entering an order that essentially [7] denies the motions for summary judgment and [8] also grants partial summary judgment to [9] Fairchild with regard to the damages evidence.

[10] If there's any questions about that [11] after you read it, you could write me a letter [12] and we'll try to explain essentially what it [13] boils down to, the discovery ruling and then [14] the setting of a date.

[15] With regard to the pretrial order, [16] I sound like a broken record sometimes at these [17] conferences, but you list witnesses, for [18] instance, on behalf of Power Integrations, you [19] have like seven people that you say are going [20] to testify and then there's a list that is a [21] little more extensive and there's the cryptic [22] statement that these folks may be called in [23] rebuttal, they may come to Wilmington for [24] lunch, I don't know what they're doing in the

Page 4

[1] pretrial order, but, you know, you got to [2] pretry the case.

[3] So what has to happen is both sides [4] have to — and it's important for the [5] allocation of time, you have to tell me who the [6] witnesses are going to be and

then I can make [7] decisions about whether there's too many, [8] they're accumulative, there's some question [9] about the offer of their testimony. But I need [10] to know exactly who the witnesses are going to [11] be and it would seem not illogical that they [12] would be — that they'd be listed in the order [13] you intend to call them and a little bit about [14] what they're going to say.

[15] There's no surprises in this case, [16] so there's no rebuttal witnesses, other than a [17] planned rebuttal witness to an answer, and I [18] call that more of an answering witness but it's [19] fairly characterized as a rebuttal witness. [20] But we would know who they are and it's just a [21] question of putting it on logically and [22] consistent with the order of proof so the jury [23] gets, well, this is what they said with the [24] burden and this is what they answered and this [25] (302)658-6697 FAX(302)658-8418

Page 5

[1] is our rebuttal or answer to that, but that has [2] to be set out.

[3] And then you know exhibits would be [4] — there's a certain volume of exhibits in a [5] patent case that I allow to come in just for [6] the record because you think you might need it [7] later on but they never get shown to the jury [8] and they're part of the pretrial order and [9] admitted in the record. But I really need to [10] know exactly the — and I never put lawyers to [11] this test, but, you know, sometimes you can [12] actually tell us with what witnesses they're [13] coming in and who's testifying about them but [14] maybe that's too difficult. But at least [15] you'll be able to say exactly what exhibits are [16] going to be presented with testimony before the [17] jury and that gives me some idea of how to make [18] decisions again about time, also about any [19] objections that may be offered. Both of those [20] are going to have to be tightened up in this [21] proposed order. And I guess depending on when [22] we pick a trial date I'll give you an amount of [23] time to get that done.

[24] With regard to the case, the

[25] (302)658-6697 FAX(302)658-8418

Page 6

[1] validity case, the invalidity case, I'm [2] seriously thinking about separating that from [3] infringement and damages. And without knowing [4] something that would be prejudicial or unduly [5] prejudicial, I'm inclined to do that.

[6] MR. GUY: If I may be heard on [7] that, Your Honor?

[8] THE COURT: Yes.

[9] MR. SPEAKER: We have suggested [10] bifurcation — Fairchild has sug-

gested. What [11] we would like to do there is because of some [12] issues that are ongoing right now with respect [13] to damages, we still have a number of [14] depositions to take. The experts have not been [15] deposed, the two damages experts. We need to [16] propound or provide a 30(B)6 deposition on U.S. [17] manufacturing, should be a limited deposition.

[18] Also, there has been an undisclosed [19] expert that — or unnamed expert that is [20] provided, expert reports in end of April, early [21] May, so that would tend to move that issue of [22] damages, all the damages related issues out.

[23] The other point though is that the [24] damages experts, particularly the plaintiff's

[25] (302)658-6697 FAX(302)658-8418

Page 7

[1] damages experts, relies upon Power Integrations [2] financial statements, their filings, annual [3] reports, and quarterly reports with the SCC.

[4] There is currently an ongoing [5] investigation apparently going on at Power [6] Integrations. They have not filed their 2005 [7] annual reports. They have notified the SCC [8] that all prior reports are unreliable. I want [9] to make that clear that all prior SCC reports, [10] annual reports, quarterly reports going back to [11] 1999 are unreliable. They'll need to be [12] restated. And in addition, Your Honor, they [13] expect to have those — according to the [14] information we have and it's not subject to [15] discovery, but they would have that information [16] to NASDAQ by August the 2nd. I don't know [17] whether they'll meet that or not.

[18] They have been up in front of the [19] NASDAQ board twice on delisting issues [20] regarding their failure to provide these [21] reports. So this is a fundamental issue that's [22] going on. The damages experts have relied upon [23] these. It relates to back dating of stock [24] options. It's our understanding that both the

[25] (302)658-6697 FAX(302)658-8418

Page 8

[1] chairman and the chief financial officer have [2] been fired related to this issue. We know that [3] they've resigned and left the company at the [4] same time this was going on. So this is a [5] material issue and, again, it all relates to [6] damages and I'd ask the Court to consider that [7] in terms of bifurcation in terms of pushing the [8] damages component off.

[9] Thank you, Your Honor.

[10] THE COURT: Thank you.

[11] MR. SCHERKENBACH: I didn't hear

[12] any substantive argument as to why the [13] issues couldn't be divided in the way you [14] suggest. I'm perfectly happy with that. It [15] makes quite a bit of sense to do it. So [16] infringement and damages in one trial, validity [17] in other. [18] I don't know if Your Honor has in [19] mind the same jury or different juries. I [20] might have some concerns if we're talking about [21] different juries or if there is a substantial [22] subrogation but I suppose we could talk about [23] that. [24] To respond to Mr. Guy's point, the [25] (302)658-6697 FAX(302)658-8418

Page 9

[1] further discovery is minor. The two damages [2] experts need to be deposed. We've been trying [3] to schedule that for some time. That will [4] happen shortly. [5] The witness Mr. Guy referred to [6] relating to Manufacturing, you may have seen [7] this, Your Honor, in the pretrial papers, but [8] there had been an issue in the case about the [9] extent to which Fairchild manufactured the [10] accused products in the U.S. Fairchild is [11] saying essentially they never did that and [12] Power Integrations is a little skeptical. [13] It turns out Mr. Kim, the elusive [14] Mr. Kim whose deposition we finally got, you [15] may recall you ordered that. He said, well, [16] actually, in fact, they did manufacture in the [17] U.S. This just came out in the last several [18] weeks. We were surprised because we've been [19] told the contrary. And Fairchild then went [20] back to the drawing board, investigated it and [21] said, yes, it turns out that several million of [22] the accused parts have in fact been [23] manufactured in the U.S. [24] So we agreed that as a result of [25] (302)658-6697 FAX(302)658-8418

Page 10

[1] that we now get at least one further deposition [2] on the extent to which the U.S. manufacturing [3] actually occurred. It's one deposition. There [4] will be some additional, I think, document [5] discovery that's required but it's not the sort [6] of thing that's going to cause any sort of [7] significant delay. [8] The financial statement point, if I [9] can comment on that. There's some truth [10] certainly what Mr. Guy is saying. On the other [11] hand, with all due respect, in our view is a [12] sideshow. It doesn't have anything to do with [13] the damages information that's relevant to this [14] case. [15] Yes, there are some SCC statements [16] and filings that are going to be revised. The [17] portions that the SCC filings were relied on by [18] either expert have nothing to do with stock [19] options, date of grants, so forth. That's [20]

really just a sideshow and shouldn't derail [21] what the scope is in the case. [22] **MR. GUY:** Your Honor, first of all [23] with respect to the U.S. manufacturing issue, [24] we were unaware that this was going on and what [25] (302)658-6697 FAX(302)658-8418

Page 11

[1] happened in that case is approximately single [2] digit percentage, five percent or so, certain [3] parts, one part in particular was manufactured [4] in the U.S. very, very briefly. [5] Mr. Kim's testimony was he did not [6] know whether there was U.S. manufacturing or [7] not; however, a document was produced during [8] that deposition and that's what triggered the [9] investigation. [10] With respect to the issue about the [11] stock option and issues like that, it has to do [12] with what their true expenses are. It has to [13] do with what their true costs in the case are [14] and they're claiming huge loss profits and huge [15] price erosion claims here basically over a [16] rather minor amount of U.S. sales. [17] Even if you take their numbers, I [18] think they say that 23 percent of our product [19] comes into the United State, and this is about [20] \$27 million worth of worldwide, so we're [21] talking about maybe \$6 million in the U.S. and [22] yet their damages claim is \$45 million to be [23] trebled to total some \$135 million. [24] **THE COURT:** So the damages claim, I [25] (302)658-6697 FAX(302)658-8418

Page 12

[1] thought I read, was like 5 or 6 million in lost [2] profits and then there was this price erosion [3] claim in twenties of million. [4] **MR. GUY:** Yes. [5] **THE COURT:** How does it get to 45 [6] million? Does that add up to something more? [7] **MR. GUY:** Yes, if you add it all up [8] it ends up being — the last page under Tab 2 [9] there's 5.9 million lost profits, lost profits, [10] damages and price erosion is 29, almost 30 [11] million, and reasonable royalty is another 6 [12] million. [13] **THE COURT:** Okay. [14] **MR. GUY:** So that's about 40 [15] million. [16] **THE COURT:** I was leaving out the [17] reasonable royalty because that wasn't [18] implicated in your argument about the relevance [19] of the cost factor of whatever is going on with [20] the filings. [21] **MR. GUY:** I think it does in terms [22] of a hypothetical negotiation about what a [23] reasonable buyer and reasonable seller would [24] come to about what

their true profit is. I [25] (302)658-6697 FAX(302)658-8418

Page 13

[1] think it would be relevant to that even for [2] reasonable royalty. Assuming that's correct, [3] we still have \$36 million in lost profits and [4] price erosion and their financial statements [5] clearly depend upon that. That's what they [6] are. They report their profit a loss. [7] With all due respect to [8] Mr. Scherkenbach, he can't stand up here and [9] tell you what the restatement will be, how much [10] will the amounts vary. All we know are the two [11] key members of Power Integrations have been [12] fired over this and that they have filed [13] statements with the SCC saying that it's going [14] to be material. [15] **THE COURT:** You're from a large [16] firm. This is 2006. This is corporate [17] America. [18] **MR. GUY:** Yes. [19] **THE COURT:** I don't mean to [20] belittle it, but a couple executives get fired, [21] a few restatements, a few false filings, I [22] mean, you know, I don't even know anymore. [23] **MR. GUY:** Your Honor, that's [24] exactly right and neither do we and nor does [25] (302)658-6697 FAX(302)658-8418

Page 14

[1] Mr. Scherkenbach. [2] **THE COURT:** I don't know if that's [3] real important stuff anymore. I used to be a [4] prosecutor. I thought I understood what crime [5] was. I really did. I thought I had a handle [6] on it for about 20 years. I'm not sure I [7] understand what crime is anymore. You can rape [8] somebody and go to jail for three years, and [9] I'm not belittling it, but if you steal a few [10] million you get 25 years. I'm not working the [11] numbers well. I'm glad I'm getting out of this [12] profession soon. [13] **MR. SCHERKENBACH:** Don't say that. [14] **THE COURT:** I shouldn't be glad I'm [15] getting out? [16] **MR. SCHERKENBACH:** No, don't say [17] you're getting out of this profession. [18] **THE COURT:** I'm going to take up [19] boating. Everybody is real nice. They help [20] you. [21] **MR. SCHERKENBACH:** Judge Maher used [22] to say he was going to take up mullet spotting. [23] (Brief discussion off the record.) [24] **THE COURT:** But I understand what [25] (302)658-6697 FAX(302)658-8418

Page 15

[1] you're saying and I'm going to give you a [2] chance to get some information, but like, you [3] know, damages are an important issue here and [4] I want you to have as good a handle on what [5] evidence is available.

[6] I'm one that's not going to be too [7] persuaded by a lot of what goes on in corporate [8] governs. I'm interested in damages would be [9] the second route because you can't get to [10] damages unless you have a verdict on [11] infringement, so that's important.

[12] And then if you have a verdict on [13] infringement, it's important to know whether [14] the patents are valid. That's the way I kind [15] of look at things. I don't see any crime going [16] on in infringement invalidity, unless I live [17] another year maybe I will. Because I feel bad [18] for you lawyers and what they're doing with the [19] patent and trademark office.

[20] Anyway, let me say this, I'm going [21] to give you a chance. I think what you're [22] really asking me, Judge, can you hold off. [23] Because I'm not going to try this case in the [24] summer anyway. I have two other patent cases.

[25] (302)658-6697 FAX(302)658-8418

Page 16

[1] You're looking at a fall trial date so we have [2] some time.

[3] But I do want you to tell me — let [4] me tell you my thought about separation of [5] issues rather than bifurcation. I'm willing to [6] separate issues because I have concerns in [7] patent trials, having done a number of them, [8] that there's a lot of overlapping evidence that [9] becomes prejudicial, unduly prejudicial. I've [10] convinced myself, which is pretty easy to do [11] when you talk to yourself, that it's important [12] that if you separate infringement invalidity [13] that they ought to have a different jury. And [14] the first injury ought to hear about [15] infringement and possibly damages.

[16] The second jury ought to hear that [17] the person accusing the patent of being invalid [18] has been found to infringe. That's all they [19] need to know. These defendants were found to [20] infringe and they claim that the patents are [21] invalid, so you're going to get to decide [22] whether the patents are invalid. And, again, [23] in my mind I've reasoned that that's a real [24] fair way to try a patent case.

[25] (302)658-6697 FAX(302)658-8418

Page 17

[1] Now, there's obviously issues on [2] both sides they'd rather have some sort of [3] overlap, maybe and maybe not. But the real [4] issue I focus on is whether or not it violates [5] the Seventh Amen-

dment about jury trials. [6] Federal circuit doesn't seem to have the [7] stomach to take that issue up. But they have [8] said that separation of issues is not a bad [9] thing from when Chief Judge Maher was there [10] he's kind of like when he wrote early on and [11] others have what they've written is that they [12] think it's a good idea.

[13] And so the only issues I can focus [14] on is whether or not a second jury violates [15] lays someone jury trial right. I guess as long [16] as it's still a jury how can it do that? [17] I haven't been able to find a way or heard a good [18] argument that it does.

[19] So let me say this, in your case [20] you got to work on your witness list. You got [21] to work on your exhibit list. So it's really a [22] pretried case. You have to understand you're [23] going to have separation of issues. I'm [24] inclined strongly toward infringement and

[25] (302)658-6697 FAX(302)658-8418

Page 18

[1] damages and then validity. And I'm inclined to [2] two separate juries with some spread of time [3] between the infringement and damages verdict. [4] Of course if it's four defendants then you [5] don't try the validity because you don't go [6] after a patent that you don't infringe. But if [7] there is infringement, then we would have the [8] validity case maybe in a month or so after [9] that.

[10] And, again, let me make this clear, [11] I don't do that so that there's pressure on [12] people to settle. I don't worry about [13] settlement. I just do it because it gives you [14] time to think about your case and get ready and [15] you're not coming right off the trial on the [16] first set of issues. So then we would have [17] that second trial.

[18] Now, I'm willing to listen to [19] anything you want to tell me about — you [20] obviously think that damages ought to be put [21] off even further, as I understand it.

[22] **MR. GUY:** Yes, Your Honor. At [23] least until the numbers are set. I understand [24] your point about crime. I understand the

[25] (302)658-6697 FAX(302)658-8418

Page 19

[1] issue. But the point being here is that all we [2] know is the numbers that both experts have [3] relied upon are unreliable and we need to know [4] what those numbers are. And hopefully we'll [5] have it by August, but at the same time —

[6] **THE COURT:** You said August 2. [7] We're thinking about a fall trial.

[8] **MR. GUY:** We need to talk about a [9] trial date, if you're talking October, [10] November, I think it would be plenty of time [11] but I understand there may be

conflicts.

[12] **MR. SCHERKENBACH:** Your Honor, on [13] this financial point, you've indicated that [14] you're inclined to give them some further [15] discovery. I guess we can live with that. I'm [16] frankly disappointed in it because what they [17] want to do is have a fifth day of depositions [18] with my CEO who they've had for four days.

[19] You may remember there was a [20] dispute over the fourth day. But it's a [21] sideshow. If we have to do that to stay on [22] track here we're willing to do it.

[23] **THE COURT:** I'm inclined, based on [24] what I'm being told today, if the supplemental

[25] (302)658-6697 FAX(302)658-8418

Page 20

[1] filings or substitute filings are about matters [2] that are different than are being argued here [3] today and you can demonstrate they're just [4] nothing relevant to what's going on in this [5] trial I may not be inclined.

[6] **MR. SCHERKENBACH:** I appreciate [7] that clarification. I think we at least will [8] be able to make that showing and we'd like an [9] opportunity to do it. It's stock option [10] related. It's non-operating expense. It has [11] nothing to do with the operating profit. It [12] doesn't affect the revenues. It doesn't affect [13] the cost of manufacturing or other costs.

[14] So the thing that the patent [15] damages experts rely on are not going to change [16] a bit as a result of this and we'll be able to [17] show that to you.

[18] In terms of separating the issues, [19] just to respond to your proposal, infringement [20] and damages in one trial to one jury, validity [21] to a later jury. I'll be able to accept that [22] on behalf of Power Integrations. I'm not going [23] to make a Seventh Amendment argument. I [24] understand one probably could be made, but

[25] (302)658-6697 FAX(302)658-8418

Page 21

[1] we're not going to get an answer to that anyway [2] in time to matter.

[3] I think as long as the second jury [4] though is told that what the outcome — without [5] embellishment of what the outcome in the first [6] case was, I think that's important.

[7] **THE COURT:** When I've done it I [8] have the jury understand that there has been an [9] infringement finding but nothing else. We [10] don't talk about the damages award if there is [11] one. We just say there's been an infringement [12] finding but under the law now there's a [13] challenge to the validity of the patent

that's [14] been found to infringe. It puts it real nicely [15] before the jury. They understand that. But it [16] gives you eight new people who hear the [17] validity fresh so there's not any prejudice to [18] the presentation of either sides validity case.

[19] **MR. SCHERKENBACH:** And, again, I [20] can accept that on behalf of my client. I've [21] been through that before with Judge Robinson. [22] I thought it worked reasonably well. Despite [23] what defendants tend to think, it tends to be [24] pretty fair.

[25] (302)658-6697 FAX(302)658-8418

Page 22

[1] My major concern is drawing it out. [2] You mentioned fall, that's great. I'm very [3] much hoping we can get September for the first [4] trial, some time in September, and a delay of [5] maybe no longer then until December or so for [6] the second one. We don't want to drag it out.

[7] **THE COURT:** I was thinking I can [8] sort of give you a range.

[9] **MR. SCHERKENBACH:** That would be [10] great.

[11] **THE COURT:** And I want to give you [12] some dates to revise, what I need revised and [13] presented. Let me go to my manually electronic [14] calendar here.

[15] September has been eaten up by [16] Lucent versus Extreme. They're back for a [17] retrial. I have to hear them. That's a [18] retrial. I granted a motion for a new trial [19] and we set that date a long time ago, so [20] there's really difficulty in getting in [21] September.

[22] However, October, the early part of [23] October is available.

[24] **MR. GUY:** That's fine with us, Your

[25] (302)658-6697 FAX(302)658-8418

Page 23

[1] Honor.

[2] **MR. SCHERKENBACH:** My wife is going [3] to kill me. We're expecting our third on the [4] 8th. I was hoping I could avoid a direct train [5] wreck.

[6] I, also, I'm in trial with Judge [7] Robinson the beginning 30th of October for [8] three weeks, so if we could work around that, [9] maybe start a little after the eight and [10] continue it in that way. I don't actually have [11] the days of the week. Actually, here I do. [12] Okay.

[13] **THE COURT:** I'll tell you what's [14] going on in October. The week of October 2nd [15] — and I don't want you here if your wife is [16] giving birth to your third child on October [17] 8th, so they're the two blank weeks I have in [18] October. Starting the week of October 16th [19] Affymetrix wants to sue Illum-

ina, and Sun Power [20] Company from Puerto Rico wants to sue another [21] power company and they're double scheduled to [22] share the trial day.

[23] And then the week of the 23rd of [24] October, a company called Trilogen wants to

[25] (302)658-6697 FAX(302)658-8418

Page 24

[1] sues Martese for patent infringement and they'd [2] like to be here for seven days.

[3] So other than those first two weeks [4] that sort of eats up October. But we could go [5] to the week — the first week of November, [6] which is actually — it's available and then we [7] could go thirty days later in December.

[8] Now, remember, when there's [9] separation of issues you don't need as much [10] trial time as you needed if you have everything [11] together, obviously. You could go the week of [12] December 4th. So you could have the week of [13] November 6th and then the week of December 4th. [14] It my run in to the following week on either [15] scheduling but that would be fine.

[16] So if those dates work, that would [17] give you enough time to have the August 2nd [18] filing and some discovery if it's ordered [19] and —

[20] **MR. GUY:** Your Honor, my [21] understanding then we'd only have one week to [22] do damages and infringement?

[23] **THE COURT:** Well, maybe only three [24] days.

[25] (302)658-6697 FAX(302)658-8418

Page 25

[1] No, I didn't want you to grab your [2] chest.

[3] **MR. GUY:** I do workout. It's not [4] too dangerous to hear things like that.

[5] **THE COURT:** Typically here [6] infringement, validity and damages you get ten [7] trial days. That's why we're able to try as [8] many cases we do. If we gave everybody what [9] they wanted, we'd never do what we do.

[10] Actually, the week of November 6th. [11] What I was saying is I have the ability to go [12] in to the next week if you eat up more than [13] let's say five or six days. We can do that on [14] the infringement, damages. And, again, on the [15] December date I can go in to next week. But I [16] can't allocate time until I actually see a good [17] pretrial order and a number of witness and I [18] can measure how much time I'm going to give [19] each witness based on what they're going to [20] say.

[21] So the answer is don't be nervous [22] about that. I'm only saying that's the week [23] we'll start. There's enough time

to get seven [24] days if we need it.

[25] (302)658-6697 FAX(302)658-8418

Page 26

[1] **MR. SCHERKENBACH:** I have a mark-
man [2] hearing that's already scheduled on November [3] 15th.

[4] **THE COURT:** You'll be out of here by [5] November 15th, I'll guarantee it, unless the [6] jury is deliberating. There's no way you would [7] be here on infringement and damages November [8] 15th.

[9] **MR. GUY:** We need to raise one [10] other issue, Your Honor, and that has to do [11] with some jury insufficiency in the pretrial [12] order, Power Integrations disclosure. There [13] are 38 products that are accused of infringing [14] 18 claims. And just to March through that, [15] Your Honor, I think — and just 18 claims, Your [16] Honor, in three days is huge.

[17] **THE COURT:** Mr. Scherkenbach has [18] been here before. He knows we're not going to [19] have 38 products.

[20] **MR. GUY:** Well, there are four [21] groups of product, Your Honor, that statements [22] at face value isn't very helpful. We will pair [23] down the number of claims further.

[24] **THE COURT:** The claims are going to [25] (302)658-6697 FAX(302)658-8418

Page 27

[1] be paired down.

[2] **MR. GUY:** The claims will be paired [3] down. The products we'll break down in to only [4] three or four groups. 38 is not a real [5] meaningful number. I'm not prepared to say [6] we'll drop whole groups of products. I think [7] the case can easily be tried in groups, in [8] fact, the experts on both sides have dealt with [9] them in that way, so it's not a real —

[10] **THE COURT:** Four categories of [11] products are different than 38 products. 18 [12] claims is 18 claims. That has to be cut back [13] which you're acknowledging.

[14] **MR. GUY:** Absolutely. We have four [15] patents so it works out one per — I think one [16] of them you only have two claims that's [17] asserted. If we're pairing it back to one [18] claim per patent, that would certainly make it [19] doable. But still these technologies are [20] different. Even though three of them are [21] circuit patents, they do different things. So [22] it is important we recognize that what we're [23] asking the jury to do is to consider at least [24] 16 different permutations of four product

[25] (302)658-6697 FAX(302)658-8418

Page 28

[1] groups versus at least four patent

claims and [2] four different patent. So I'm anxious to see [3] how it's going to be paired down and I think we [4] can have a meaningful understanding in a more [5] thorough pretrial conference state once we know [6] that.

[7] **THE COURT:** You know, there's no [8] order prohibiting both of you from talking [9] about that.

[10] **MR. GUY:** We have asked, Your [11] Honor.

[12] **THE COURT:** Well, it's, you know, [13] actually having a discussion about what might [14] be reasonable and then if you have dispute [15] bring it to me. But here's what I'm — I'm not [16] discussing that today because I recognize that [17] there's some ugliness in other parts of [18] pretrial order, but usually what sets the tone [19] is who's going to be the witness and what [20] they're going to testify about and what [21] exhibits you're going to use.

[22] When I get done addressing those [23] two categories of the pretrial order, I think a [24] little more will become apparent, a little more

[25] (302)658-6697 FAX(302)658-8418

Page 29

[1] of what you have to do will become apparent. [2] If you haven't gotten it done by addressing [3] witnesses and the exhibits.

[4] And when you address witness [5] exhibits they should be addressed in the [6] present understanding of infringement, damages [7] and invalidity. And that should go a long way [8] in pairing down. And you should have [9] discussion with each other, and then if you [10] can't agree then I may have to weigh in.

[11] **MR. SCHERKENBACH:** Can I go back to [12] scheduling for a moment?

[13] **THE COURT:** Yes, you can.

[14] **MR. SCHERKENBACH:** People seem to [15] get a little bit interest in November. That is [16] when I'm in trial if front of Judge Robinson, [17] so October 30 to November 24th. I think that [18] case is highly likely to go. What I would [19] request is that we take the first week of [20] October.

[21] **THE COURT:** You're in a four week [22] trial?

[23] **MR. SCHERKENBACH:** It's two [24] defendants, multiple patents. I think that [25] (302)658-6697 FAX(302)658-8418

Page 30

[1] will be paired back to probably two weeks at [2] the end of the day. Judge Robinson did [3] bifurcate damages. Nonetheless, the first two [4] weeks in November won't work for me. I'd be [5] happy to take the first week of October

because [6] I don't believe damages and infringement will [7] take more than five trial days by anyone's [8] stretch of the imagination and then we can [9] perhaps take the first week in December for [10] validity trial if necessary. That would work.

[11] **MR. GUY:** That's fine with me, Your [12] Honor, as long as we have the ability to [13] overflow into the second week of October if [14] need be.

[15] **MR. SCHERKENBACH:** I think that's [16] fine. Once Your Honor sees the revised [17] pretrial you can make that decision as to [18] whether it requires that much trial time. I [19] don't believe it will.

[20] **THE COURT:** All right. October [21] 2nd, for present purposes, will be the [22] commencement of — Monday, October 2nd will be [23] the commencement of infringement and damages, [24] and December the 4th will be the commencement

[25] (302)658-6697 FAX(302)658-8418

Page 31

[1] of invalidity.

[2] And both sides understand that [3] there will be time allocations set, which I [4] don't know what they'll be yet because I don't [5] know what the witness list looks like or the [6] exhibit list.

[7] **MR. GUY:** We also have an issue of [8] inequitable conduct in this case. That will be [9] tried during the invalidity section?

[10] **THE COURT:** I don't send that, for [11] any purpose, to the jury. I'll listen to the [12] evidence and then I'll issue a decision post [13] trial.

[14] And if you need to present a [15] witness outside of what's presented to the [16] jury, I'll spend the time to hear that one or [17] two witnesses after the jury section is over [18] some day or at a day after the jury evidence is [19] complete.

[20] **MR. SCHERKENBACH:** Very good.

[21] **THE COURT:** Here's what I'm going [22] to do, I'm going to set a second pretrial [23] conference and a date to submit a revised [24] pretrial order along the lines that I've

[25] (302)658-6697 FAX(302)658-8418

Page 32

[1] indicated here.

[2] The second pretrial order will be [3] due Friday, September 1, and then the second [4] pretrial conference — what are your schedules [5] looking like in September? Do you want to come [6] a couple weeks before the trial?

[7] **MR. SCHERKENBACH:** Yes, Your Honor. [8] Fine for Power Integrations really any time in [9] September.

[10] **MR. GUY:** I have a conflict on the [11] 11th, that's it.

[12] **THE COURT:** Okay. So let's see, [13] the 11th — I guess traveling is better in the [14] middle of the week, right, then getting near [15] the end. So do you want to come for the second [16] pretrial conference on either the 13th or the [17] 14th of September?

[18] **MR. GUY:** 14th would be better, [19] Your Honor.

[20] **MR. SCHERKENBACH:** That's fine with [21] me, Your Honor.

[22] **THE COURT:** All right. We'll do it [23] on the 14th of September, which is a Thursday, [24] and we'll do it at I guess 1:30. Does that

[25] (302)658-6697 FAX(302)658-8418

Page 33

[1] work?

[2] **MR. SCHERKENBACH:** Yes, Your Honor.

[3] **MR. GUY:** Your Honor, we have an [4] issue of motions in liminae in the case. Can [5] we take up the hearing on the motion in liminae [6] or briefing schedule for the September 1st [7] date?

[8] **THE COURT:** Yes, you can agree to [9] that. What I typically will do is at the [10] pretrial conference that actually is [11] anticipation of a set trial I will give you my [12] rulings at that pretrial conference. So you [13] should give me enough time to read whatever it [14] is you're going to write before that pretrial [15] conference. So if it's the 14th, you probably [16] should get it here that Monday or the Friday [17] before and then we'll take a look at it and [18] give you the rulings on the pretrial [19] conference.

[20] **MR. GUY:** So, in other words, you [21] would like to have briefing completed by [22] September the 4th, that would be the Monday the [23] week before?

[24] **THE COURT:** No, just the Monday —

[25] (302)658-6697 FAX(302)658-8418

Page 34

[1] **MR. GUY:** The 11th?

[2] **THE COURT:** That would be fine if [3] you got it here by then. You know, it's [4] granted or denied. It doesn't take a lot of [5] effort if you get excellent briefing. The [6] decision is as good as what the argument is, [7] right?

[8] **MR. GUY:** Absolutely.

[9] **THE COURT:** Unless minimally [10] skewed.

[11] **MR. SCHERKENBACH:** Can I ask Your [12] Honor how you're handling the issue of experts [13] beyond the scope of report? Is it the same way [14] you have been in the past?

[15] **THE COURT:** Absolutely.

[16] MR. SCHERKENBACH: I think that [17] will help resolve a number of things.
[18] THE COURT: Right. That's one of [19] my, what is it, we all get 27 great ideas and [20] I'm working on 4,011. That was one of the [21] great ideas. It really works. I've now [22] ordered new trial. It's not good if you play [23] around with the expert report.

[24] You know that practice.

[25] (302)658-6697 FAX(302)658-8418

Page 35

[1] MR. GUY: Perhaps I should hear it [2] clearer from you, Your Honor.

[3] THE COURT: I'll give it to you [4] straight up here. Everybody argues over expert [5] reports and then the expert gets to trial and [6] of course there's something alleged to be [7] different, some new opinion, some nuance on an [8] opinion, particularly after the other side has [9] taken advantage of the opportunity for [10] deposition under the rule.

[11] My practice is in a trial, a [12] serious trial with a jury, or even in a bench, [13] I guess, but particularly the jury, I don't [14] have time to go back and read the report and [15] make an evidentiary ruling on the expert's [16] testimony, so you have to interpose your [17] objection.

[18] If you think the witness is [19] testifying outside of the report and deposition [20] or if it's just a report of the report, if post [21] trial you maintain that objection and I take a [22] look at it and in fact there is some variance, [23] and I mean "some," it doesn't have to be a lot, [24] something that I think could have affected the

[25] (302)658-6697 FAX(302)658-8418

Page 36

[1] other side to their detriment because it wasn't [2] disclosed, I simply say that there's a mistrial [3] and the other side pays the cost of the first [4] trial and we go to a second trial.

[5] It puts a lot of burden on the [6] attorneys but it's, you know, how can you have [7] experts — I mean discovery. I used to find [8] after trial that in fact the witness deviated [9] substantially and what do you do then? You [10] know, you're kind of interested in keeping the [11] verdict and things like that but it really [12] isn't fair during a trial in my experience, so [13] that's the practice.

[14] MR. GUY: Your Honor, both sides [15] filed supplemental expert reports in light of [16] other fact discovery that was ongoing and we [17] still have an issue, certainly if there's a [18] debate 30 days before the trial in which the [19] expert reports are filed by that point, any [20] variance from that is certainly understandable. [21] You're not addressing

issues where there's been [22] an ongoing fact discovery and expert report [23] comes in to supplement?

[24] THE COURT: No. You all, as I

[25] (302)658-6697 FAX(302)658-8418

Page 37

[1] understand it, have a little more you want to [2] do. So get it done, pick a date, if you can't [3] pick a date I'll give you one. It will be some [4] time in August.

[5] MR. SCHERKENBACH: For damages I [6] think that's fine. This doesn't bear on [7] liability at all?

[8] THE COURT: No, liability from what [9] I saw in the proposed pretrial order is clear. [10] So you will get that date. And what you're not [11] allowed to do is to send a letter like a week [12] before trial saying the witness just told me [13] this and I'm going to add this or something. [14] So whatever that date is, that's what you're [15] locked in to as a report and deposition.

[16] MR. GUY: Your Honor, just so we're [17] clear, we had an expert who did add additional [18] prior art at a deposition. As long as that's [19] in a report by this cutoff date, that should be [20] okay. We'll certainly make sure that whatever [21] he testified to is actually contained in that [22] report.

[23] THE COURT: That's pushing the [24] envelope a little bit because damages, by your

[25] (302)658-6697 FAX(302)658-8418

Page 38

[1] request, has opened up a little bit.

[2] MR. GUY: Yes, Your Honor.

[3] THE COURT: We have expert dates [4] and I know we all get up every day and have a [5] better idea than we had yesterday, but in [6] litigation we really have to tell the expert [7] that there's a date where you can't think [8] anymore. And I'm trying to say this very [9] simply.

[10] So if a new piece of prior art came [11] in but there's been a cutoff date, they're [12] stuck with that cutoff date. We have to limit [13] the discovery and the opinion offering.

[14] Now, if in this case, because the [15] trial date is some time off, you can both agree [16] that you want to — but I wouldn't let that be [17] an August date on liability. That's too close [18] to the trial date. But if by July or something [19] you want to extent it and you want to [20] supplement reports, get them all cleaned up, [21] but you got to on expert opinion testimony [22] there has to be a date when it ends.

[23] In a medical malpractice case and [24] the guy comes in, the doctor, a surgeon, wants

[25] (302)658-6697 FAX(302)658-8418

Page 39

[1] to talk about an operation he had last week, [2] how are you supposed to prepare for that? At [3] some point — because he learned something. I [4] believe he did. Then they say you can [5] foreclose. You have to foreclose.

[6] Mr. GUY: Your Honor, we can [7] certainly set a date this summer in which [8] everything will be final and we have the other [9] discovery to do. I just want to make sure that [10] to the extent the expert has provided testimony [11] on something, that we can make sure it's in, [12] we'll go back and make sure if any supplement [13] report is due we can probably do it by the end [14] of June, first of July and give them plenty of [15] time.

[16] THE COURT: Do you have a problem [17] with that?

[18] MR. SCHERKENBACH: We do because [19] the deposition has happened. It's done and [20] over with. This is actually one of the motions [21] in liminae. Not that I expect the Court to [22] even look at them at this point, but there's a [23] particular person they have in mind who [24] substantially changed his opinions at

[25] (302)658-6697 FAX(302)658-8418

Page 40

[1] deposition and without supplementing the report [2] and we were told, well, you've had a chance to [3] ask questions, ask him questions at deposition, [4] that's too bad.

[5] So what I'm sure they'd now love to [6] do is have a date in the future that they can [7] put it in a report. I guess we'll depose him [8] again. We object to that. That's over. It's [9] a very limited window to do damages expert [10] reports — discovery, excuse me, reports are [11] done. Finish those, a will bit of clean up and [12] that should be that.

[13] Maybe this is something Your Honor [14] decides in motion in liminae and if we lose we [15] have to go back to the drawing board. We're [16] doing a mock trial next weekend. I need to [17] know what the case looks like, what it's going [18] to be. I think I do on the liability side and [19] we're preparing for trial. I should not have [20] to be redoing liability expert discovery.

[21] THE COURT: I'll tell you what that [22] motion in liminae gets you a decision, then [23] you'll know whether you can — see, one of the [24] things, if what I'm hearing is factual, if the

[25] (302)658-6697 FAX(302)658-8418

Page 41

[1] witness changed at the deposition what the [2] opinions of the report were,

that's an [3] egregious violation of the scheduling order [4] because how would you ever prepare for a [5] deposition except from the report, and then [6] when you showed up if there were new opinions [7] that weren't in the report, what would be the [8] sense of a deposition?

[9] **MR. GUY:** Your Honor, he did not [10] change his view in the report originally. What [11] he did was he supplemented with additional [12] prior art and also with an obviousness argument [13] that he provided them with a clear shot at it [14] at the deposition.

[15] **THE COURT:** That's my point. Let's [16] assume he added a piece of prior art and [17] modified his opinion. It's like the surgeon [18] that comes in and says last week I had a [19] cardiac operation, let me tell you what I did. [20] So I go to the deposition, you know, I'm [21] prepared and done and happy, and all of a [22] sudden he starts talking about prior art [23] because it's not in his report, how did I [24] prepare for that? So how did I intelligently

[25] (302)658-6697 FAX(302)658-8418

Page 42

[1] conduct the deposition, which is my opportunity [2] to get further information about the opinions [3] in the report?

[4] **MR. GUY:** They were certainly aware [5] on notice that there was obviousness issue. [6] There was certainly notice on prior art. They [7] certainly had an opportunity and all we wish to [8] do is preserve what is already in a deposition [9] for trial.

[10] **THE COURT:** I'm asking you, we're [11] just having a conversation here, we're not a [12] accusing anybody.

[13] **MR. GUY:** Furthermore —

[14] **THE COURT:** How would I have [15] prepared for that deposition if I didn't know [16] about the new piece of prior art?

[17] **MR. GUY:** You would have gone in [18] and you would have prepared for obviousness. [19] You would have learned about the additional [20] prior art. You would have asked questions [21] related to obviousness.

[22] **THE COURT:** I would have done that?

[23] **MR. GUY:** Furthermore, I forgot [24] this, but it was in part in response to their [25] (302)658-6697 FAX(302)658-8418

Page 43

[1] rebuttal report. So it's a lot more involved [2] in this than just we surprised them. They [3] certainly had an opportunity to cross the [4] expert. They had an opportunity to go in. If [5] they needed more time, they had that, also.

[6] So all we're trying to do is [7] preserve what's in a deposition. It was right [8] after the markman hearing, so it would have [9] been late February or March. So they had ample [10] opportunity. There's no surprise like on a [11] witness stand when someone talks about what [12] they did last week. We have all summer, Your [13] Honor, to address this if there's an issue. We [14] just want to be able to get the evidence in for [15] a validity issue which isn't going to trial [16] until December, so there's ample opportunity [17] here to address this rather than trying to [18] strike some evidence that they feel that they [19] don't like.

[20] I would also add that at least in [21] one instance that where we were aware of the [22] art through one of their experts, so, you know, [23] it does take a little bit of iteration here to [24] get all the evidence in and all the expert

[25] (302)658-6697 FAX(302)658-8418

Page 44

[1] reports right. We certainly will not deviate [2] from the expert reports once they're final. [3] And we can make that final date July.

[4] **THE COURT:** See, there could be a [5] book written, or at least a chapter, that you [6] and I could do in a patent trial treatise. [7] Because my view would be, and I'm not an [8] advocate, is that the deposition is the trial [9] date in the context of the scheduling order for [10] expert discovery. That's the drop dead [11] examination day.

[12] But you have the view of 95 percent [13] of the lawyers that come here, which is [14] understandable because you need some iteration, [15] you need to play a little bit, you got to find [16] out, then they put a rebuttal and I have to [17] respond to that.

[18] But that, in my view, runs [19] completely against all of the rules of [20] procedure. So why did I do a scheduling order [21] and have expert discovery dates? They're like [22] the world ends on those dates. There is no [23] other day. And they're drop dead dates.

[24] So when that witness comes in and [25] (302)658-6697 FAX(302)658-8418

Page 45

[1] has a new piece of prior art, which is the [2] practice, I mean, that's what the lawyers do, [3] then you open up the date.

[4] **MR. GUY:** I understand but I think [5] it's one of degree. We're not talking about we [6] submitted two pieces of prior art.

[7] **THE COURT:** You're getting nervous. [8] Don't get nervous I'm going to foreclose. [9] You're getting nervous. We're just having a [10] conversation about the real world versus Civil [11] Procedure 1 in

law school. There's actually [12] people that think that there are dates that [13] count.

[14] I might let you have this in. I [15] have to see what was said. But how do we get [16] lawyers to understand that they are drop dead [17] dates and there is no iteration beyond that [18] date? I mean, the world ended for purposes of [19] that discovery. And it doesn't matter whether [20] they learned which was until then truly not [21] able to be found by them some new information, [22] how do we package a trial if we keep having 95 [23] percent of the lawyers think that the dates [24] have some sort of elasticity in them, you know,

[25] (302)658-6697 FAX(302)658-8418

Page 46

[1] they can be just pushed a little bit? It's [2] really hard. But we're not going to solve that [3] today.

[4] What's the motion in liminae I got [5] to look at?

[6] **MR. SCHERKENBACH:** No. 2, Your [7] Honor, on Power Integrations list. This is tab [8] 16 the second item.

[9] **THE COURT:** We'll get you a quick [10] answer from Tab 16 on No. 2.

[11] **MR. SCHERKENBACH:** I assume you'd [12] like us to — do you want short letter briefs [13] on this or —

[14] **THE COURT:** Sure. Because the [15] motions are only listed.

[16] **MR. SCHERKENBACH:** Yes, just [17] identifies the issues. So we can get you a [18] short letter brief in say a week.

[19] **THE COURT:** That's fine. And then [20] we'll get you the answer.

[21] **MR. GUY:** Your Honor, would we be [22] also allowed to — they've done much the same [23] and we would like to file a similar motion in [24] liminae on the same issue if they're going to

[25] (302)658-6697 FAX(302)658-8418

Page 47

[1] do it this way.

[2] **THE COURT:** In the legal profession [3] it's always fair to punch back.

[4] **MR. GUY:** Just wanted to make sure.

[5] **THE COURT:** Sure.

[6] **MR. SCHERKENBACH:** Which one is [7] that, Mr. Guy?

[8] **THE COURT:** How would we maintain [9] the adversary system if we didn't punch back? [10] It would just collapse. We'd have lawyers with [11] low blood pressure or something.

[12] Which one do you want to punch back [13] with?

[14] **MR. GUY:** Under our Tab 17.

[15] **THE COURT:** This is the limit now. [16]

This is dropping dead. I'm not going to look [17] at any others.

[18] **MR. GUY:** In terms of?

[19] **THE COURT:** In terms of opening up [20] any kind of expert discovery beyond the damages [21] that you've argued you can't get done because [22] of the August 2 filings, anticipate filing.

[23] **MR. GUY:** In our motions in [24] liminae —

[25] (302)658-6697 FAX(302)658-8418

Page 48

[1] **MR. SCHERKENBACH:** And I don't [2] believe Your Honor to raise one that relates to [3] this issue.

[4] **THE COURT:** Let them look at my [5] filing. Give them a chance.

[6] **MR. GUY:** The first one is defense [7] motion in liminae, motion to exclude untimely [8] reports in an undisclosed expert.

[9] **THE COURT:** They got you pretty [10] good there, Scherk.

[11] **MR. SCHERKENBACH:** The expert. If [12] that's the one you want, that's great. No. 1, [13] fine.

[14] **MR. GUY:** Motion with respect to [15] their expert, Troxel, I believe all of those [16] deal with there is an untimely report there as [17] well. I think it's item No. 3 under 2.

[18] **THE COURT:** No. 1, 2. Item No. 3.

[19] **MR. SCHERKENBACH:** I don't think [20] we're talking about damages related stuff. [21] This is liability.

[22] **THE COURT:** If you throw damages in [23] there, you get a yellow flag for piling on.

[24] **MR. GUY:** That was the damage

[25] (302)658-6697 FAX(302)658-8418

Page 49

[1] expert, Your Honor, so we're going to preserve [2] those.

[3] **THE COURT:** We've already said [4] that's a different category. We're going to [5] wait until after August 2 to let you have at [6] each other on damages. This is only liability, [7] that be the context of infringement, validity, [8] expert reports.

[9] All right, your time up. It's a [10] game clock. So you have No. 1, Tab 17 and [11] there's No. 2, Tab 16, and we'll get letters [12] and you'll agree to that schedule for about a [13] week to get them in here and we'll give you [14] expeditious decision so you know where you are.

[15] **MR. SCHERKENBACH:** Thank you, Your [16] Honor.

[17] **THE COURT:** Okay. I think that's [18] all we can do today. I will expect that the [19] one date I got to give you is let's just make [20] it —

[21] **MR. GUY:** I'm sorry, Your Honor, [22] the first letter brief would be due June 7th; [23] is that right?

[24] **THE COURT:** I'm not getting in to

[25] (302)658-6697 FAX(302)658-8418

Page 50

[1] that. You're going to talk with each other and [2] come up with an exchange schedule.

[3] **MR. SCHERKENBACH:** The date for [4] damages wrap up?

[5] **THE COURT:** We need a date for [6] that. It has to be in August because we'll [7] need a couple weeks before the pretrial for any [8] disputes.

[9] **MR. SCHERKENBACH:** The 4th is a [10] Friday. Does that work?

[11] **MR. GUY:** The quarterly reports [12] don't come out until the 2nd.

[13] **MR. SCHERKENBACH:** Okay, the 11th.

[14] **MR. GUY:** You're going to be able [15] to give us a deposition on any changes in that [16] time? Maybe we should push it to the 18th, [17] Your Honor.

[18] **THE COURT:** That would put it [19] beyond the —

[20] **MR. GUY:** It's August the 18th.

[21] **THE COURT:** Oh, August 18th. [22] August 18th is fine with me.

[23] So August 18th is the damages [24] cutoff.

[25] (302)658-6697 FAX(302)658-8418

Page 51

[1] **MR. SCHERKENBACH:** That would be [2] fine, Your Honor.

[3] **MR. GUY:** Be fine, Your Honor.

[4] **THE COURT:** Okay. We'll put this [5] all in an order and get it entered and then [6] look to see those motions in liminae letters.

[7] **MR. SCHERKENBACH:** Thank you, Your [8] Honor.

[9] **THE COURT:** Thank you. We'll be in [10] recess.

[11] (Court adjourned at 1:32 p.m.)

[12] (302)658-6697 FAX(302)658-8418

Page 52

State of Delaware)
New Castle County)
CERTIFICATE OF REPORTER
I, Stacy L. Vickers, Registered
Professional Reporter and Notary Public, do hereby
certify that the foregoing record is a true and
accurate transcript of my stenographic notes taken
on May 31, 2006, in the above-captioned matter.
IN WITNESS WHEREOF, I have hereunto set my
hand and seal this 14th day of June, 2006, at
Wilmington.

Stacy L. Vickers, RPR
Cert.#: 115-RPR
Hawkins Reporting Service
715 North King Street - Wilmington, Delaware 19801
(302)658-6697 FAX(302)658-8418

Lawyer's Notes

\$

\$135 million 11:23
\$27 million 11:20
\$36 million 13:3
\$45 million 11:22
\$6 million 11:21

1

1 32:3; 45:11; 48:12, 18; 49:10
11th 32:11, 13; 34:1; 50:13
13th 32:16
14th 32:17, 18, 23; 33:15
15th 26:3, 5, 8
16 27:24; 46:8, 10; 49:11
16th 23:18
17 47:14; 49:10
18 26:14, 15; 27:11, 12
18th 50:16, 20, 21, 22, 23
1999 7:11
1:30 32:24
1:32 51:11
1st 33:6

2

2 12:8; 19:6; 46:6, 10; 47:22; 48:17, 18; 49:5, 11
20 14:6
2005 7:6
2006 13:16
23 11:18
23rd 23:23
24th 29:17
25 14:10
27 34:19
29 12:10
2nd 7:16; 23:14; 24:17; 30:21, 22; 50:12

3

3 48:17, 18
30 12:10; 29:17; 36:18
30(B)6 6:16
302)658-6697 4:25; 5:25; 6:25; 7:25; 8:25; 9:25; 10:25; 11:25; 12:25; 13:25; 14:25; 15:25; 16:25; 17:25; 18:25; 19:25; 20:25; 21:25; 22:25; 23:25; 24:25; 25:25; 26:25; 27:25; 28:25; 29:25; 30:25; 31:25; 32:25; 33:25; 34:25; 35:25; 36:25; 37:25; 38:25; 39:25; 40:25; 41:25; 42:25;

43:25; 44:25; 45:25; 46:25; 47:25; 48:25; 49:25; 50:25; 51:12
30th 23:7
38 26:13, 19; 27:4, 11

4

4,011 34:20
40 12:14
45 12:5
4th 24:12, 13; 30:24; 33:22; 50:9

5

5 12:1
5.9 12:9

6

6 12:1, 11
6th 24:13; 25:10

7

7th 49:22

8

8th 23:4, 17

9

95 44:12; 45:22

A

ability 25:11; 30:12
able 5:15; 17:17; 20:8, 16, 21; 25:7; 43:14; 45:21; 50:14
Absolutely 27:14; 34:8, 15
accept 20:21; 21:20
according 7:13
accumulative 4:8
accused 9:10, 22; 26:13
accusing 16:17; 42:12
acknowledging 27:13
actually 5:12; 9:16; 10:3; 23:10, 11; 24:6; 25:10, 16; 28:13; 33:10; 37:21; 39:20; 45:11
add 12:6, 7; 37:13, 17; 43:20
added 41:16
addition 7:12
additional 10:4; 37:17; 41:11; 42:19

address 29:4; 43:13, 17
addressed 29:5
addressing 28:22; 29:2; 36:21
adjourned 51:11
admitted 5:9
advantage 35:9
adversary 47:9
advocate 44:8
affect 20:12, 12
affected 35:24
Affymetrix 23:19
again 5:18; 8:5; 16:22; 18:10; 21:19; 25:14; 40:8
against 44:19
ago 22:19
agree 29:10; 33:8; 38:15; 49:12
agreed 9:24
alleged 35:6
allocate 25:16
allocation 4:5
allocations 31:3
allow 5:5
allowed 37:11; 46:22
almost 12:10
along 31:24
always 47:3
Amendment 17:5; 20:23
America 13:17
amount 5:22; 11:16
amounts 13:10
ample 43:9, 16
annual 7:2, 7, 10
answered 4:24
anticipate 47:22
anticipation 33:11
anxious 28:2
anymore 13:22; 14:3, 7; 38:8
apparent 28:24; 29:1
apparently 7:5
appreciate 20:6
approximately 11:1
April 6:20
argued 20:2; 47:21
argues 35:4
argument 8:12; 12:18; 17:18; 20:23; 34:6; 41:12
around 23:8; 34:23
art 37:18; 38:10; 41:12, 16, 22; 42:6, 16, 20; 43:22; 45:1, 6
asserted 27:17
assume 41:16; 46:11
Assuming 13:2
attorneys 36:6
August 7:16; 19:5, 6; 24:17; 37:4; 38:17; 47:22; 49:5; 50:6, 20, 21, 22, 23
available 15:5; 22:23; 24:6

avoid 23:4
award 21:10
aware 42:4; 43:21

B

back 7:10, 23; 9:20; 22:16; 27:12, 17; 29:11; 30:1; 35:14; 39:12; 40:15; 47:3, 9, 12
bad 15:17; 17:8; 40:4
based 19:23; 25:19
basically 11:15
bear 37:6
become 28:24; 29:1
becomes 16:9
beginning 23:7
behalf 20:22; 21:20
belittle 13:20
belittling 14:9
bench 35:12
better 32:13, 18; 38:5
beyond 34:13; 45:17; 47:20; 50:19
bifurcate 30:3
bifurcation 6:10; 8:7; 16:5
birth 23:16
bit 4:13; 8:15; 20:16; 29:15; 37:24; 38:1; 40:11; 43:23; 44:15; 46:1
blank 23:17
blood 47:11
board 7:19; 9:20; 40:15
boating 14:19
book 44:5
both 4:3; 5:19; 7:24; 17:2; 19:2; 27:8; 28:8; 31:2; 36:14; 38:15
break 27:3
Brief 14:23; 46:18; 49:22
briefing 33:6, 21; 34:5
briefly 11:4
briefs 46:12
bring 28:15
burden 4:24; 36:5
buyer 12:23

C

calendar 22:14
call 4:13, 18
called 23:24
came 9:17; 38:10
can 4:6; 5:11; 10:9; 14:7; 15:22; 17:13, 16; 19:15; 20:3; 21:20; 22:3, 7; 25:13, 15, 18; 27:7; 28:4; 29:11, 13; 30:8, 17; 33:4, 8; 34:11; 36:6; 38:15; 39:4, 6, 11, 13; 40:6, 23; 44:3; 46:1, 17; 49:18

cardiac 41:19
case 4:2, 15; 5:5, 24; 6:1, 1; 9:8; 10:14, 21; 11:1, 13; 15:23; 16:24; 17:19, 22; 18:8, 14; 21:6, 18; 27:7; 29:18; 31:8; 33:4; 38:14, 23; 40:17
cases 15:24; 25:8
categories 27:10; 28:23
category 49:4
cause 10:6
CEO 19:18
certain 5:4; 11:2
certainly 10:10; 27:18; 36:17, 20; 37:20; 39:7; 42:4, 6, 7; 43:3; 44:1
chairman 8:1
challenge 21:13
chance 15:2, 21; 40:2; 48:5
change 20:15; 41:10
changed 39:24; 41:1
changes 50:15
chapter 44:5
characterized 4:19
chest 25:2
chief 8:1; 17:9
child 23:16
circuit 17:6; 27:21
Civil 45:10
claim 11:22, 24; 12:3; 16:20; 27:18
claiming 11:14
claims 11:15; 26:14, 15, 23, 24; 27:2, 12, 12, 16; 28:1
clarification 20:7
clean 40:11
cleaned 38:20
clear 7:9; 18:10; 37:9, 17; 41:13
clearer 35:2
clearly 13:5
client 21:20
clock 49:10
close 38:17
collapse 47:10
coming 5:13; 18:15
commencement 30:22, 23, 24
comment 10:9
company 8:3; 23:20, 21, 24
complete 31:19
completed 33:21
completely 44:19
component 8:8
concern 22:1
concerns 8:20; 16:6
conduct 31:8; 42:1
conference 28:5; 31:23; 32:4, 16; 33:10, 12, 15, 19
conflict 32:10

conflicts 19:11
consider 8:6; 27:23
consistent 4:22
contained 37:21
context 44:9; 49:7
continue 23:10
contrary 9:19
conversation 42:11;
45:10
convinced 16:10
corporate 13:16; 15:7
cost 12:19; 20:13; 36:3
costs 11:13; 20:13
count 45:13
couple 13:20; 32:6; 50:7
course 18:4; 35:6
COURT 6:8; 8:6, 10;
11:24; 12:5, 13, 16; 13:15,
19; 14:2, 14, 18, 24; 19:6,
23; 21:7; 22:7, 11; 23:13;
24:23; 25:5; 26:4, 17, 24;
27:10; 28:7, 12; 29:13, 21;
30:20; 31:10, 21; 32:12,
22; 33:8, 24; 34:2, 9, 15,
18; 35:3; 36:24; 37:8, 23;
38:3; 39:16, 21; 40:21;
41:15; 42:10, 14, 22; 44:4;
45:7; 46:9, 14, 19; 47:2, 5,
8, 15, 19; 48:4, 9, 18, 22;
49:3, 17, 24; 50:5, 18, 21;
51:4, 9, 11
crime 14:4, 7; 15:15;
18:24
cross 43:3
currently 7:4
cut 27:12
cutoff 37:19; 38:11, 12;
50:24

D

damage 48:24
damages 6:3, 13, 15, 22,
22, 24; 7:1, 22; 8:6, 8, 16;
9:1; 10:13; 11:22, 24;
12:10; 15:3, 8, 10; 16:15;
18:1, 3, 20; 20:15, 20;
21:10; 24:22; 25:6, 14;
26:7; 29:6; 30:3, 6, 23;
37:5, 24; 40:9; 47:20;
48:20, 22; 49:6; 50:4, 23
dangerous 25:4
date 5:22; 10:19; 16:1;
19:9; 22:19; 25:15; 31:23;
33:7; 37:2, 3, 10, 14, 19;
38:7, 11, 12, 15, 17, 18,
22; 39:7; 40:6; 44:3, 9;
45:3, 18; 49:19; 50:3, 5
dates 22:12; 24:16; 38:3;
44:21, 22, 23; 45:12, 17,
23
dating 7:23
day 19:17, 20; 23:22;
30:2; 31:18, 18; 38:4;
44:11, 23

days 19:18; 23:11; 24:2,
7, 24; 25:7, 13, 24; 26:16;
30:7; 36:18
dead 44:10, 23; 45:16;
47:16
deal 48:16
dealt 27:8
debate 36:18
December 22:5; 24:7, 12,
13; 25:15; 30:9, 24; 43:16
decide 16:21
decides 40:14
decision 30:17; 31:12;
34:6; 40:22; 49:14
decisions 4:7; 5:18
defendants 16:19; 18:4;
21:23; 29:24
defense 48:6
degree 45:5
delay 10:7; 22:4
deliberating 26:6
delisting 7:19
demonstrate 20:3
denied 34:4
depend 13:5
depending 5:21
depose 40:7
deposed 6:15; 9:2
deposition 6:16, 17;
9:14; 10:1, 3; 11:8; 35:10,
19; 37:15, 18; 39:19; 40:1,
3; 41:1, 5, 8, 14, 20; 42:1,
8, 15; 43:7; 44:8; 50:15
depositions 6:14; 19:17
derail 10:20
Despite 21:22
detriment 36:1
deviate 44:1
deviated 36:8
different 8:19, 21; 16:13;
20:2; 27:11, 20, 21, 24;
28:2; 35:7; 49:4
difficult 5:14
difficulty 22:20
digit 11:2
direct 23:4
disappointed 19:16
disclosed 36:2
disclosure 26:12
discovery 7:15; 9:1;
10:5; 19:15; 24:18; 36:7,
16, 22; 38:13; 39:9; 40:10,
20; 44:10, 21; 45:19; 47:20
discussing 28:16
discussion 14:23; 28:13;
29:9
dispute 19:20; 28:14
disputes 50:8
divided 8:13
doable 27:19
doctor 38:24
document 10:4; 11:7
done 5:23; 16:7; 21:7;

28:22; 29:2; 37:2; 39:19;
40:11; 41:21; 42:22;
46:22; 47:21
double 23:21
down 26:23; 27:1, 3, 3;
28:3; 29:8
drag 22:6
drawing 9:20; 22:1;
40:15
drop 27:6; 44:10, 23;
45:16
dropping 47:16
due 10:11; 13:7; 32:3;
39:13; 49:22
during 11:7; 31:9; 36:12

E

early 6:20; 17:10; 22:22
easily 27:7
easy 16:10
eat 25:12
eaten 22:15
eats 24:4
effort 34:5
egregious 41:3
eight 21:16; 23:9
either 10:18; 21:18;
24:14; 32:16
elasticity 45:24
electronic 22:13
else 21:9
elusive 9:13
embellishment 21:5
end 6:20; 30:2; 32:15;
39:13
ended 45:18
ends 12:8; 38:22; 44:22
enough 24:17; 25:23;
33:13
entered 51:5
envelope 37:24
erosion 11:15; 12:2, 10;
13:4
essentially 9:11
Even 11:17; 13:1, 22;
18:21; 27:20; 35:12; 39:22
Everybody 14:19; 25:8;
35:4
evidence 15:5; 16:8;
31:12, 18; 43:14, 18, 24
evidentiary 35:15
exactly 4:10; 5:10, 15;
13:24
examination 44:11
excellent 34:5
except 41:5
exchange 50:2
exclude 48:7
excuse 40:10
executives 13:20
exhibit 17:21; 31:6

exhibits 5:3, 4, 15; 28:21;
29:3, 5
expect 7:13; 39:21; 49:18
expecting 23:3
expeditious 49:14
expense 20:10
expenses 11:12
experience 36:12
expert 6:19, 19, 20;
10:18; 34:23; 35:4, 5;
36:15, 19, 22; 37:17; 38:3,
6, 21; 39:10; 40:9, 20;
43:4, 24; 44:2, 10, 21;
47:20; 48:8, 11, 15; 49:1, 8
expert's 35:15
experts 6:14, 15, 24; 7:1,
22; 9:2; 19:2; 20:15; 27:8;
34:12; 36:7; 43:22
extent 9:9; 10:2; 38:19;
39:10
Extreme 22:16

F

face 26:22
fact 9:16, 22; 27:8; 35:22;
36:8, 16, 22
factor 12:19
factual 40:24
failure 7:20
fair 16:24; 21:24; 36:12;
47:3
Fairchild 6:10; 9:9, 10, 19
fairly 4:19
fall 16:1; 19:7; 22:2
false 13:21
FAX(302)658-8418 4:25;
5:25; 6:25; 7:25; 8:25;
9:25; 10:25; 11:25; 12:25;
13:25; 14:25; 15:25;
16:25; 17:25; 18:25;
19:25; 20:25; 21:25;
22:25; 23:25; 24:25;
25:25; 26:25; 27:25;
28:25; 29:25; 30:25;
31:25; 32:25; 33:25;
34:25; 35:25; 36:25;
37:25; 38:25; 39:25;
40:25; 41:25; 42:25;
43:25; 44:25; 45:25;
46:25; 47:25; 48:25;
49:25; 50:25; 51:12
February 43:9
Federal 17:6
feel 15:17; 43:18
few 13:21, 21; 14:9
fifth 19:17
file 46:23
filed 7:6; 13:12; 36:15, 19
filing 24:18; 47:22; 48:5
filings 7:2; 10:16, 17;
12:20; 13:21; 20:1, 1;
47:22
final 39:8; 44:2, 3

finally 9:14
financial 7:2; 8:1; 10:8;
13:4; 19:13
find 17:17; 36:7; 44:15
finding 21:9, 12
fine 22:24; 24:15; 30:11,
16; 32:8, 20; 34:2; 37:6;
46:19; 48:13; 50:22; 51:2,
3
Finish 40:11
fired 8:2; 13:12, 20
firm 13:16
first 10:22; 16:14; 18:16;
21:5; 22:3; 24:3, 5; 29:19;
30:3, 5, 9; 36:3; 39:14;
48:6; 49:22
five 11:2; 15:1; 25:13;
30:7
flag 48:23
focus 17:4, 13
following 24:14
foreclose 39:5, 5; 45:8
forgot 42:23
forth 10:19
found 16:18, 19; 21:14;
45:21
four 18:4; 19:18; 26:20;
27:4, 10, 14, 24; 28:1, 2;
29:21
fourth 19:20
frankly 19:16
fresh 21:17
Friday 32:3; 33:16; 50:10
front 7:18; 29:16
fundamental 7:21
further 9:1; 10:1; 18:21;
19:14; 26:23; 42:2
Furthermore 42:13, 23
future 40:6

G

game 49:10
gave 25:8
gets 4:23; 35:5; 40:22
gives 5:17; 18:13; 21:16
giving 23:16
glad 14:11, 14
goes 15:7
good 15:4; 17:12, 17;
25:16; 31:20; 34:6, 22;
48:10
governs 15:8
grab 25:1
granted 22:18; 34:4
grants 10:19
great 22:2, 10; 34:19, 21;
48:12
groups 26:21; 27:4, 6, 7;
28:1
guarantee 26:5
guess 5:21; 17:15; 19:15;
32:13, 24; 35:13; 40:7

GUY 6:6; 9:5; 10:10, 22;
12:4, 7, 14, 21; 13:18, 23;
18:22; 19:8; 22:24; 24:20;
25:3; 26:9, 20; 27:2, 14;
28:10; 30:11; 31:7; 32:10,
18; 33:3, 20; 34:1, 8; 35:1;
36:14; 37:16; 38:2, 24;
39:6; 41:9; 42:4, 13, 17,
23; 45:4; 46:21; 47:4, 7,
14, 18, 23; 48:6, 14, 24;
49:21; 50:11, 14, 20; 51:3
Guy's 8:24

H

hand 10:11
handle 14:5; 15:4
handling 34:12
happen 4:3; 9:4
happened 11:1; 39:19
happy 8:14; 30:5; 41:21
hard 46:2
hear 8:11; 16:14, 16;
21:16; 22:17; 25:4; 31:16;
35:1
heard 6:6; 17:17
hearing 26:2; 33:5;
40:24; 43:8
help 14:19; 34:17
helpful 26:22
here's 28:15; 31:21
highly 29:18
hold 15:22
Honor 6:7; 7:12; 8:9, 18;
9:7; 10:22; 13:23; 18:22;
19:12; 23:1; 24:20; 26:10,
15, 16, 21; 28:11; 30:12,
16; 32:7, 19, 21; 33:2, 3;
34:12; 35:2; 36:14; 37:16;
38:2; 39:6; 40:13; 41:9;
43:13; 46:7, 21; 48:2; 49:1,
16, 21; 50:17; 51:2, 3, 8
hopefully 19:4
hoping 22:3; 23:4
huge 11:14, 14; 26:16
hypothetical 12:22

I

idea 5:17; 17:12; 38:5
ideas 34:19, 21
identifies 46:17
illogical 4:11
Illumina 23:19
imagination 30:8
implicated 12:18
important 4:4; 14:3; 15:3,
11, 13; 16:11; 21:6; 27:22
inclined 6:5; 17:24; 18:1;
19:14, 23; 20:5
indicated 19:13; 32:1
inequitable 31:8
information 7:14, 15;

10:13; 15:2; 42:2; 45:21
infringe 16:18, 20; 18:6;
21:14
infringement 6:3; 8:16;
15:11, 13, 16; 16:12, 15;
17:24; 18:3, 7; 20:19; 21:9,
11; 24:1, 22; 25:6, 14;
26:7; 29:6; 30:6, 23; 49:7
infringing 26:13
injury 16:14
instance 43:21
insufficiency 26:11
Integrations 7:1, 6, 9; 12;
13:11; 20:22; 26:12; 32:8;
46:7
intelligently 41:24
intend 4:13
interest 29:15
interested 15:8; 36:10
interpose 35:16
into 11:19; 30:13
invalid 16:17, 21, 22
invalidity 6:1; 15:16;
16:12; 29:7; 31:1, 9
investigated 9:20
investigation 7:5; 11:9
involved 43:1
issue 6:21; 7:21; 8:2, 5;
9:8; 10:23; 11:10; 15:3;
17:4, 7; 19:1; 26:10; 31:7,
12; 33:4; 34:12; 36:17;
42:5; 43:13, 15; 46:24;
48:3
issues 6:12, 22; 7:19;
8:13; 11:11; 16:5, 6; 17:1,
8, 13, 23; 18:16; 20:18;
24:9; 36:21; 46:17
item 46:8; 48:17, 18
iteration 43:23; 44:14;
45:17

J

jail 14:8
Judge 14:21; 15:22; 17:9;
21:21; 23:6; 29:16; 30:2
July 38:18; 39:14; 44:3
June 39:14; 49:22
juries 8:19, 21; 18:2
jury 4:22; 5:7, 17; 8:19;
16:13, 16; 17:5, 14, 15, 16;
20:20, 21; 21:3, 8, 15;
26:6, 11; 27:23; 31:11, 16,
17, 18; 35:12, 13

K

keep 45:22
keeping 36:10
key 13:11
kill 23:3
Kim 9:13, 14
Kim's 11:5

kind 15:14; 17:10; 36:10;
47:20
knowing 6:3
knows 26:18

L

large 13:15
last 9:17; 12:8; 39:1;
41:18; 43:12
late 43:9
later 5:7; 20:21; 24:7
law 21:12; 45:11
lawyers 5:10; 15:18;
44:13; 45:2, 16, 23; 47:10
lays 17:15
learned 39:3; 42:19;
45:20
least 5:14; 10:1; 18:23;
20:7; 27:23; 28:1; 43:20;
44:5
leaving 12:16
left 8:3
legal 47:2
letter 37:11; 46:12, 18;
49:22
letters 49:11; 51:6
liability 37:7, 8; 38:17;
40:18, 20; 48:21; 49:6
light 36:15
likely 29:18
liminae 33:4, 5; 39:21;
40:14, 22; 46:4, 24; 47:24;
48:7; 51:6
limit 38:12; 47:15
limited 6:17; 40:9
lines 31:24
list 17:20, 21; 31:5, 6;
46:7
listed 4:12; 46:15
listen 18:18; 31:11
litigation 38:6
little 4:13; 9:12; 23:9;
28:24, 24; 29:15; 37:1, 24;
38:1; 43:23; 44:15; 46:1
live 15:16; 19:15
locked 37:15
logically 4:21
long 17:15; 21:3; 22:19;
29:7; 30:12; 37:18
longer 22:5
look 15:15; 33:17; 35:22;
39:22; 46:5; 47:16; 48:4;
51:6
looking 16:1; 32:5
looks 31:5; 40:17
lose 40:14
loss 11:14; 13:6
lost 12:1, 9, 9; 13:3
lot 15:7; 16:8; 34:4; 35:23;
36:5; 43:1
love 40:5
low 47:11

Lucent 22:16

M

Maher 14:21; 17:9
maintain 35:21; 47:8
major 22:1
makes 8:15
malpractice 38:23
manually 22:13
manufacture 9:16
manufactured 9:9, 23;
11:3
manufacturing 6:17;
9:6; 10:2, 23; 11:6; 20:13
many 4:7; 25:8
March 26:14; 43:9
markman 26:1; 43:8
Martese 24:1
material 8:5; 13:14
matter 21:2; 45:19
matters 20:1
may 5:19; 6:6, 21; 9:6, 15;
19:11, 19; 20:5; 29:10
maybe 5:14; 11:21;
15:17; 17:3, 3; 18:8; 22:5;
23:9; 24:23; 40:13; 50:16
mean 13:19, 22; 35:23;
36:7; 45:2, 18
meaningful 27:5; 28:4
measure 25:18
medical 38:23
meet 7:17
members 13:11
mentioned 22:2
middle 32:14
might 5:6; 8:20; 28:13;
45:14
million 9:21; 12:1, 3, 6, 9,
11, 12, 15; 14:10
mind 8:19; 16:23; 39:23
minimally 34:9
minor 9:1; 11:16
mistril 36:2
mock 40:16
modified 41:17
moment 29:12
Monday 30:22; 33:16, 22,
24
month 18:8
more 4:18; 12:6; 25:12;
28:4, 24, 24; 30:7; 37:1;
43:1, 5
motion 22:18; 33:5;
40:14, 22; 46:4, 23; 48:7,
7, 14
motions 33:4; 39:20;
46:15; 47:23; 51:6
move 6:21
much 13:9; 22:3; 24:9;
25:18; 30:18; 46:22
mullet 14:22

multiple 29:24
myself 16:10

N

NASDAQ 7:16, 19
near 32:14
necessary 30:10
need 4:9; 5:6, 9; 6:15;
7:11; 9:2; 16:19; 19:3, 8;
22:12; 24:9; 25:24; 26:9;
30:14; 31:14; 40:16;
44:14, 15; 50:5, 7
needed 24:10; 43:5
negotiation 12:22
neither 13:24
nervous 25:21; 45:7, 8, 9
new 21:16; 22:18; 34:22;
35:7; 38:10; 41:6; 42:16;
45:1, 21
next 25:12, 15; 40:16
nice 14:19
nicely 21:14
Nonetheless 30:3
nonoperating 20:10
nor 13:24
notice 42:5, 6
notified 7:7
November 19:10; 24:5,
13; 25:10; 26:2, 5, 7;
29:15, 17; 30:4
nuance 35:7
number 6:13; 16:7;
25:17; 26:23; 27:5; 34:17
numbers 11:17; 14:11;
18:23; 19:2, 4

O

object 40:8
objection 35:17, 21
objections 5:19
obviously 17:1; 18:20;
24:11
obviousness 41:12;
42:5, 18, 21
occurred 10:3
October 19:9; 22:22, 23;
23:7, 14, 14, 16, 18, 18,
24; 24:4; 29:17, 20; 30:5,
13, 20, 22
off 8:8; 14:23; 15:22;
18:15, 21; 38:15
offer 4:9
offered 5:19
offering 38:13
office 15:19
officer 8:1
once 28:5; 30:16; 44:2
one 8:16; 10:1, 3; 11:3;
15:6; 20:20, 20, 24; 21:11;
22:6; 24:21; 26:9; 27:15,
15, 17; 31:16; 34:18, 20;

37:3; 39:20; 40:23; 43:21,
22; 45:5; 47:6, 12; 48:2, 6,
12; 49:19
ongoing 6:12; 7:4; 36:16,
22
only 17:13; 24:21, 23;
25:22; 27:3, 16; 46:15;
49:6
open 45:3
opened 38:1
opening 47:19
operating 20:11
operation 39:1; 41:19
opinion 35:7, 8; 38:13,
21; 41:17
opinions 39:24; 41:2, 6;
42:2
opportunity 20:9; 35:9;
42:1, 7; 43:3, 4, 10, 16
option 11:11; 20:9
options 7:24; 10:19
order 4:1, 12, 22; 5:8, 21;
25:17; 26:12; 28:8, 18, 23;
31:24; 32:2; 37:9; 41:3;
44:9, 20; 51:5
ordered 9:15; 24:18;
34:22
originally 41:10
others 17:11; 47:17
ought 16:13, 14, 16;
18:20
out 5:2; 6:22; 9:13, 17, 21;
12:16; 14:11, 15, 17; 22:1,
6; 26:4; 27:15; 44:16;
50:12
outcome 21:4, 5
outside 31:15; 35:19
over 11:15; 13:12; 19:20;
31:17; 35:4; 39:20; 40:8
overflow 30:13
overlap 17:3
overlapping 16:8

P

p.m 51:11
package 45:22
page 12:8
pair 26:22
paired 27:1, 2; 28:3; 30:1
pairing 27:17; 29:8
papers 9:7
part 5:8; 11:3; 22:22;
42:24
particular 11:3; 39:23
particularly 6:24; 35:8,
13
parts 9:22; 11:3; 28:17
past 34:14
patent 5:5; 15:19, 24;
16:7, 17, 24; 18:6; 20:14;
21:13; 24:1; 27:18; 28:1, 2;
44:6

patents 15:14; 16:20, 22;
27:15, 21; 29:24
pays 36:3
people 18:12; 21:16;
29:14; 45:12
per 27:15, 18
percent 11:2, 18; 44:12;
45:23
percentage 11:2
perfectly 8:14
perhaps 30:9; 35:1
permutations 27:24
person 16:17; 39:23
persuaded 15:7
pick 5:22; 37:2, 3
piece 38:10; 41:16;
42:16; 45:1
pieces 45:6
piling 48:23
plaintiff's 6:24
planned 4:17
play 34:22; 44:15
plenty 19:10; 39:14
point 6:23; 8:24; 10:8;
18:24; 19:1, 13; 36:19;
39:3, 22; 41:15
portions 10:17
possibly 16:15
post 31:12; 35:20
Power 7:1, 5; 9:12; 13:11;
20:22; 23:19, 21; 26:12;
32:8; 46:7
practice 34:24; 35:11;
36:13; 45:2
prejudice 21:17
prejudicial 6:4, 5; 16:9, 9
prepare 39:2; 41:4, 24
prepared 27:5; 41:21;
42:15, 18
preparing 40:19
present 29:6; 30:21;
31:14
presentation 21:18
presented 5:16; 22:13;
31:15
preserve 42:8; 43:7; 49:1
pressure 18:11; 47:11
pretrial 4:1; 5:8; 9:7;
25:17; 26:11; 28:5, 18, 23;
30:17; 31:22, 24; 32:2, 4,
16; 33:10, 12, 14, 18; 37:9;
50:7
pretried 17:22
pretry 4:2
pretty 16:10; 21:24; 48:9
price 11:15; 12:2, 10;
13:4
prior 7:8, 9; 37:18; 38:10;
41:12, 16, 22; 42:6, 16, 20;
45:1, 6
probably 20:24; 30:1;
33:15; 39:13
problem 39:16

procedure 44:20; 45:11
produced 11:7
product 11:18; 26:21;
27:24
products 9:10; 26:13, 19;
27:3, 6, 11, 11
profession 14:12, 17;
47:2
profit 12:24; 13:6; 20:11
profits 11:14; 12:2, 9, 9;
13:3
prohibiting 28:8
proof 4:22
proposal 20:19
proposed 5:21; 37:9
propound 6:16
prosecutor 14:4
provide 6:16; 7:20
provided 6:20; 39:10;
41:13
Puerto 23:20
punch 47:3, 9, 12
purpose 31:11
purposes 30:21; 45:18
push 50:16
pushed 46:1
pushing 8:7; 37:23
put 5:10; 18:20; 40:7;
44:16; 50:18; 51:4
puts 21:14; 36:5
putting 4:21

Q

quarterly 7:3, 10; 50:11
quick 46:9
quite 8:15

R

raise 26:9; 48:2
range 22:8
rape 14:7
rather 11:16; 16:5; 17:2;
43:17
read 12:1; 33:13; 35:14
ready 18:14
real 14:3, 19; 16:23; 17:3;
21:14; 27:4, 9; 45:10
really 5:9; 10:20; 14:5;
15:22; 17:21; 22:20; 32:8;
34:21; 36:11; 38:6; 46:2
reasonable 12:11, 17,
23, 23; 13:2; 28:14
reasonably 21:22
reasoned 16:23
rebuttal 4:16, 17, 19; 5:1;
43:1; 44:16
recall 9:15
recess 51:10
recognize 27:22; 28:16
record 5:6, 9; 14:23

redoing 40:20
referred 9:5
regard 5:24
regarding 7:20
related 6:22; 8:2; 20:10;
42:21; 48:20
relates 7:23; 8:5; 48:2
relating 9:6
relevance 12:18
relevant 10:13; 13:1;
20:4
relied 7:22; 10:17; 19:3
relies 7:1
rely 20:15
remember 19:19; 24:8
report 13:6; 34:13, 23;
35:14, 19, 20, 20; 36:22;
37:15, 19, 22; 39:13; 40:1,
7; 41:2, 5, 7, 10, 23; 42:3;
43:1; 48:16
reports 6:20; 7:3, 3, 7, 8,
9, 10, 10, 21; 35:5; 36:15,
19; 38:20; 40:10, 10; 44:1,
2; 48:8; 49:8; 50:11
request 29:19; 38:1
required 10:5
requires 30:18
resigned 8:3
resolve 34:17
respect 6:12; 10:11, 23;
11:10; 13:7; 48:14
respond 8:24; 20:19;
44:17
response 42:24
restated 7:12
restatement 13:9
restatements 13:21
result 9:24; 20:16
retiral 22:17, 18
revenues 20:12
revise 22:12
revised 10:16; 22:12;
30:16; 31:23
Rico 23:20
right 6:12; 13:24; 17:15;
18:15; 30:20; 32:14, 22;
34:7, 18; 43:7; 44:1; 49:9,
23
Robinson 21:21; 23:7;
29:16; 30:2
route 15:9
royalty 12:11, 17; 13:2
rule 35:10
rules 44:19
ruling 35:15
rulings 33:12, 18
run 24:14
runs 44:18

S

sales 11:16
same 8:4, 19; 19:5; 34:13;

46:22, 24
saw 37:9
saying 9:11; 10:10;
13:13; 15:1; 25:11, 22;
37:12
SCC 7:3, 7, 9; 10:15, 17;
13:13
schedule 9:3; 33:6;
49:12; 50:2
scheduled 23:21; 26:2
schedules 32:4
scheduling 24:15; 29:12;
41:3; 44:9, 20
Scherk 48:10
SCHERKENBACH 8:11;
13:8; 14:1, 13, 16, 21;
19:12; 20:6; 21:19; 22:9;
23:2; 26:1, 17; 29:11, 14,
23; 30:15; 31:20; 32:7, 20;
33:2; 34:11, 16; 37:5;
39:18; 46:6, 11, 16; 47:6;
48:1, 11, 19; 49:15; 50:3,
9, 13; 51:1, 7
school 45:11
scope 10:21; 34:13
second 15:9; 16:16;
17:14; 18:17; 21:3; 22:6;
30:13; 31:22; 32:2, 3, 15;
36:4; 46:8
section 31:9, 17
seem 4:11; 17:6; 29:14
sees 30:16
seller 12:23
send 31:10; 37:11
sense 8:15; 41:8
separate 16:6, 12; 18:2
separating 6:2; 20:18
separation 16:4; 17:8,
23; 24:9
September 22:3, 4, 15,
21; 32:3, 5, 9, 17, 23; 33:6,
22
serious 35:12
seriously 6:2
set 5:2; 18:16, 23; 22:19;
31:3, 22; 33:11; 39:7
sets 28:18
settle 18:12
settlement 18:13
seven 24:2; 25:23
Seventh 17:5; 20:23
several 9:17, 21
share 23:22
short 46:12, 18
shortly 9:4
shot 41:13
show 20:17
showed 41:6
showing 20:8
shown 5:7
side 35:8; 36:1, 3; 40:18
sides 4:3; 17:2; 21:18;
27:8; 31:2; 36:14
sideshow 10:12, 20;

19:21
significant 10:7
similar 46:23
simply 36:2; 38:9
single 11:1
six 25:13
skeptical 9:12
skewed 34:10
solve 46:2
somebody 14:8
someone 17:15; 43:11
sometimes 5:11
soon 14:12
sorry 49:21
sort 10:5, 6; 17:2; 22:8;
24:4; 45:24
SPEAKER 6:9
spend 31:16
spotting 14:22
spread 18:2
stand 13:8; 43:11
start 23:9; 25:23
Starting 23:18
starts 41:22
State 11:19; 28:5
statement 10:8
statements 7:2; 10:15;
13:4, 13; 26:21
stay 19:21
steal 14:9
still 6:13; 13:3; 17:16;
27:19; 36:17
stock 7:23; 10:18; 11:11;
20:9
stomach 17:7
straight 35:4
stretch 30:8
strike 43:18
strongly 17:24
stuck 38:12
stuff 14:3; 48:20
subject 7:14
submit 31:23
submitted 45:6
subrogation 8:22
substantial 8:21
substantially 36:9; 39:24
substantiative 8:12
substitute 20:1
sudden 41:22
sue 23:19, 20
sues 24:1
suggest 8:14
suggested 6:9, 10
summer 15:24; 39:7;
43:12
Sun 23:19
supplement 36:23;
38:20; 39:12
supplemental 19:24;
36:15

supplemented 41:11
supplementing 40:1
suppose 8:22
supposed 39:2
sure 14:6; 37:20; 39:9,
11, 12; 40:5; 46:14; 47:4, 5
surgeon 38:24; 41:17
surprise 43:10
surprised 9:18; 43:2
surprises 4:15
system 47:9

T

Tab 12:8; 46:7, 10; 47:14;
49:10, 11
talk 8:22; 16:11; 19:8;
21:10; 39:1; 50:1
talking 8:20; 11:21; 19:9;
28:8; 41:22; 45:5; 48:20
talks 43:11
technologies 27:19
ten 25:6
tend 6:21; 21:23
tends 21:23
terms 8:7, 7; 12:21;
20:18; 47:18, 19
test 5:11
testified 37:21
testify 28:20
testifying 5:13; 35:19
testimony 4:9; 5:16;
11:5; 35:16; 38:21; 39:10
thinking 6:2; 19:7; 22:7
third 23:3, 16
thirty 24:7
thorough 28:5
though 6:23; 21:4; 27:20
thought 12:1; 14:4, 5;
16:4; 21:22
three 14:8; 23:8; 24:23;
26:16; 27:4, 20
throw 48:22
Thursday 32:23
tightened 5:20
today 19:24; 20:3; 28:16;
46:3; 49:18
together 24:11
told 9:19; 19:24; 21:4;
37:12; 40:2
tone 28:18
total 11:23
toward 17:24
track 19:22
trademark 15:19
train 23:4
traveling 32:13
treatise 44:6
trebled 11:23
trial 5:22; 8:16; 16:1;
17:15; 18:15, 17; 19:7, 9;
20:5, 20; 22:4, 18; 23:6,

22; 24:10; 25:7; 29:16, 22;
30:7, 10, 18; 31:13; 32:6;
33:11; 34:22; 35:5, 11, 12,
21; 36:4, 4, 8, 12, 18;
37:12; 38:15, 18; 40:16,
19; 42:9; 43:15; 44:6, 8;
45:22
trials 16:7; 17:5
tried 27:7; 31:9
triggered 11:8
Trilogen 23:24
Troxel 48:15
true 11:12, 13; 12:24
truly 45:20
truth 10:9
try 15:23; 16:24; 18:5;
25:7
trying 38:8; 43:6, 17
turns 9:13, 21
twenties 12:3
twice 7:19
two 6:15; 9:1; 13:10;
15:24; 18:2; 23:17; 24:3;
27:16; 28:23; 29:23; 30:1,
3; 31:17; 45:6
tying 9:2
Typically 25:5; 33:9

U

U.S 6:16; 9:10, 17, 23;
10:2, 23; 11:4, 6, 16, 21
ugliness 28:17
unaware 10:24
under 12:8; 21:12; 35:10;
47:14; 48:17
understandable 36:20;
44:14
understood 14:4
undisclosed 6:18; 48:8
unduly 6:4; 16:9
United 11:19
unless 15:10, 16; 26:5;
34:9
unnamed 6:19
unreliable 7:8, 11; 19:3
untimely 48:7, 16
up 5:20; 7:18; 12:6, 7, 8;
13:8; 14:18, 22; 17:7;
22:15; 24:4; 25:12; 33:5;
35:4; 38:1, 4, 20; 40:11;
41:6; 45:3; 47:19; 49:9;
50:2, 4
upon 7:1, 22; 13:5; 19:3
use 28:21
used 14:3, 21; 36:7
usually 28:18

V

valid 15:14
validity 6:1; 8:16; 18:1, 5,
8; 20:20; 21:13, 17, 18;

25:6; 30:10; 43:15; 49:7
value 26:22
variance 35:22; 36:20
vary 13:10
verdict 15:10, 12; 18:3;
36:11
versus 22:16; 28:1; 45:10
view 10:11; 41:10; 44:7,
12, 18
violates 17:4, 14
violation 41:3
volume 5:4

W

wait 49:5
wants 23:19, 20, 24;
38:24
way 8:13; 15:14; 16:24;
17:17; 23:10; 26:6; 27:9;
29:7; 34:13; 47:1
week 23:11, 14, 18, 23;
24:5, 5, 11, 12, 13, 14, 21;
25:10, 12, 15, 22; 29:19,
21; 30:5, 9, 13; 32:14;
33:23; 37:11; 39:1; 41:18;
43:12; 46:18; 49:13
weekend 40:16
weeks 9:18; 23:8, 17;
24:3; 30:1, 4; 32:6; 50:7
weigh 29:10
weren't 41:7
what's 20:4; 23:13;
31:15; 43:7; 46:4
who's 5:13; 28:19
whole 27:6
whose 9:14
wife 23:2, 15
willing 16:5; 18:18; 19:22
window 40:9
wish 42:7
without 6:3; 21:4; 40:1
witness 4:17, 18, 19; 9:5;
17:20; 25:17, 19; 28:19;
29:4; 31:5, 15; 35:18; 36:8;
37:12; 41:1; 43:11; 44:24
witnesses 4:6, 10, 16;
5:12; 29:3; 31:17
words 33:20
work 17:20, 21; 23:8;
24:16; 30:4, 10; 33:1;
50:10
worked 21:22
working 14:10; 34:20
workout 25:3
works 27:15; 34:21
world 44:22; 45:10, 18
worldwide 11:20
worry 18:12
worth 11:20
wrap 50:4
wreck 23:5
write 33:14

written 17:11; 44:5
wrote 17:10

Y

year 15:17
years 14:6, 8, 10
yellow 48:23
yesterday 38:5

Lawyer's Notes

06-15-2006 16:04

FISH & RICHARDSON P.C.
Wilmington, DE

[Yahoo!](#) [My Yahoo!](#) [Mail](#)

Search the Web

YAHOO! FINANCE [Sign In](#)
 New User? [Sign Up](#)

[Finance Home](#) - [Help](#)

[Home](#) [Investing](#) [News & Commentary](#) [Retirement & Planning](#) [Banking & Credit](#) [Loans](#) [Taxes](#)

[Special Editions](#) [Columnists](#) [Personal Finance](#) [Investing Ideas](#) [Markets](#) [Company Finances](#) [Providers](#)

Get Quotes

GO

Symbol Lookup | Finance Search

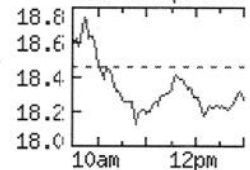


SCHWAB ACTIVE TRADER
GO

7 Trades **Scottrade**

Related Q

FCS 11-Apr 1:1



FCS 18.23 -

[View Detailed](#)

Delayed 20 m

[Providers](#) - [Dis](#)

Press Release

Source: Fairchild Semiconductor

Fairchild Semiconductor Files Patent Infringement Lawsuit Against Power Integrations, Inc.

Tuesday April 11, 12:36 pm ET

SOUTH PORTLAND, Maine--(BUSINESS WIRE)--April 11, 2006--Fairchild Semiconductor (NYSE: [FCS](#) - [News](#)) announced today that it has filed a patent infringement lawsuit against Power Integrations, Inc. in the United States District Court for the Eastern District of Texas.

ADVERTISEMENT

[Cameras](#)

[MP3 Players](#)

[Shoes](#)

[Cell Phones](#)

[Handbags](#)

[Laptops](#)

The lawsuit asserts infringement of U.S. Patent No. 5,264,719 by Power Integrations' pulse width modulation (PWM) products. Fairchild intends to take all possible steps to seek a court order to stop Power Integrations from making, using, selling, offering for sale or importing the infringing products into the United States and to obtain monetary damages for Power Integrations' infringing activities.

Fairchild and Power Integrations have been in litigation since 2004 in the United States District Court for the District of Delaware. This lawsuit is a separate action filed in the United States District Court for the Eastern District of Texas.

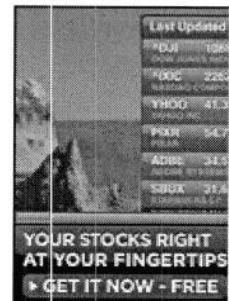
"What Power Integrations has not been able to achieve in the marketplace, they have sought to achieve in the court room. We are forced to respond in kind. However, in our case, Fairchild is asserting a patent that pre-dates Power Integrations' patents by at least fifteen months," said Tom Beaver, Fairchild's executive vice president for Worldwide Sales and Marketing. "We believe Power Integrations' products are infringing the '719 patent. We will take all possible steps to bring Power Integrations' infringement to a stop and to be made whole for the damages they are inflicting."

Intersil Corporation owns U.S. Patent No. 5,264,719, for High Voltage Lateral Semiconductor Devices, and is a co-plaintiff with Fairchild in the lawsuit. Fairchild has held license rights under the patent since 2001 and more recently secured exclusive rights to assert the patent against Power Integrations.

About Fairchild Semiconductor:

- [MagnaChip Name Executive as SVP Sales](#) - PR Newswire (
- [Fairchild Semiconductor Announces Conference First Quarter 2006 Results](#) - Business Wi
- [UPDATE - RESEARCH ALERT-Credit Sui Micro, 3 others - at \(Wed Apr 5\)](#)
- [Fairchild Semiconductor 2.0 Switch with Inc Highest 8kV ESD Ideal for Port Isola Portables](#) - Business

- By industry: [Semic Integrated Circuits](#)



Top Stor

- [Viox Plaintiff Gets to Appeal](#) - AP (11:22

Fairchild Semiconductor (NYSE: [FCS](#) - News) is the leading global supplier of high-performance power products critical to today's leading electronic applications in the computing, communications, consumer, industrial and automotive segments. As The Power Franchise®, Fairchild offers the industry's broadest portfolio of components that optimize system power. Fairchild's 9,000 employees design, manufacture and market power, analog & mixed signal, interface, logic, and optoelectronics products. Please contact us on the web at www.fairchildsemi.com.

- [Gas Costs Expected to Rise High This Summer](#)
- [Stocks Slide on High Oil Prices](#) - AP (12:38 pm)
- [Skilling Denies Spouse's Conspiracy](#) - AP (11:30 am)

Contact:

Fairchild Semiconductor:
Fran Harrison, 207-775-8576
Corporate Communications
Fax: 207-775-8161
fran.harrison@fairchildsemi.com

or

Agency Contact:

CHEN PR

Julianne Greenwood, 781-672-3137

Fax: 781-466-8989

jgreenwood@chenpr.com

- [Most-emailed article](#)
- [Most-viewed article](#)

RSS Feeds

Add headlines to your personalized My Yahoo! ([About My Yahoo!](#) and [RSS Feeds](#))

[FCS Headlines](#)

[Semiconductor - Integrations Headlines](#)

[More Finance RSS Feeds](#)

Source: Fairchild Semiconductor

 [Email Story](#)

 [Set News Alert](#)

 [Print Story](#)

[Search News](#)

Sponsor Results

Homeowners - Don't Miss Out

\$145,000 mortgage for \$484 per month. Refinance while rates are still low.
www.lowermybills.com

2.75% Fixed Student Loan Consolidation

70% lower student loan payments - fixed rate, no fees, qualify in one minute.
www.nextstudent.com

Donate Now - Food Saves Lives

Your donation of \$30 will provide \$240 worth of food in East Africa. Help now.
www.worldvision.org

[\(What's This?\)](#)

Copyright © 2006 Yahoo! Inc. All rights reserved. [Privacy Policy](#) - [Terms of Service](#) - [Copyright Policy](#) - [Ad Feedback](#)
Copyright © 2006 Business Wire. All rights reserved. All the news releases provided by Business Wire are copyrighted. Any forms of copying other than an individual user's personal reference without express written permission is prohibited. Further distribution of these materials by posting, archiving in a public web site or database, or redistribution in a computer network is strictly forbidden.

Exhibit B

To Fairchild's Supplemental Response to Power Integrations' First Set of Interrogatories
June 30, 2005

'075 Patent	U.S. Patent 5,264,719
1. A high voltage MOS transistor comprising:	<p>U.S. Patent 5,264,719 ("719 Patent") describes and claims "A high voltage MOS transistor comprising:". '719 Patent, Claim 8.</p> <p>The '719 Patent describes a high voltage MOS transistor. "The present invention provides an improved lateral drift region for both bipolar and MOS devices where improved breakdown voltage and low ON resistance are desired." '719 Patent, Abstract.</p> <p>"The present invention relates to lateral semiconductor devices and an improved method of making lateral semiconductor devices. More specifically, the invention relates to high voltage lateral devices with reduced ON resistance and a method of making such devices." '719 Patent, 1:12-16; see Figure 10 ("Figure 10 is a cross section of an MOS device, including the lateral drift region and top gate of the invention, in a preferred embodiment." '719 Patent, 3:18-20).</p>
a semiconductor substrate of a first conductivity type having a surface	<p>The '719 Patent describes and claims "a semiconductor substrate of a first conductivity type having a surface,". '719 Patent, Claim 8.</p> <p>An N-type semiconductor substrate (11) with a surface is shown in Figure 10. "Around the entire periphery of the drift region there is a curved portion 17_e which rounds up to the surface of the N⁻ substrate 11 to insure that the JFET channel in the drift region 17 contacts the MOS channel 11_b under the MOS gate 16." '719 Patent, 6:52-56.</p>
a pair of laterally spaced pockets of semiconductor material of a second conductivity type within the substrate and adjoining the substrate surface,	<p>The '719 Patent describes and claims "a pair of laterally spaced source and drain pockets of semiconductor material of a second conductivity type within the substrate and adjoining the substrate surface,". '719 Patent, Claim 8.</p> <p>P-type source and drain regions (14 and 12) (a pair of laterally spaced pockets of semiconductor material of second conductivity type) within substrate (11) and adjoining the substrate surface are shown in Figure 10. "For the MOS device, the drain 12 is surrounded by the P⁻ drift region 17 and N type top gate 21." '719 Patent, 6:50-52. "The P⁺ source 14 and</p>

Exhibit B

To Fairchild's Supplemental Response to Power Integrations' First Set of Interrogatories
June 30, 2005

'075 Patent	U.S. Patent 5,264,719
	N ⁺ body contact 11 _c are shown as is the dielectric 13 which serves as the gate oxide 13 _g beneath the MOS gate 16." '719 Patent, 6:59-61
a source contact connected to one pocket,	A source contact is necessarily connected to the source pocket (14) in order for the MOS device to operate.
a drain contact connected to the other pocket,	A drain contact is connected to the other pocket (drain pocket 12) in order for the MOS device to operate. "The two contacts, drain contact 12 _a and body contact 11 _c are shown for completeness." '719 Patent, 1:27-29. "FIG. 4 shows an MOS device where P ⁺ drain contact 12 _a is formed in P ⁻ type drain 12...." '719 Patent, 3:37-38.
an extended drain region of the second conductivity type extending laterally each way from the drain contact pocket to surface-adjointing positions,	<p>The '719 Patent describes and claims "an extended drain region of the second conductivity type extending laterally each way from said drain pocket to surface-adjointing positions,". '719 Patent, Claim 8.</p> <p>An extended drain region (17) of second conductivity type (P) extending laterally each way from drain contact pocket (12) to surface-adjointing positions is shown in Figure 10. "For the MOS device, the drain 12 is surrounded by the P⁻ drift region 17 and N type top gate 21. Around the entire periphery of the drift region there is a curved portion 17_e which rounds up to the surface of the N⁻ substrate 11 to insure that the JFET channel in the drift region 17 contacts the MOS channel 11_b under the MOS gate 16. The drift region 17 extends outward from the entire perimeter of the drain 12." '719 Patent, 6:50-57.</p>
a surface adjoining layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain contact pocket and the surface-adjointing positions,	<p>The '719 Patent describes and claims "a surface adjoining, top layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain pocket and the surface-adjointing positions,". '719 Patent, Claim 8.</p> <p>A surface adjoining top gate (21) of first conductivity type (N) on top of an intermediate portion of the extended drain region (17) between the drain contact pocket (12) and the surface adjoining positions is shown in Figure</p>

Exhibit B

To Fairchild's Supplemental Response to Power Integrations' First Set of Interrogatories
June 30, 2005

'075 Patent	U.S. Patent 5,264,719
	10. "For the MOS device, the P ⁺ drain 12 is surrounded by the P ⁻ drift region 17 and N type top gate 21." '719 Patent, 6:50-52.
said top layer of material and said substrate being subject to application of a reverse-bias voltage,	<p>The '719 Patent describes and claims "said top layer of material and said substrate being subject to application of a reverse-bias voltage,". '719 Patent, Claim 8.</p> <p>Top gate (21) (said top layer of material) and substrate (11) are subjected to application of a reverse-bias voltage. "This top gate allows the total channel doping to be increased because the top gate to channel depletion layer holds some additional channel charge when reverse biased in addition to that held by the bottom gate to channel depletion layer of the prior art structure." '719 Patent, 2:44-49.</p>
an insulating layer on the surface of the substrate and covering at least that portion between the source contact pocket and the nearest surface-adjointing position of the extended drain region, and	<p>The '719 Patent describes and claims "an insulating layer on the surface of the substrate and covering at least that portion between the source pocket and the nearest surface-adjointing position of the extended drain region, and". '719 Patent, Claim 8.</p> <p>A insulating dielectric layer (13) on the surface of substrate (11) and covering the portion between source contact pocket (14) and the nearest surface-adjointing position of extended drain region (17) is shown in Figure 10. "The P⁺ source 14 and N⁺ body contact 11_c are shown as is the dielectric 13 which serves as the gate oxide 13_g beneath the MOS gate 16." '719 Patent, 6:59-61.</p>
a gate electrode on the insulating layer and electrically isolated from the substrate region thereunder which forms a channel laterally between the source contact pocket and the nearest surface-adjointing position of the extended drain region, said gate electrode controlling by field-effect the flow of current thereunder through the channel.	<p>The '719 Patent describes and claims "a gate electrode on the insulating layer and electrically isolated from the substrate region thereunder which forms a channel laterally between the source pocket and the nearest surface-adjointing position of the extended drain region, said gate electrode controlling by field-effect the flow of current thereunder through the channel." '719 Patent, Claim 8.</p> <p>A gate electrode (16) on the insulating layer (13) and electrically isolated from the substrate (11) is shown in Figure 10. The gate electrode (16) controls by field-effect the flow of current through channel (11_b) between source contact pocket (14) and the nearest surface-adjointing</p>

Exhibit B

To Fairchild's Supplemental Response to Power Integrations' First Set of Interrogatories
June 30, 2005

'075 Patent	U.S. Patent 5,264,719
	position of the extended drain region (17). "Around the entire periphery of the drift region there is a curved portion 17 _e which rounds up to the surface of the N ⁻ substrate 11 to insure that the JFET channel in the drift region 17 contacts the MOS channel 11 _b under the MOS gate 16." '719 Patent, 6:52-56.
5. The high voltage MOS transistor of claim 1 combined on the same chip with a low voltage CMOS implemented device.	It is inherent or would have been obvious to combine the MOS transistor described by the '719 Patent on the same chip with a low voltage CMOS implemented device.

I hereby certify that this document is being deposited with the United States Postal Service "EXPRESS MAIL" SERVICE TO ADDRESSEE" address: 1111 and and Trade Department of Patents Date: 5/24/91 By: C. D. Jones Express Mail No.: FB 1236 905 9X45

118/28508CO

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: James D. Beason
SERIAL NO.: Rule 60 Continuation Application
of USSN: 242,405, Filed: September 8, 1988
FOR: HIGH VOLTAGE LATERAL SEMICONDUCTOR DEVICE

Honorable Commissioner of
Patents and Trademarks
Washington, D.C. 20231

May 24, 1991

PRELIMINARY AMENDMENT

Sir:

Preliminary to the examination of the above-identified application, the following Amendments and Remarks are respectfully submitted.

IN THE SPECIFICATION:

Page 2, eighth line from the bottom, change "drain body" to --drain-to-body--;

Page 3, line 4, change "channel body" to --channel-to-body--;

Page 3, fourth line from the bottom, change "12" to --contact 12A--;

Page 4, first full paragraph, fifth line, change "body drain" to --body-to-drain--;

Page 9, tenth line from the bottom, change "drain body" to --drain-to-body--;

Page 9, fourth line from the bottom, change "gate to drift" to --gate-to-drift--; after "junction", insert --17A--; after "gate" (last occurrence), insert --21--;

Page 10, top paragraph, line 2, after "channel", insert --17--;

Page 10, line 5, change "body to drain" to --body-to-drain--;

Page 10, line 6, change "gate to channel" to --gate-to-channel--;

Page 10, line 7, change "additon" to --addition--;

Page 10, line 13, after "region", insert --17--;

Page 10, bottom paragraph, line 3, change "body to drain" to --body-to-drain--;

Page 10, bottom paragraph, line 4, change "gate to drain" to --gate-to-drain--;

Page 10, bottom paragraph, line 5, after "11", insert --(as shown in Figures 6A, 6B to be described below)--; change "gate to drain" to --gate-to-drain--;

Page 11, line 1, change "body to drain" to --body-to-drain--;

Page 11, line 2, change "gate to drain" to --gate-to-drain--;

Page 11, second paragraph, line 3, after "region", insert --17--;

Page 11, second paragraph, line 6, after "and", insert --N--;

Page 11, second paragraph, line 8, change "effected" to
 --affected--;

Page 12, line 1, after "and", insert --,--;

Page 12, line 2, after ")", insert --,--;

Page 12, line 9, change "ion implanted" to
 --ion-implanted--;

Page 12, second paragraph, line 3, after "channel" (first
 occurrence), insert --17--;

Page 13, line 1, after "region", insert --17--; after
 "gate", insert --21--;

Page 13, line 2, after "oxide", insert --53--;

Page 13, line 13, after "gate" (last occurrence), insert
 --21--;

Page 14, line 7, after "17", insert --,--;

Page 14, second paragraph, line 8, change "so" to --as--;

Page 14, second paragraph, line 11, after "11", insert
 --, via contact region 11C--;

Page 15, first full paragraph, line 4, before "top", insert
 --N type--;

Page 15, line 8, change "gate to drift" to --gate-to-
 drift--;

Page 15, line 9, after "region" (last occurrence), insert
 --123--;

Page 15, line 10, after "negative", insert --,--;

Page 16, bottom paragraph, first line, change "base to" to
 --base-to-";

Page 16, bottom paragraph, line 4, after "gate", insert
 --126A--; after "region" (last occurrence), insert --123A--;

Page 16, bottom paragraph, line 6, after "region", insert
--123A--;

Page 16, bottom paragraph, line 7, change "ro" to --for--;

Page 17, line 3, after "shield", insert --121--;

Page 17, first full paragraph, line 5, after "region",
insert
--17--;

Page 18, first full paragraph, line 3, after "contact",
insert
--11C--;

Page 18, last paragraph, line 1, change "in" to --by way
of--; after "second", insert --(surface)--;

Page 18, last paragraph, line 2, change "217," to --217--;
before "prior", insert --(deeper)--; after "region" (last
occurrence), insert --217A--;

Page 18, last paragraph, line 3, change "as shown" to
--, refer to above--;

Page 18, last paragraph, line 4, after "region", insert
--11--; before "layer", insert --top gate--;

Page 19, line 2, change "region" to --body 11--;

Page 19, line 3, after "layers", insert --217, 250
respectively--;

Page 19, first full paragraph, line 3, change "region" to
--body 11--;

Page 19, first full paragraph, line 4, change "region" to
--first drift region 217--;

Page 19, first full paragraph, line 6, after "contact",
insert

--12A--; change "region" to --body 11--;

Page 19, first full paragraph, line 7, change "drain body" to

--drain-to-body--;

Page 19, first full paragraph, line 8, before "region", insert

--first drift--;

Page 20, line 3, change "layer" to --first drift region--;

Page 20, line 4, change "layer" (first occurrence) to --first drift region--; change "layer" (last occurrence) to --region--;

Page 20, line 5, change "layer" to --region 250--;

Page 20, first full paragraph, line 2, change "drain body" to

--drain-to-body--;

Page 20, first full paragraph, line 3, after "junction", insert --15--; change "P and N-" to --P N- --;

Page 20, first full paragraph, line 4, change "P to N" to --P N--; change "N and " to --N first drift region 217 and--;

Page 20, first full paragraph, line 5, change "regions" to --body 11--; after "layer", insert --250--;

Page 20, first full paragraph, line 6, change "layer" to --first drift region--;

Page 21, line 4, change "layer" to --first drift region--;

Page 21, first full paragraph, line 2, change "layers" to --regions--; change "250" to --221--;

Page 21, last paragraph, line 2, change "250" to --221--;

Page 21, last paragraph, line 3, change "region" to --body 11--; and

Page 21, last paragraph, line 4, change "region" (last occurrence) to --first drift region 217--.

IN THE CLAIMS:

Claim 1, delete without prejudice, and substitute therefor the following new claims.

--31. A semiconductor device comprising:

a semiconductor body of a first conductivity type having a first surface;

a first semiconductor region of a second conductivity type formed in a first portion of said first surface of said semiconductor body, and defining a first PN junction with said semiconductor body;

a second semiconductor region of said first conductivity type formed in a surface portion of said first semiconductor region and defining therewith a second PN junction, said second PN junction being spaced apart from said first PN junction by material of said first semiconductor region therebetween;

a third semiconductor region of said first conductivity type formed in a second surface portion of said semiconductor body, spaced apart from said first surface portion by a third surface portion thereof;

a fourth semiconductor region of said second conductivity type formed in a first surface part of said third surface portion of said semiconductor body spaced apart from said first surface portion of said semiconductor body by a second surface part of said third surface portion thereof and defining with said semiconductor body a third PN junction, said fourth semiconductor region being connected to said first semiconductor region and being contiguous with said third semiconductor region;

a fifth semiconductor region of said first conductivity type, and having an impurity concentration greater than that of said semiconductor body, formed in said fourth semiconductor region and defining therewith a fourth PN junction, said fifth semiconductor region being contiguous with said third semiconductor region;

an insulator layer formed on said first surface of said semiconductor body; and

a gate electrode formed on said insulator layer so as to overlie said second surface part of said third surface portion of said semiconductor body and material of said first and fourth semiconductor regions, that portion of said first semiconductor region lying beneath said gate electrode serving as a channel region of said device, said gate electrode having a gate voltage applied to induce a conductive channel through said first semiconductor region therebeneath; and wherein

when said device is reverse-biased, a first depletion region extends from said fourth PN junction into said fourth semiconductor region and said semiconductor body, and a second depletion region extends from said fifth PN junction into said fifth semiconductor region and said fourth semiconductor region;

said semiconductor body having a first ON resistance in a first current flow path therethrough between said second and third semiconductor regions, and said fifth semiconductor region providing a second ON resistance in a second current flow path along the surface of said semiconductor body from said second semiconductor region through said channel and said fourth and fifth semiconductor regions to said third semiconductor region, so that said fifth semiconductor region serves to provide a current flow path in parallel with said first current flow path, thereby effectively reducing the total ON resistance of the overall current flow path between said second and third semiconductor regions.

32. A semiconductor device according to claim 31, wherein a peripheral edge of said gate electrode is aligned with a peripheral edge of said fifth semiconductor region.

33. A semiconductor device according to claim 31, wherein said fourth semiconductor region overlaps said first semiconductor region.

34. A semiconductor device according to claim 31, wherein the impurity concentration said fifth semiconductor region is such that said fifth semiconductor region is completely depleted by said second depletion region at a reverse bias less than that at which said first and second depletion regions come together within and punch through said fourth semiconductor region.

35. A semiconductor device comprising:

a semiconductor body of a first conductivity type having a first surface;

a first semiconductor region of a second conductivity type formed in a first portion of said first surface of said semiconductor body, and defining a first PN junction with said semiconductor body;

a second semiconductor region of said first conductivity type formed in a surface portion of said first semiconductor region and defining therewith a second PN junction, said second PN junction being spaced apart from said first PN junction by material of said first semiconductor region therebetween;

a third semiconductor region of said first conductivity type formed in a second surface portion of said semiconductor body, spaced apart from said first surface portion by a third surface portion thereof;

a fourth semiconductor region of said second conductivity type formed in said third surface portion of said semiconductor body and defining with said semiconductor body a third PN junction, said fourth semiconductor region being connected to said first semiconductor region and being contiguous with said first and third semiconductor regions;

a fifth semiconductor region of said first conductivity type, and having an impurity concentration greater than that of said semiconductor body, formed in said fourth semiconductor region and defining therewith a fourth PN junction, said fifth semiconductor region being contiguous with said first and third semiconductor regions;

an insulator layer formed on said first surface of said semiconductor body; and

a gate electrode formed on said insulator layer so as to overlie material of said first and fourth semiconductor regions, that portion of said first semiconductor region lying beneath said gate electrode serving as a channel region of said device, said gate electrode having a gate voltage applied to induce a conductive channel through said first semiconductor region therebeneath; and wherein

when said device is reverse-biased, a first depletion region extends from said fourth PN junction into said fourth semiconductor region and said semiconductor body, and a second depletion region extends from said fifth PN junction into said fifth semiconductor region and said fourth semiconductor region.

36. A semiconductor device according to claim 34 wherein the impurity concentration said fifth semiconductor region is such that said fifth semiconductor region is completely depleted by said second depletion region at a reverse bias less than that at which said first and second depletion regions come together within and punch through said fourth semiconductor region.

37. A semiconductor device comprising:

a semiconductor body of a first conductivity type having a first surface;

a first semiconductor region of a second conductivity type formed in a first portion of said first surface of said semiconductor body, and defining a first PN junction with said semiconductor body;

a second semiconductor region of said first conductivity type formed in a second surface portion of said semiconductor body, spaced apart from said first surface portion by a third surface portion thereof and defining a second PN junction with said semiconductor body;

a third semiconductor region of said second conductivity type formed in a first surface part of said third surface portion of said semiconductor body spaced apart from said first surface portion of said semiconductor body by a second surface part of said third surface portion thereof and defining with said semiconductor body a third PN junction, said third semiconductor region being contiguous with said second semiconductor region;

a fourth semiconductor region of said first conductivity type, and having an impurity concentration greater than that of said semiconductor body, formed in said third semiconductor region and defining therewith a fourth PN junction;

an insulator layer formed on said first surface of said semiconductor body; and

a gate electrode formed on said insulator layer so as to overlie said second surface part of said third surface portion of said semiconductor body, that portion of said semiconductor body lying beneath said gate electrode serving as a channel region of said device, said gate electrode being applied with a gate voltage for inducing a conductive channel through said channel region;

said device being reverse-biased, so that a first depletion region extends from said third PN junction into said third semiconductor region and said semiconductor body and a second depletion region extends from said fourth PN junction into said third semiconductor region and said fourth semiconductor region;

said semiconductor body having a first ON resistance in a first current flow path therethrough between said first and second semiconductor regions, and said fourth semiconductor region providing a second ON resistance, less than said first ON resistance, in a second current flow path along the surface of said semiconductor body from said first semiconductor region through said channel and said third and fourth semiconductor regions to said second semiconductor region, so that said fourth semiconductor region serves to provide a reduced resistance current flow path in parallel with said first current flow path,

thereby effectively reducing the total ON resistance of the overall current flow path between said first and second semiconductor regions; and

wherein the impurity concentration said fourth semiconductor region is such that said fourth semiconductor is completely depleted by said second depletion region at a reverse bias less than that at which said first and second depletion regions come together within and punch through said third semiconductor region.

38. A high voltage MOS transistor comprising:

a semiconductor substrate of a first conductivity type having a surface,

a pair of laterally spaced source and drain pockets of semiconductor material of a second conductivity type within the substrate and adjoining the substrate surface,

an extended drain region of the second conductivity type extending laterally each way from said drain pocket to surface-adjoining positions,

a surface adjoining layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain pocket and the surface-adjoining positions,

said top layer of material and said substrate being subject to application of a reverse-bias voltage,

an insulating layer on the surface of the substrate and covering at least that portion between the source pocket and the nearest surface-adjointing position of the extended drain region, and

a gate electrode on the insulating layer and electrically isolated from the substrate region thereunder which forms a channel laterally between the source pocket and the nearest surface-adjointing position of the extended drain region, said gate electrode controlling by field-effect the flow of current thereunder through the channel.

39. A high voltage MOS transistor according to claim 38, wherein said extended drain region has an impurity concentration greater than $1 \times 10^{12} \text{ cm}^{-2}$.

40. A high voltage MOS transistor according to claim 38, further including an ohmic contact region of said first conductivity type formed in a surface adjoining portion of said semiconductor substrate, said ohmic contact region overlapping said top layer of material.

41. A high voltage MOS transistor comprising:

semiconductor material of a first conductivity type having a surface,

a pair of laterally spaced source and drain pockets of semiconductor material of a second conductivity type within the substrate and adjoining the surface of said semiconductor material,

an extended drain region of the second conductivity type extending laterally from said drain pocket to a surface-adjointing position,

a surface adjoinig top layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain pocket and said surface-adjointing position,

said top layer of material and said semiconductor material being subject to application of a reverse-bias voltage,

an insulating layer on the surface of said semiconductor material and covering at least that portion between the source pocket and the nearest surface-adjointing position of the extended drain region, and

a gate electrode on the insulating layer and electrically isolated from a semiconductor material region thereunder containing a channel that extends laterally between the source pocket and the nearest surface-adjointing position of the extended drain region, said gate electrode controlling by field-effect the flow of current thereunder through the channel.

42. A high voltage MOS transistor according to claim 41, wherein said extended drain region extends in a plurality of different directions from said drain pocket to respective plural surface adjoinig positions.

43. A high voltage MOS transistor according to claim 41, wherein said extended drain region surrounds said drain pocket and extends to a surrounding surface adjoinig position.

44. A high voltage MOS transistor according to claim 41, wherein said drain pocket comprises a first relatively deep pocket of a first impurity concentration and a second relatively shallow pocket formed in a surface portion of said first relatively deep pocket and having a second impurity concentration greater than said first impurity concentration and providing a drain contact region.

45. A high voltage MOS transistor according to claim 41, wherein said extended drain region has an impurity concentration greater than $1 \times 10^{12} \text{ cm}^{-2}$.

46. A high voltage MOS transistor according to claim 41, further including an ohmic contact region of said first conductivity type formed in a surface adjoining portion of said semiconductor material, said ohmic contact region overlapping said top layer of material.

47. A high voltage field effect transistor device comprising:

semiconductor material of a first conductivity type having a surface;

a source region of a second conductivity type formed in a first surface portion of said semiconductor material;

a drain region of said second conductivity type formed in a second surface portion of said semiconductor material spaced apart from said first surface portion by a third surface portion therebetween;

an extended drain region of said second conductivity type extending from said drain region beneath a first portion of said third surface portion of said semiconductor material, to adjoin a second portion of said third surface portion of said semiconductor material, spaced apart from said second surface portion of said semiconductor material, by said first portion of said third surface portion of said semiconductor material;

a surface region of said first conductivity type formed in said first portion of said third surface portion of said semiconductor material;

an insulating layer disposed on said surface of said semiconductor material, so as to overlie a third portion of said third surface portion of said semiconductor material between the second portion of said third surface portion of said semiconductor material and said first surface portion of said semiconductor material; and

a gate electrode disposed on that portion of said insulating layer overlying said third portion of said third surface portion of said semiconductor material, and wherein said surface region and said semiconductor material are subject to the application of a reverse bias voltage.

48. A high voltage field effect transistor device according to claim 47, wherein said extended drain region extends laterally in a plurality of different directions from said drain region to adjoin said second portion of said third surface portion of said semiconductor material and to adjoin a fifth surface portion of said semiconductor material.

49. A high voltage field effect transistor device according to claim 47, wherein said extended drain region surrounds said drain region and extends to a surrounding surface-adjoining portion of said semiconductor material.

50. A high voltage field effect transistor device according to claim 47, wherein said drain region comprises a first relatively deep region of a first impurity concentration and a second relatively shallow region formed in a surface portion of said first relatively deep region and having a second impurity concentration greater than said first impurity concentration and providing a drain contact region.

51. A high voltage field effect transistor device according to claim 47, wherein said extended drain region has an impurity concentration greater than $1 \times 10^{12} \text{ cm}^{-2}$.

52. A high voltage field effect transistor device according to claim 47, further including an ohmic contact region of said first conductivity type formed in a surface adjoining portion of said semiconductor material, said ohmic contact region overlapping said surface region.

53. An integrated MOS/JFET transistor device comprising an insulated gate field effect transistor and a double-sided junction field effect transistor integrated together in semiconductor substrate which contains a source region, and a drain region formed therein, and a dual channel path formed in said semiconductor material between said source and drain regions, said dual channel path comprising an insulated gate-controlled channel region having a first conductivity type in the presence of a channel-inducing gate voltage, said insulated gate controlled channel region being contiguous with a double-sided junction channel region of said first conductivity type, and wherein said source region adjoins said insulated gate-controlled channel region and said drain region adjoins said double-sided channel region.

54. An integrated MOS/JFET transistor device according to claim 53, wherein said insulated gate-controlled channel region comprises a surface portion of said semiconductor material adjoining said source region, and wherein said double-sided junction channel region comprises an extended drain region extending laterally from said drain region beneath a top gate region to said surface portion of said semiconductor material, an underlying portion of said semiconductor material extending beneath and adjoining said extended drain region and forming a bottom gate, said top gate region and said bottom gate forming respective PN junctions with said double-sided junction channel region.

55. An integrated MOS/JFET transistor device according to claim 53, wherein said extended drain region and said double-sided junction channel region surround said drain region and extend to a surrounding surface-adjointing position.

56. An integrated MOS/JFET transistor device according to claim 53, ~~wherein said extended drain region and said double,~~ wherein said drain region comprises a first relatively deep region of a first impurity concentration and a second relatively shallow region formed in a surface portion of said first relatively deep region and having a second impurity concentration greater than said first impurity concentration and providing a drain contact region.

57. An integrated MOS/JFET transistor device according to claim 53, ~~wherein said extended drain region and said double,~~ further including an ohmic contact region of said first conductivity type formed in a surface adjoining portion of said semiconductor material, said ohmic contact region overlapping said top gate.

58. An integrated MOS/JFET transistor device according to claim 53, wherein said extended drain region has an impurity concentration greater than $1 \times 10^{12} \text{ cm}^{-2}$.

59. A high voltage MOS transistor comprising:

semiconductor material of a first conductivity type having a surface;

source and drain regions of a second conductivity type adjoining spaced apart portions of the surface of said semiconductor material;

an extended drain region of said second conductivity type extending laterally from said drain region through said semiconductor material to a surface-adjoining portion of the surface of said semiconductor material;

a top gate semiconductor layer of said first conductivity type adjoining said drain region and adjoining said extended drain region along the surface of said semiconductor material to said surface-adjoining portion of the surface of said semiconductor material, said top gate semiconductor layer and said semiconductor material being subject to the application of a reverse-bias voltage;

an insulating layer on the surface of the semiconductor material and covering at least that portion of the surface of said semiconductor material between said source region and said surface-adjoining portion of said extended drain region; and

a gate electrode disposed on said insulating layer and being electrically isolated from that portion of the surface of said semiconductor material thereunder which forms a channel laterally between said source region and said surface-adjoining portion of said extended drain region, said gate electrode controlling, by field-effect, the flow of current thereunder through said channel.

60. A high voltage MOS transistor according to claim 59, wherein said extended drain region extends laterally each way from said drain region to surface-adjoining portions of the surface of said semiconductor material, and wherein said top gate semiconductor layer extends laterally in a plurality of different directions from said drain region and adjoins said extended drain region along the surface of said semiconductor material to said surface-adjoining portions of the surface of said semiconductor material.

61. A high voltage MOS transistor according to claim 59, wherein said extended drain region surrounds said drain region and extends to a surrounding surface adjoining position.

62. A high voltage MOS transistor according to claim 59, wherein said drain region comprises a first relatively deep region of a first impurity concentration and a second relatively shallow region formed in a surface portion of said first relatively deep region and having a second impurity concentration greater than said first impurity concentration and providing a drain contact region.

63. A high voltage MOS transistor according to claim 59, wherein said extended drain region has an impurity concentration greater than $1 \times 10^{12} \text{ cm}^{-2}$.

64. A high voltage MOS transistor according to claim 59, further including an ohmic contact region of said first conductivity type formed in a surface adjoining portion of said semiconductor material, said ohmic contact region overlapping said top gate layer.

65. A high voltage diode comprising:

semiconductor material of a first conductivity type having a surface,

a first, surface-adjoining region of a second conductivity type;

a second surface-adjoining region of said first conductivity type spaced apart from said first, surface-adjoining region;

a third region of said second conductivity type extending laterally from said first, surface-adjoining region; and

a fourth, surface-adjoining region of said first conductivity type overlying an intermediate portion of said third, laterally extending and surface-adjoining region.

66. A high voltage diode according to claim 65, wherein said third region surrounds said first, surface-adjoining region and extends to a surrounding surface adjoining position.

67. A high voltage diode according to claim 65, wherein said first region comprises a first relatively deep region of a first impurity concentration and a second relatively shallow region formed in a surface portion of said first relatively deep region and having a second impurity concentration greater than said first impurity concentration.

68. A high voltage diode according to claim 65, wherein said third region has an impurity concentration greater than $1 \times 10^{12} \text{ cm}^{-2}$.

69. A lateral bipolar transistor having a high voltage base-collector diode comprising:

semiconductor material of a first conductivity type having a surface and forming a base of said bipolar transistor,

a first, surface-adjointing collector region of a second conductivity type forming a base-collector junction with said semiconductor material;

a second surface-adjointing base region of said first conductivity type spaced apart from said first, surface-adjointing collector region;

a third, extended collector region of said second conductivity type extending laterally from said first, surface-adjointing collector region, so that said base-collector junction extends laterally from said first, surface adjointing collector region;

a fourth, surface-adjointing region of said first conductivity type overlying an intermediate portion of said third, laterally extending and surface-adjointing extended collector region; and

a fifth, surface-adjointing emitter region of said second conductivity type formed in said second surface-adjointing base region and defining therewith an emitter-base junction.

70. A lateral bipolar transistor according to claim 69, wherein said third region surrounds said first, surface-adjointing region and extends to a surrounding surface adjointing position.

71. A lateral bipolar transistor according to claim 69, wherein said first region comprises a first relatively deep region of a first impurity concentration and a second relatively shallow region formed in a surface portion of said first relatively deep region and having a second impurity concentration greater than said first impurity concentration.

72. A lateral bipolar transistor according to claim 69, wherein said third, extended collector region has an impurity concentration greater than $1 \times 10^{12} \text{ cm}^{-2}$.--

REMARKS

The specification has been amended to conform with the Amendment filed July 13, 1990 in parent application Serial No. 242,405.

Original claims 1-30 have been replaced by new claims 31-72. Of these newly presented claims, claims 31-37 correspond to those claims filed in the Amendments of July 13, 1990 and January 25, 1991, in parent application Serial No. 242,405, and incorporating the Amendments of the Examiner's Amendment dated February 22, 1991. New claims 38-72 embody further definitions of subject matter for which patent protection is sought.

With respect to newly added claims 38-72, to the extent that 37 C.F.R. 1.607(c) is applicable, please be advised that claim 38, although not identically copied, is considered to be generic to the invention defined in claim 1 of U.S. Patent No. 4,811,075 to Eklund. Claims 41, 47 and 59 are also considered to be generic to the invention defined in claim 1 of the patent to Eklund, 4,811,075.

U.S. Patent No. 4,823,173, of which application Serial No. 242,405, filed September 8, 1988 is a continuation-in-part, has a filing date of January 7, 1986, the present application being a continuation of application Serial No. 242,405, it is respectfully submitted that the effective filing date of the above-identified claims is the filing date of parent Patent 4,823,173, or January 7, 1986. This filing date antedates the filing date of April 24, 1987 of the above-identified Eklund patent, 4,811,075.

Early examination of the present application is earnestly solicited.

To the extent necessary, Applicants petition for an Extension of Time under 37 C.F.R. 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including Extension of Time fees, to Deposit Account No. 05-1323 (118/28508CO) and please credit any excess fees to such deposit account.

Respectfully submitted,

Charles E. Wands
Reg. No. 25,649
EVENSON, WANDS, EDWARDS,
LENAHAN & MCKEOWN

CEW:cn
Attachment
(407) 725-4760
(202) 828-8300

pat\28508.pa



US005264719A

United States Patent [19][11] **Patent Number:** **5,264,719****Beasom**[45] **Date of Patent:** **Nov. 23, 1993**[54] **HIGH VOLTAGE LATERAL SEMICONDUCTOR DEVICE**[75] **Inventor:** **James D. Beasom**, Melbourne Village, Fla.[73] **Assignee:** **Harris Corporation**, Melbourne, Fla.[21] **Appl. No.:** **705,509**[22] **Filed:** **May 24, 1991**

4,628,341 12/1986 Thomas 357/23.8
 4,811,075 3/1989 Eklund et al. 357/46
 4,994,889 2/1991 Takeuchi et al. 357/55
 4,994,904 2/1991 Nakagawa et al. 357/38

Primary Examiner—Rolf Hille*Assistant Examiner*—Roy Potter*Attorney, Agent, or Firm*—Evenson, Wands, Edwards, Lenahan & McKeown[57] **ABSTRACT**

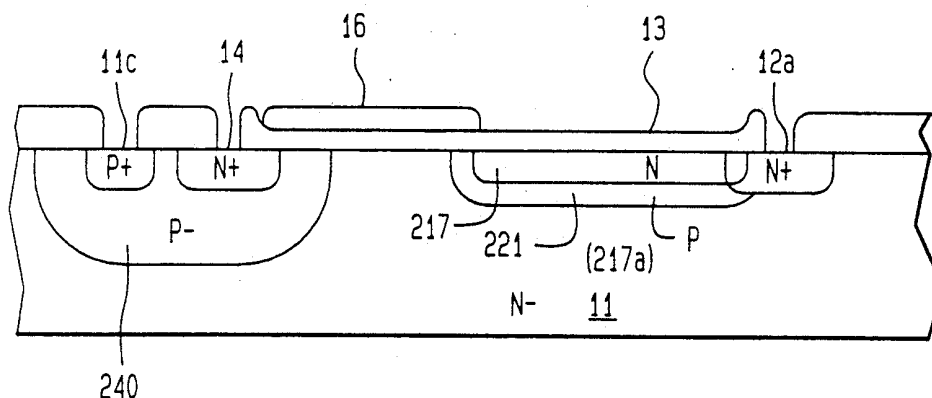
The present invention provides an improved lateral drift region for both bipolar and MOS devices where improved breakdown voltage and low ON resistance are desired. A top gate of the same conductivity type as the device region with which it is associated is provided along the surface of the substrate and overlying the lateral drift region. In an MOS device, the extremity of the lateral drift region curves up to the substrate surface beyond the extremity of the top gate to thereby provide contact between the JFET channel and the MOS channel.

Related U.S. Application Data

[63] Continuation of Ser. No. 242,405, Sep. 8, 1988, abandoned, which is a continuation-in-part of Ser. No. 831,384, Jan. 7, 1986, Pat. No. 4,823,173.

[51] **Int. Cl.⁵** **H01L 29/80**[52] **U.S. Cl.** **257/335; 257/336; 257/339**[58] **Field of Search** 357/38, 55, 23.8, 46[56] **References Cited****U.S. PATENT DOCUMENTS**

4,626,879 12/1986 Colak 357/23.8

42 Claims, 7 Drawing Sheets

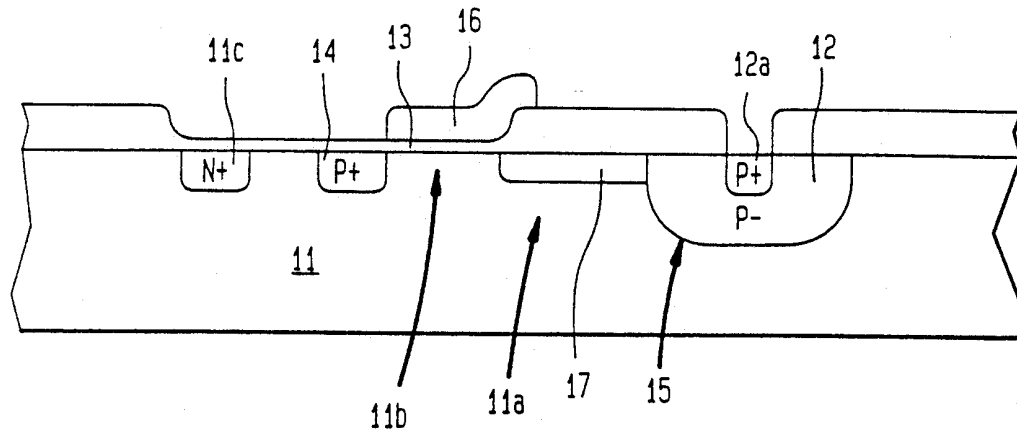


FIG. 1

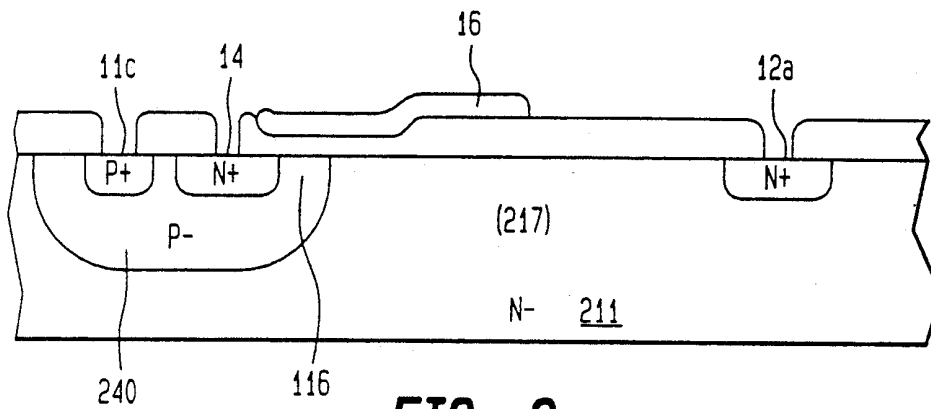


FIG. 2
(PRIOR ART)

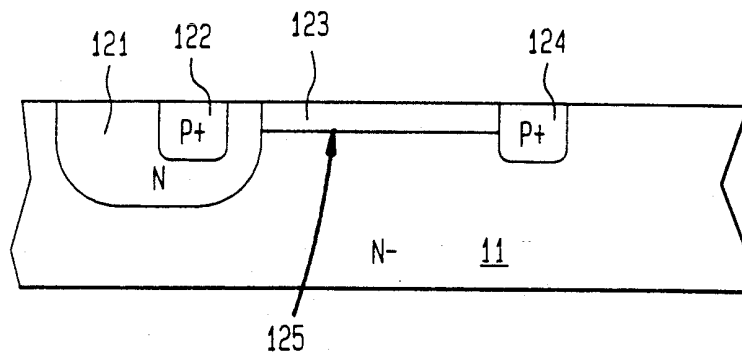


FIG. 3

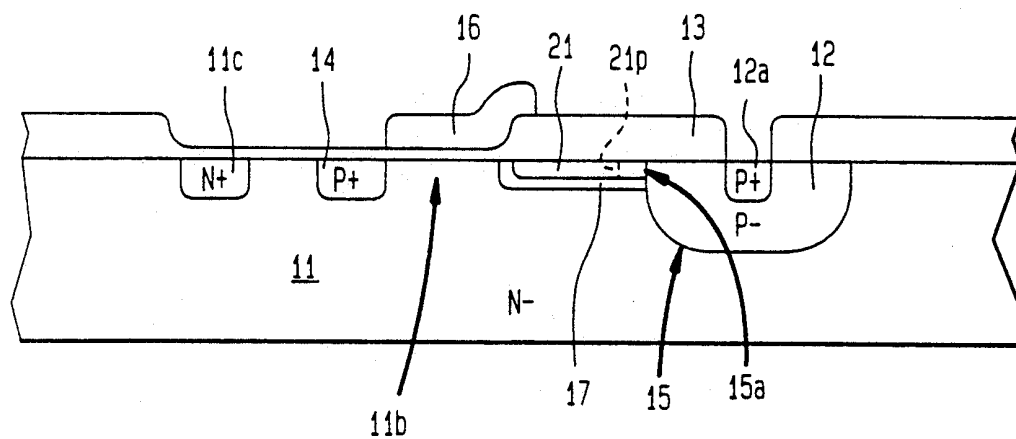


FIG. 4

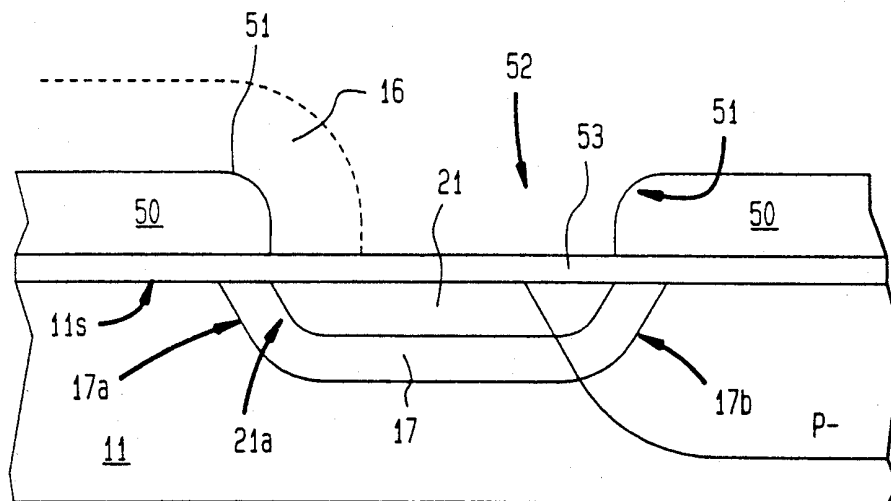


FIG. 5

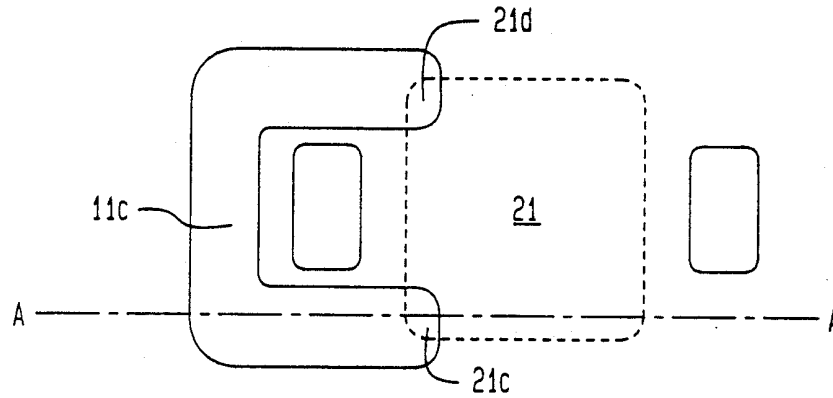


FIG. 6a

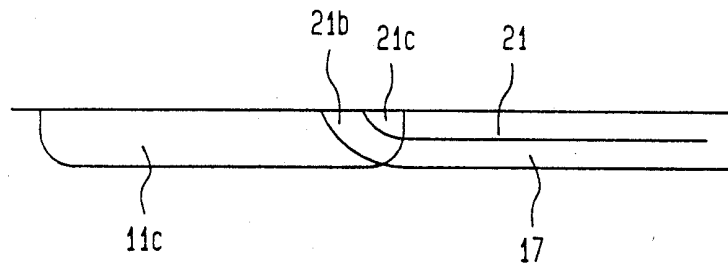


FIG. 6b

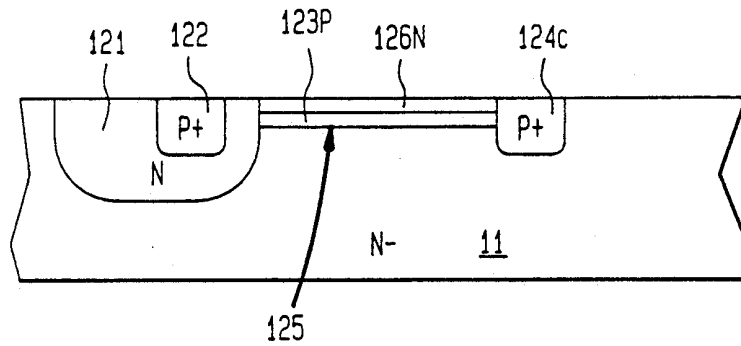


FIG. 7

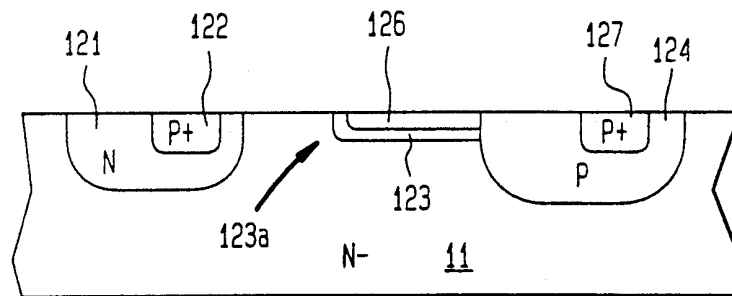


FIG. 8

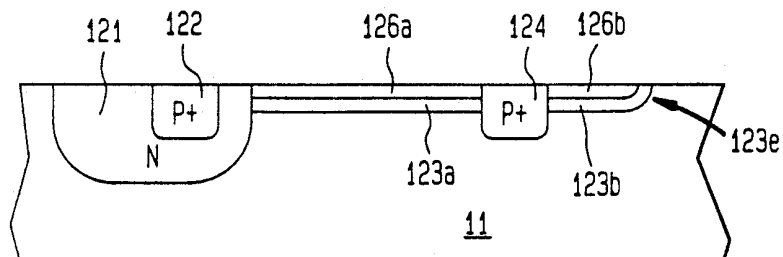


FIG. 9

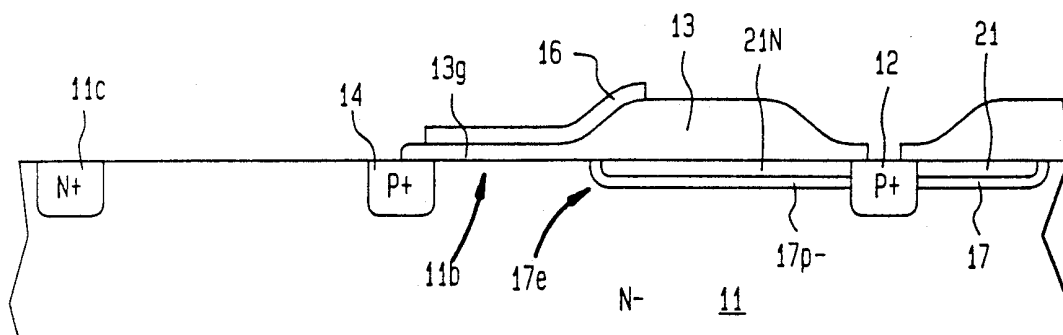


FIG. 10

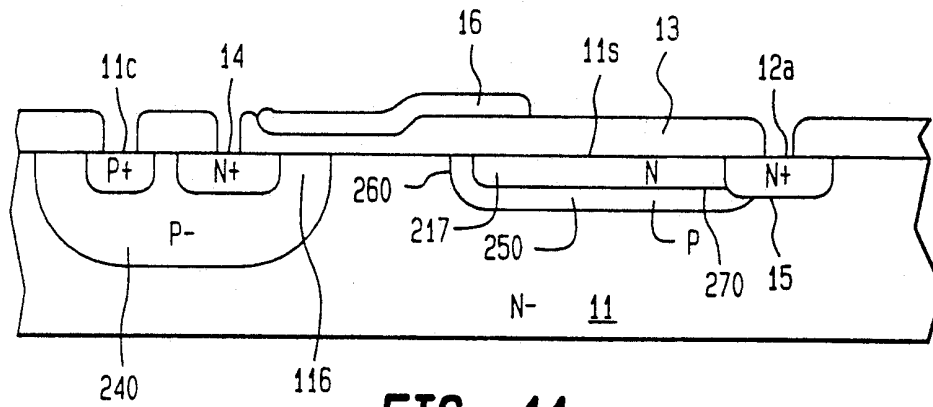


FIG. 11

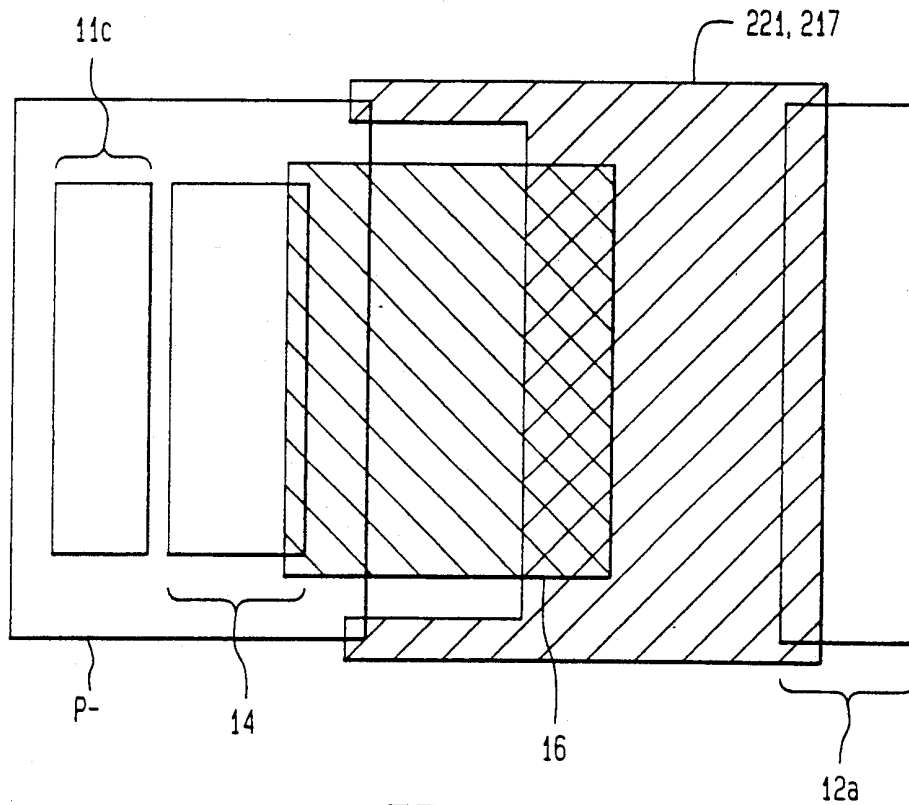


FIG. 12

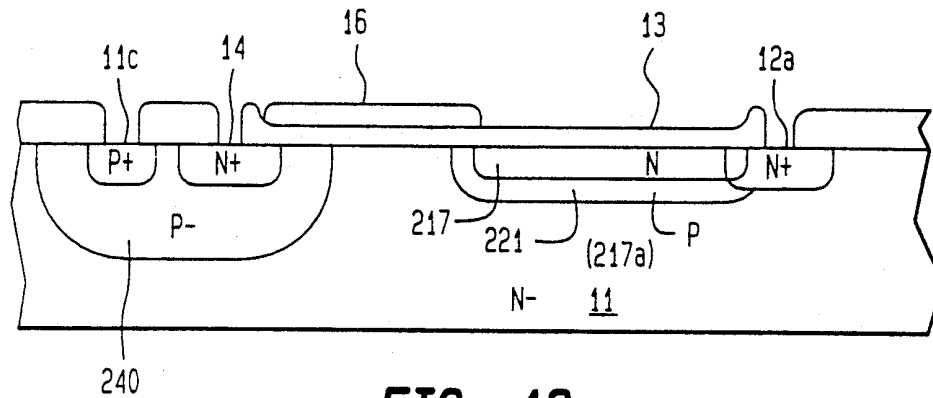


FIG. 13

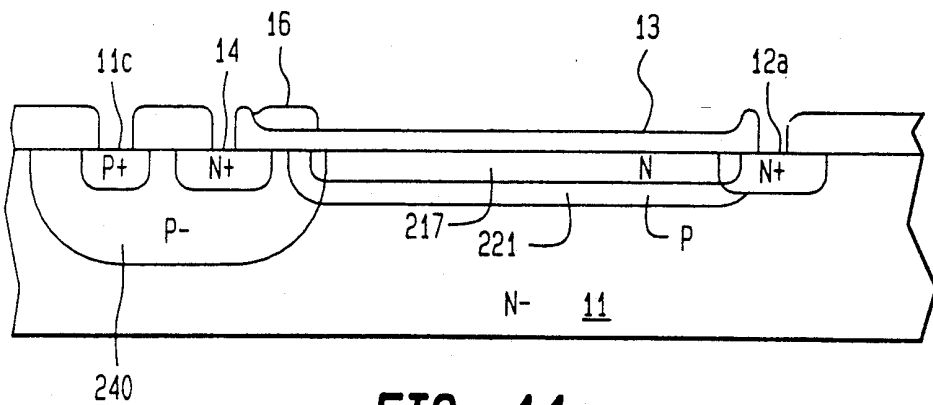


FIG. 14

HIGH VOLTAGE LATERAL SEMICONDUCTOR DEVICE

This is a continuation of application, Ser. No. 242,405, filed Sep. 8, 1988, now abandoned which, in turn, is a continuation-in-part of application, Ser. No. 831,384, filed Jan. 7, 1986, now U.S. Pat. No. 4,823,173, issued Apr. 18, 1989.

FIELD OF THE INVENTION

The present invention relates to lateral semiconductor devices and an improved method of making lateral semiconductor devices. More specifically, the invention relates to high voltage lateral devices with reduced ON resistance and a method of making such devices.

Previous high voltage lateral devices include both MOS devices and bipolar transistors. For example, FIG. 1 illustrates a known structure which can be used as a high voltage lateral MOS device. This device is known as a lateral drift region MOS device and is dependent upon the drain-to-body junction 15 as the basic high voltage junction of the device. The drift region 17 is a P region along the top surface of the N- substrate 11 and is located so as to lie adjacent the P- drain region 12. The drift region 17 is used to connect the high voltage drain 12 to the gate 16 and source 14. The two contacts, drain contact 12_a and body contact 11_c are shown for completeness. In the operation of this circuit, the gate 16 and source 14 never assume large voltages relative to the body 11. The drift region 17 serves as a JFET channel with the portion 11_a of body region 11 underlying the channel acting as a JFET gate. The JFET channel 17 is designed to totally deplete when the drain 12 is reverse biased to a voltage less than the voltage necessary to reach critical field in the channel-to-body depletion layer. This design preserves the effective high breakdown voltage of drain body junction 15. Also the source 14 and gate 16 (over the gate oxide 13) are safely shielded from the high drain body voltage by the pinched off JFET channel 17.

The resistance of the lateral drift region JFET channel 17 is in series with the resistance of the MOS channel 11_b, consequently the total channel resistance of the device is the sum of these two individual resistances. The JFET channel, which must be quite long to sustain high drain body voltages, is often the larger of the two resistance terms. Thus it is desirable to find ways to reduce the resistance of the drift region so that devices of a given size can be made with smaller channel resistance.

FIG. 2 illustrates a known structure which can be used as a high voltage lateral DMOS (LDMOS) device. In this device, an N⁺ drain contact 12A is formed in the N- substrate 211 and an N⁺ source 14 and P⁺ body contact 11_c are formed in a P- body region 240. The drift region 217 is an N- region along the top surface of the N- substrate 211 which connects the drain 12 to the gate 16 and source 14. In this high voltage device, the N- drift region 217 must be lightly doped to obtain high body 240 to drain breakdown.

The ON resistance of the LDMOS is approximately the sum of the channel resistance and the bulk resistance in the N- drift region 217. The lateral distance from the N⁺ drain 12 to the adjacent edge of the MOS channel 11_b underlying the gate on the P- body 240 must be large to allow space for the reverse bias depletion layer which spreads from the body-to-drain junction into the

lightly doped drain. This distance, along with the high N- resistivity contribute to the high drift region resistance, which is often much greater than the channel resistance. Thus, it is desirable to reduce the drift region resistance of the LDMOS device.

FIG. 3 shows a known structure which can be used as a lateral bipolar transistor. Another illustration of such a device is contained in FIG. 7 of U.S. Pat. No. 4,283,236 issued Aug. 11, 1981. Referring to FIG. 3, an N- substrate 11, has an N type emitter shield 121 formed therein and P⁺ emitter 122 and collector 124 formed as shown. Additionally, a P- drift region 123 is provided along the surface of the substrate between the collector 124 and the emitter shield 121. In the operation of this device, the total collector resistance is equal to the sum of the resistance across the drift region 125 plus the resistance of the P⁺ collector between the drift region and the collector contact. In order to provide devices of equal size having a lower collector resistance, it is desirable to find ways to reduce the resistance of the drift region.

In the operation of this device, the drift region extends the collector to the edge of the emitter shield, 121, so that the base width is just that small distance between the adjacent edges of the emitter, 121, and the drift region, therefore, providing improved frequency response.

At high base-collector voltages, the drift region, 123, depletes by JFET action with the N-base, 11, and N shield, 121, which is part of the base, acting as gate before critical field is reached just as for the MOS of FIG. 1. This preserves the high breakdown of the structure.

SUMMARY OF THE INVENTION

The present invention provides a structure having a reduced channel resistance and a process capable of efficiently obtaining the structure of the invention. The reduction in channel resistance is accomplished by providing a top gate which is located between the lateral drift region of the prior art and the surface of the channel region and which may be in contact with the high voltage device region. This top gate allows the total channel doping to be increased because the top gate to channel depletion layer holds some additional channel charge when reverse biased in addition to that held by the bottom gate to channel depletion layer of the prior art structure. The ionized channel impurity atoms associated with this additional channel charge causes the reduction in channel resistance.

With respect to providing an improved LDMOS structure having a lower drift region resistance, a second drift region which is separated from the original drift region by a region of opposing conductivity is formed. The second drift region provides a conductive path which is in parallel with the original drift region thereby achieving the desired reduction in resistance. Because of the formation of the second drift region, the first enclosed drift region can now have a much higher doping than the second drift region which it replaces, while achieving the same breakdown voltage.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cross section of a known MOS device having typical ON resistance.

FIG. 2 is a cross section of a known LDMOS device having typical ON resistance.

FIG. 3 is a cross section of a known bipolar transistor having typical collector resistance.

FIG. 4 is a cross section of an MOS device including the improved drift region and top gate of the invention.

FIG. 5 illustrates optimized process steps for obtaining the desired shape of the top gate and drift region of the invention.

FIGS. 6a and 6b are, respectively, a top view and a cutaway perspective view of the body contact extending through the top gate and drift region of the invention.

FIG. 7 is a cross section of a bipolar device made in accordance with one aspect of the invention.

FIG. 8 is a cross section of a bipolar device made in accordance with another aspect of the invention.

FIG. 9 is a cross section of a bipolar device made in accordance with a preferred aspect of the invention.

FIG. 10 is a cross section of an MOS device, including the lateral drift region and top gate of the invention, in a preferred embodiment.

FIG. 11 is a cross section of a LDMOS device made in accordance with a preferred embodiment of the invention.

FIG. 12 is a top view of the LDMOS device of FIG. 11.

FIG. 13 is a cross section of a LDMOS device made in accordance with another preferred embodiment of the invention.

FIG. 14 is a cross section of a LDMOS device made in accordance with still another preferred embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

The present invention is described herein with reference to the drawings for both MOS and bipolar applications. FIG. 4 shows an MOS device where P⁺ drain contact 12_a is formed in P⁻ type drain 12, P⁺ source 14 is formed in the N⁻ body 11 and N⁺ body contact 11_c is provided in the N⁺ body 11. The MOS channel region 11_b is in the N⁻ body 11 below the MOS gate 16. The N type top gate 21 is provided along the surface 11_s of the body 11 above the P type drift region 17 which acts as a JFET channel. The lateral edge or peripheral edge of both the top gate 21 and drift region 17 extend to the drain-to-body junction 15 and preferably terminate at the junction 15. It is noted that situations may exist where the doping level in the top gate may be sufficiently high so as to render it desirable to provide a shorter top gate having a lateral extension which stops short of contacting the junction 15. In this case care should be taken to insure that any nondepleted portion of the top gate does not result in a breakdown of the top gate-to-drift region junction 17A. Proper doping of the top gate 21 will generally be a sufficient preventative step. Dashed line 21_p designates the peripheral edge of top gate 21 in an embodiment where the top gate does not extend all the way to the junction 15.

The structure of FIG. 4 provides reduced ON resistance in the JFET channel 17 relative to the prior art lateral drift MOS device as shown in FIG. 1. The reduction in ON resistance is accomplished by providing a structure which can accommodate increased drift region doping without suffering from reduced body-to-drain breakdown. This is possible because of the provision of the top gate 21. The top gate-to-channel depletion layer which holds some channel charge when reverse biased, is in addition to the channel charge held by

the bottom gate to channel depletion layer of the prior art. This additional channel charge, in the form of ionized channel impurity atoms, causes the reduction in channel resistance. It is possible to provide more than twice the doping level previously acceptable due to the additional ability to hold channel charge. Thus, for a drift region 17 having a doping of 1×10^{12} boron atoms per square centimeter in a bottom gate arrangement, the present invention will permit 2×10^{12} boron atoms per square centimeter. Thus, the ON resistance will be only half the ON resistance of the prior arrangement.

In order to optimize performance of the structure of the invention, the top gate 21 must be designed differently than an ordinary JFET gate. Top gate 21 should become totally depleted at a body-to-drain voltage of less than the breakdown voltage of the top gate-to-drain junction 15. Since top gate 21 is connected to body 11 (as shown in FIGS. 6A, 6B to be described below), the voltage at the top gate-to-drain junction 15_a will equal the voltage of the body-to-drain junction 15 voltage and the top gate-to-drain breakdown voltage should be greater than the voltage at which top gate 21 becomes totally depleted. Additionally, the top gate 21 must totally deplete before the body 11 to channel 17 depletion layer reaches the top gate 21 to channel 17 depletion layer to thereby assure that a large top gate 21 to drain 12 voltage is not developed by punch-through action from the body 11. An ordinary JFET gate never totally depletes regardless of operating conditions.

In addition to the above described characteristics of the device of the invention, it is also necessary to insure that the channel of the JFET drift region 17 contacts the inversion layer MOS surface channel. This can be accomplished as shown in FIG. 5 where an implant mask 50 having a tapered edge 51 is provided over the body 11. An implant aperture 52 is provided in mask 50 at the location where the P drift region 17 and N top gate 21 are to be formed. The aperture 52 is shown as exposing the protective oxide 53. Ion implantation is not substantially affected by the oxide 53 due to the oxide thickness of only about 0.1–0.2 micrometers, yet the oxide provides surface passivation for the underlying body 11.

The drift region 17 is ion implanted and, because of the graduated thickness of the implant mask 50 (along the edge 51), the depth of the implanted drift region 17 is graduated or tapered. In the illustration, a fairly good rounding of the drift region 17 occurs at the peripheral edges or extremities 17_a, 17_b of the region 17. The curved extremity 17_a is of interest because at this location the channel of the JFET drift region 17 contacts the surface 11_s of body 11 beyond the end 21_a of top gate 21 and is desirably beneath the gate 16 of the MOS device. The top gate 21 may be ion-implanted using the implant mask 50 but at an energy level which results in a shallower implantation. This tapered profile, particularly if curved, provides improved performance.

In a variation of this method, a diffusion process can be used to bring the JFET channel into contact with the surface of body 11, and hence insure that the JFET channel 17 will contact the inversion layer MOS surface channel (lateral drift region 17 and top gate 21 are diffused after initial introduction by ion implant). The doping levels and diffusion times are chosen such that the extremity 17_a of JFET channel 17 diffuses beyond the end 21_a of the top gate 21 and so that the end 17_a reaches the surface 11_s of body 11. In practice, this approach can be facilitated by choosing a top gate dop-

ant which has a lower diffusion coefficient than that of the drift region dopant.

The formation of the drift region 17 and top gate 21 may be conveniently carried out by forming a mask over the gate oxide which is present in a lateral MOS application. The MOS gate may be utilized as one delineating edge of the implant for the drift region and top gate and a thick oxide portion surrounding a thinner oxide portion may form the remainder of the implant mask. The thinner oxide portion shall be located such that it extends from beneath the MOS gate to the drain and preferably overlaps the drain. The implant mask 50 illustrated in FIG. 5 is shown as having thin oxide portion 53 being surrounded by the implant mask 50. If the MOS gate 16 shown in dashed lines were used as a portion of the mask 50, the edge of the drift region and top gate would be self-aligned with the MOS gate as shown in dashed lines. Then, when diffused, the drift region will extend laterally to a point beneath the MOS gate, while the top gate 21 may be formed such that there is little or no lateral overlap with the MOS gate. The extent of lateral diffusion of the top gate is dependent upon the dopant material and processing temperatures following top gate implant. It is noted that there is a separation between the drift region and the source. This separation zone is the location where the MOS channel is located.

The top gate 21 will perform as previously described if it is tied to the body 11. Thus, the top gate 21 and the body which operates as the bottom gate of the JFET channel will be at equal potential. According to the invention, this may be accomplished in a particularly effective manner if the drift region 17 is widened to overlap with the body contact region 11_c. This is shown in FIG. 6a which shows the overlapping of the top gate 21 and the body contact 11_c at the overlap regions 21_c, 21_d. In order for this arrangement to be effective, it is necessary that the body contact 11_c have a higher dopant concentration than the JFET channel (or drift region) 17, as shown in FIG. 6b to insure that the body contact 11_c forms a continuous region horizontally and/or vertically through the JFET channel and to the body region 11 from the top gate, 21.

FIG. 6b shows a cross section of the structure of FIG. 6a taken along dashed line A—A. The body 11 is provided with body contact 11_c which is located such that the top gate 21 and drift region 17 can be conveniently extended to overlap the body contact 11_c. The depth of body contact 11_c may be made greater than the depth of region 17 such that a portion of the body contact 11_c extends below region 17 and provides contact with the body 11. This arrangement provides a contact portion 21_c where the top gate 21 is in contact with body contact 11_c. Thus, as long as the body contact doping concentration in region 21_b is sufficiently high to overcome the opposite doping in region 17, then a good connection of uniform conductivity type will be provided between the top gate 21 and the body 11, via contact region 11_c. It is also noted that the body contact 11_c extends laterally beyond the end of both of the top gate 21 and the drift region 17. The lateral extension of the contact 11_c will also provide a structure which results in a good connection of uniform conductivity type from the top gate 21 to the body 11, again, provided that the doping of body contact 11_c converts region 21_b.

Another area where the present invention finds application is in lateral bipolar transistors which employ a lateral drift region. The known structure of FIG. 3 may

be improved by providing an N type top gate 126 as shown in FIG. 7. In this arrangement the N type gate 126 extends from the collector 124 to the emitter shield 121 along the surface of body 11. The operation of this device is enhanced by the same phenomenon as the lateral drift region of the previously described MOS device. As the base 11 becomes positive relative to the collector 124, the top gate-to-drift region depletion layer facilitates pinch-off of the drift region 123. However, as the base 11 becomes more negative, the top gate 126 contributes additional surface exposure to the drift region 123 and further enhances carrier transportation.

FIG. 8 shows an improvement over the arrangement shown in FIG. 7. In FIG. 8 the drift region 123 does not extend all the way over to the emitter shield 121. The curved end 123_a of the drift region 123 contacts the top surface of body 11. It is noted that in this arrangement, the emitter shield 121 may be omitted.

An additional improvement shown in FIG. 8 is the use of a deep diffusion to form the collector 124 resulting in a significantly increased breakdown voltage. The deep diffusion step may be the same step used for forming the emitter, in which case the collector 124 shown in FIG. 7 would be deeper, or a separate collector implant and diffusion step may be employed and the collector contact 127 may then be formed simultaneously with the formation of the emitter 122. This improvement in junction breakdown voltage is equally obtainable, for example, at the body to drain junction in the MOS devices described previously.

A further extension of the invention which may be used to increase base-to-collector breakdown voltage for a PNP device is shown in FIG. 9. In addition to the provision of the N type top gate 126_a over the P- drift region 123_a, the top gate 126_a and drift region 123_a are enlarged to surround the collector 124 and a curved edge 123_b is provided at the periphery of the enlarged portion 123_b of the drift region 123_a. This enlarged portion is designated by reference numerals 123_b for the drift region and 126_b for the top gate. The collector 124 to base 11 breakdown voltage is increased relative to alternative arrangements because of mitigation of the breakdown reduction due to the junction curvature. The top gate 126_a extends to the emitter shield 121 as does the drift region 123_a. The P+ emitter 122 is formed in the N+ type emitter shield 121.

FIG. 10 illustrates an extension of the invention with respect to a P channel MOS device similar to the improvement described with respect to the bipolar device shown in FIG. 9. For the MOS device, the drain 12 is surrounded by the P- drift region 17 and N type top gate 21. Around the entire periphery of the drift region 17 there is a curved portion 17_e which rounds up to the surface of the N- substrate 11 to insure that the JFET channel in the drift region 17 contacts the MOS channel 11_b under the MOS gate 16. The drift region 17 extends outward from the entire perimeter of the drain 12. This arrangement mitigates the breakdown reduction due to junction curvature. The P+ source 14 and N+ body contact 11_c are shown as is the dielectric 13 which serves as the gate oxide 13_g beneath the MOS gate 16.

In both the arrangements shown in FIG. 9 and FIG. 10, the planar diode breakdown improvement created by the drift region acting as a surface layer of the same conductivity type as the collector in FIG. 9 and drain in FIG. 10 and extending out from the perimeter of the collector and drain can be implemented by a single series of process steps. According to the invention, a

common set of process steps produces both a suitable breakdown improvement layer and an improved drift region. The breakdown improvement layer is a two layer component.

A further extension of the invention is illustrated in FIG. 11 which shows an LDMOS device where N⁺ drain contact 12_a is formed in an N⁻ type substrate and an N⁺ source 14 and P⁺ body contact 11_a are formed in a P⁻ type body region 240. The DMOS channel region 11_b is in the P⁻ body 240 below the DMOS gate 16. The N type first drift region 217 is provided along the surface 11_c of the substrate 11 above a P⁻ type separation region 250. A second drift region 217_a exists in the substrate 11 underneath the P⁻ type separation region. The lateral edge of both the first drift region 217 and the separation region 250 extend from the gate 16 to the N⁺ drain contact 12_a.

The structure in FIG. 11 provides reduced ON resistance by way of the second (surface) drift region 217_a relative to the (deeper) prior art lateral first drift region 217_a device, refer to above in FIG. 2. To illustrate this, consider an example in which the N⁻ region 11 has a doping of 1×10^{14} ions cm⁻³. The top gate layer 217 has an integrated doping of about 1×10^{12} ions cm⁻² and is preferably not more than two microns thick while maintaining full breakdown. The thickness of the N and P layers 217, 250 together is preferably less than ten microns and can be less than one micron. The same integrated doping in the N⁻ body 11 requires a thickness of 100 microns. Thus, the N and P layers 217, 250 respectively consume only a small fraction of the N⁻ thickness required to provide doping equal to that portion of the N layer of the prior art device.

The lateral spacing between the drain contact 12_a and the channel 11_b in the device described above would be approximately 30 microns. In such a device, even if a full 100 micron thick N⁻ body 11 were provided, it would have a higher resistance than the N⁻ first drift region 217 provided according to the invention. This is because the average path length of current flowing from the drain contact 12A down through the thick N⁻ body 11 and back up to the surface edge of the channel at the drain-to-body junction would be greater than the direct path through the N⁻ first drift region.

Maximum breakdown is achieved in the invention by providing doping densities of the N and P layers 217, 250 such that they become totally depleted before breakdown is reached at any point along the junctions which they form with adjoining regions and before breakdown is reached at the junction between them. To insure that this occurs, the N region 217 should have an integrated doping not exceeding approximately 1×10^{12} ions cm⁻² and the P region 250 should have a higher integrated doping not exceeding about 1.5 to 2×10^{12} ions cm⁻².

To insure proper depletion of the P and N regions 250, 217, they must have the proper voltages applied. The N layer bias is achieved by connecting the N first drift region 217 to the higher concentration N⁺ drain contact 12_a by overlapping the N first drift region 217 and drain contact 12_a. The P region 250 bias is achieved by overlapping the P region 250 with the P⁻ body 240 at least at one end of the channel, thereby applying the body voltage to the P layer 250. This is illustrated in FIG. 12.

With this structure and choice of doping levels, the desired results are achieved. When a reverse bias voltage is applied to the drain-to-body junction 15, the same

reverse bias appears on both the PN⁻ junction 260 and the PN junction 270. Depletion layers spread up into the N first drift region 217 and down into the N⁻ body 11 from the P layer 250. In a preferred embodiment, the P and N first drift region dopings are chosen such that the N layer 217 becomes totally depleted at a lower voltage than that at which the P layer 250 becomes totally depleted. This insures that no residual undepleted portion of the N layer 217 is present which could reduce breakdown voltage.

As a result of the invention, the improved DMOS device provides a reduced resistance current path in the drain which does not depend on the N⁻ doping. This allows the N⁻ doping to be reduced to achieve a desired breakdown voltage with good manufacturing margin, while maintaining desirable low drift region resistance. In a multi-device process which includes LDMOS devices, the N⁻ region can be adjusted to achieve the desired characteristics of one or more of the other device types, while the N first drift region 217 sets the drift region 217 resistance of the LDMOS.

Another embodiment of the DMOS invention is illustrated in FIG. 13, where the N and P regions 217, 221 are self-aligned to the gate 16 by using the gate 16 as a mask. An advantage of this structure is that N and P regions can be defined by the uncovered thin oxide area which extends from gate edge to overlap the drain contact. This embodiment requires no explicit mask step to delineate the location where the N and P regions are formed.

Still another embodiment, as illustrated in FIG. 14, provides no gap between the P⁻ body 240 and the P region 221 adjacent to the channel edge. The absence of the gap prevents current from flowing in the N⁻ body 11; so the entire drift region current path is in the N first drift region 217. Elimination of the gap also allows the device structure to be made smaller. As with the other structure, the N and P regions may be self-aligned to the gate edge, as illustrated in FIG. 14, or not self-aligned. They may also be covered by thick or thin oxide as a design option.

A preferred feature of the present invention provides that the body or substrate regions 11 shown in the FIGS. 3, 4, 6, 7, 8, 9, 11, 13 and 14 are designed to be dielectrically or self-isolated regions. In contrast with the typical RESERF type of devices in which the bottom isolation junction plays a central role in the action of the device, the present invention contemplates that the isolation junction does not contribute to the depletion of the drift or top gate regions which are taught to be totally depleted. Prior art RESERF devices such as that described in U.S. Pat. No. 4,300,150 to Colak always require the substrate to be part of such depletion whereby the substrate must assume the most negative voltage in the device because of its role as one side of the isolation junction. As a result of this bias on the substrate or body region, the prior art RESERF type devices are susceptible to punch through from the device region through the epitaxial layer to the substrate. As a result of the present invention not having the substrate as part of the depletion mechanism, the invention can more effectively provide high voltage protection while not increasing the resistance of the channel path. Although the figures illustrate a nonisolating structure or self-isolated structure, it is understood that the invention applies equally well to dielectrically or junction isolated substrates.

While the present invention has been described with respect to several preferred manners of implementing the invention, it is to be understood that the claims appended hereto are intended to cover the invention in its broadest sense and are not to be limited to the specific implementations disclosed.

What is claimed is:

1. A semiconductor device comprising:

- a semiconductor body of a first conductivity type having a first surface;
- a first semiconductor region of a second conductivity type formed in a first portion of said first surface of said semiconductor body, and defining a first PN junction with said semiconductor body;
- a second semiconductor region of said first conductivity type formed in a surface portion of said first semiconductor region and defining therewith a second PN junction, said second PN junction being spaced apart from said first PN junction by material of said first semiconductor region therebetween;
- a third semiconductor region of said first conductivity type formed in a second surface portion of said semiconductor body, spaced apart from said first surface portion by a third surface portion thereof;
- a fourth semiconductor region of said second conductivity type formed in a first surface part of said third surface portion of said semiconductor body spaced apart from said first surface portion of said semiconductor body by a second surface part of said third surface portion thereof and defining with said semiconductor body a third PN junction, said fourth semiconductor region being connected to said first semiconductor region and being contiguous with said third semiconductor region;
- a fifth semiconductor region of said first conductivity type, and having an impurity concentration greater than that of said semiconductor body, formed in said fourth semiconductor region and defining therewith a fourth PN junction, said fifth semiconductor region being contiguous with said third semiconductor region;
- an insulator layer formed on said first surface of said semiconductor body; and
- a gate electrode formed on said insulator layer so as to overlie said second surface part of said third surface portion of said semiconductor body and material of said first and fourth semiconductor regions, that portion of said first semiconductor region lying beneath said gate electrode serving as a channel region of said device, said gate electrode having a gate voltage applied to induce a conductive channel through said first semiconductor region therebeneath; and wherein
- when said device is reverse-biased, a first depletion region extends from said fourth PN junction into said fourth semiconductor region and said semiconductor body, and a second depletion region extends from said fifth PN junction into said fifth semiconductor region and said fourth semiconductor region;
- said semiconductor body having a first ON resistance in a first current flow path therethrough between said second and third semiconductor regions, and said fifth semiconductor region providing a second ON resistance in a second current flow path along the surface of said semiconductor body from said second semiconductor region through said channel

and said fourth and fifth semiconductor regions to said third semiconductor region, so that said fifth semiconductor region serves to provide a current flow path in parallel with said first current flow path, thereby effectively reducing the total ON resistance of the overall current flow path between said second and third semiconductor regions.

2. A semiconductor device according to claim 1, wherein a peripheral edge of said gate electrode is aligned with a peripheral edge of said fifth semiconductor region.

3. A semiconductor device according to claim 1, wherein said fourth semiconductor region overlaps said first semiconductor region.

4. A semiconductor device according to claim 1, wherein the impurity concentration said fifth semiconductor region is such that said fifth semiconductor region is completely depleted by said second depletion region at a reverse bias less than that at which said first and second depletion regions come together within and punch through said fourth semiconductor region.

5. A semiconductor device comprising:

- a semiconductor body of a first conductivity type having a first surface;
- a first semiconductor region of a second conductivity type formed in a first portion of said first surface of said semiconductor body, and defining a first PN junction with said semiconductor body;
- a second semiconductor region of said first conductivity type formed in a surface portion of said first semiconductor region and defining therewith a second PN junction, said second PN junction being spaced apart from said first PN junction by material of said first semiconductor region therebetween;
- a third semiconductor region of said first conductivity type formed in a second surface portion of said semiconductor body, spaced apart from said first surface portion by a third surface portion thereof;
- a fourth semiconductor region of said second conductivity type formed in said third surface portion of said semiconductor body and defining with said semiconductor body a third PN junction, said fourth semiconductor region being connected to said first semiconductor region and being contiguous with said first and third semiconductor regions;
- a fifth semiconductor region of said first conductivity type, and having an impurity concentration greater than that of said semiconductor body, formed in said fourth semiconductor region and defining therewith a fourth PN junction, said fifth semiconductor region being contiguous with said first and third semiconductor regions;
- an insulator layer formed on said first surface of said semiconductor body; and
- a gate electrode formed on said insulator layer so as to overlie material of said first and fourth semiconductor regions, that portion of said first semiconductor region lying beneath said gate electrode serving as a channel region of said device, said gate electrode having a gate voltage applied to induce a conductive channel through said first semiconductor region therebeneath; and wherein
- when said device is reverse-biased, a first depletion region extends from said fourth PN junction into said fourth semiconductor region and said semiconductor body, and a second depletion region extends from said fifth PN junction into said fifth semiconductor

5,264,719

11

ductor region and said fourth semiconductor region.

6. A semiconductor device according to claim 5, wherein the impurity concentration said fifth semiconductor region is such that said fifth semiconductor region is completely depleted by said second depletion region at a reverse bias less than that at which said first and second depletion regions come together within and punch through said fourth semiconductor region.

7. A semiconductor device comprising:

- a semiconductor body of a first conductivity type having a first surface;
- a first semiconductor region of a second conductivity type formed in a first portion of said first surface of said semiconductor body, and defining a first PN junction with said semiconductor body;
- a second semiconductor region of said second conductivity type formed in a second surface portion of said semiconductor body, spaced apart from said first surface portion by a third surface portion thereof and defining a second PN junction with said semiconductor body;
- a third semiconductor region of said second conductivity type formed in a first surface part of said third surface portion of said semiconductor body spaced apart from said first surface portion of said semiconductor body by a second surface part of said third surface portion thereof and defining with said semiconductor body a third PN junction, said third semiconductor region being contiguous with said second semiconductor region;
- a fourth semiconductor region of said first conductivity type, and having an impurity concentration greater than that of said semiconductor body, formed in said third semiconductor region and defining therewith a fourth PN junction;
- an insulating layer formed on said first surface of said semiconductor body; and
- a gate electrode formed on said insulator layer so as to overlie said second surface part of said third surface portion of said semiconductor body, that portion of said semiconductor body lying beneath said gate electrode serving as a channel region of said device, said gate electrode being applied with a gate voltage for inducing a conductive channel through said channel region;

said device being reverse-biased, so that a first depletion region extends from said third PN junction into said third semiconductor region and said semiconductor body and a second depletion region extends from said fourth PN junction into said third semiconductor region and said fourth semiconductor region;

said semiconductor body having a first ON resistance in a first current flow path therethrough between said first and second semiconductor regions, and said fourth semiconductor region providing a second ON resistance, less than said first ON resistance, in a second current flow path along the surface of said semiconductor body from said first semiconductor region through said channel and said third and fourth semiconductor regions to said second semiconductor region, so that said fourth semiconductor region serves to provide a reduced resistance current flow path in parallel with said first current flow path, thereby effectively reducing the total ON resistance of the overall current

12

flow path between said first and second semiconductor regions; and

wherein the impurity concentration said fourth semiconductor region is such that said fourth semiconductor is completely depleted by said second depletion region at a reverse bias less than that at which said first and second depletion regions come together within and punch through said third semiconductor region.

8. A high voltage MOS transistor comprising:

- a semiconductor substrate of a first conductivity type having a surface,
- a pair of laterally spaced source and drain pockets of semiconductor material of a second conductivity type within the substrate and adjoining the substrate surface,
- an extended drain region of the second conductivity type extending laterally each way from said drain pocket to surface-adjoining positions,
- a surface adjoining, top layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain pocket and the surface-adjoining positions,
- said top layer of material and said substrate being subject to application of a reverse-bias voltage,
- an insulating layer on the surface of the substrate and covering at least that portion between the source pocket and the nearest surface-adjoining position of the extended drain region, and
- a gate electrode on the insulating layer and electrically isolated from the substrate region thereunder which forms a channel laterally between the source pocket and the nearest surface-adjoining position of the extended drain region, said gate electrode controlling by field-effect the flow of current thereunder through the channel.

9. A high voltage MOS transistor according to claim 8, wherein said extended drain region has an impurity concentration greater than $1 \times 10^{12} \text{ cm}^{-2}$.

10. A high voltage MOS transistor according to claim 8, further including an ohmic contact region of said first conductivity type formed in a surface adjoining portion of said semiconductor substrate, said ohmic contact region overlapping said top layer of material.

11. A high voltage MOS transistor comprising:

- semiconductor material of a first conductivity type having a surface,
- a pair of laterally spaced source and drain pockets of semiconductor material of a second conductivity type within the substrate and adjoining the surface of said semiconductor material,
- an extended drain region of the second conductivity type extending laterally from said drain pocket to a surface-adjoining position,
- a surface adjoining top layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain pocket and said surface-adjoining position,
- said top layer of material and said semiconductor material being subject to application of a reverse-bias voltage,
- an insulating layer on the surface of said semiconductor material and covering at least that portion between the source pocket and the nearest surface-adjoining position of the extended drain region, and
- a gate electrode on the insulating layer and electrically isolated from a semiconductor material re-

gion thereunder containing a channel that extends laterally between the source pocket and the nearest surface-adjointing position of the extended drain region, said gate electrode controlling by field-effect the flow of current thereunder through the channel.

12. A high voltage MOS transistor according to claim 11, wherein said extended drain region extends in a plurality of different directions from said drain pocket to respective plural surface adjoining positions.

13. A high voltage MOS transistor according to claim 11, wherein said extended drain region surrounds said drain pocket and extends to a surrounding surface adjoining position.

14. A high voltage MOS transistor according to claim 11, wherein said drain pocket comprises a first relatively deep pocket of a first impurity concentration and a second relatively shallow pocket formed in a surface portion of said first relatively deep pocket and having a second impurity concentration greater than said first impurity concentration and providing a drain contact region.

15. A high voltage MOS transistor according to claim 11, wherein said extended drain region has an impurity concentration greater than $1 \times 10^{12} \text{ cm}^{-2}$.

16. A high voltage MOS transistor according to claim 11, further including an ohmic contact region of said first conductivity type formed in a surface adjoining portion of said semiconductor material, said ohmic contact region overlapping said top layer of material.

17. A high voltage field effect transistor device comprising:
semiconductor material of a first conductivity type having a surface;
a source region of a second conductivity type formed in a first surface portion of said semiconductor material;
a drain region of said second conductivity type formed in a second surface portion of said semiconductor material spaced apart from said first surface portion by a third surface portion therebetween;
an extended drain region of said second conductivity type extending from said drain region beneath a first portion of said third surface portion of said semiconductor material, to adjoin a second portion of said third surface portion of said semiconductor material, spaced apart from said said second surface portion of said semiconductor material, by said first portion of said third surface portion of said semiconductor material;
a surface region of said first conductivity type formed in said first portion of said third surface portion of said semiconductor material;
an insulating layer disposed on said surface of said semiconductor material, so as to overlie a third portion of said third surface portion of said semiconductor material between the second portion of said third surface portion of said semiconductor material and said first surface portion of said semiconductor material; and
a gate electrode disposed on that portion of said insulating layer overlying said third portion of said third surface portion of said semiconductor material, and wherein said surface region and said semiconductor material are subject to the application of a reverse bias voltage.

18. A high voltage field effect transistor device according to claim 17, wherein said extended drain region

extends laterally in a plurality of different directions from said drain region to adjoin said second portion of said third surface portion of said semiconductor material and to adjoin a fifth surface portion of said semiconductor material.

19. A high voltage field effect transistor device according to claim 17, wherein said extended drain region surrounds said drain region and extends to a surrounding surface-adjointing portion of said semiconductor material.

20. A high voltage field effect transistor device according to claim 17, wherein said drain region comprises a first relatively deep region of a first impurity concentration and a second relatively shallow region formed in a surface portion of said first relatively deep region and having a second impurity concentration greater than said first impurity concentration and providing a drain contact region.

21. A high voltage field effect transistor device according to claim 17, wherein said extended drain region has an impurity concentration greater than $1 \times 10^{12} \text{ cm}^{-2}$.

22. A high voltage field effect transistor device according to claim 17, further including an ohmic contact region of said first conductivity type formed in a surface adjoining portion of said semiconductor material, said ohmic contact region overlapping said surface region.

23. An integrated MOS/JFET transistor device comprising an insulated gate field effect transistor and a double-sided junction field effect transistor integrated together in semiconductor substrate which contains a source region, and a drain region, and a dual channel path formed in said semiconductor material between said source and drain regions, said dual channel path comprising an insulated gate-controlled channel region having a first conductivity type in the presence of a channel-inducing gate voltage, said insulated gate-controlled channel region being contiguous with a double-sided junction channel region of said first conductivity type, and wherein said source region adjoins said insulated gate-controlled channel region and said drain region adjoins said double-sided channel region.

24. An integrated MOS/JFET transistor device according to claim 23, wherein said insulated gate-controlled channel region comprises a surface portion of said semiconductor material adjoining said source region, and wherein said double-sided junction channel region comprises an extended drain region extending laterally from said drain region beneath a top gate region to said surface portion of said semiconductor material, an underlying portion of said semiconductor material extending beneath and adjoining said extended drain region and forming a bottom gate, said top gate region and said bottom gate forming respective PN junctions with said double-sided junction channel region.

25. An integrated MOS/JFET transistor device according to claim 23, wherein said extended drain region and said double-sided junction channel region surround said drain region and extend to a surrounding surface-adjointing position.

26. An integrated MOS/JFET transistor device according to claim 23, wherein said extended drain region and said double, wherein said drain region comprises a first relatively deep region of a first impurity concentration and a second relatively shallow region formed in a surface portion of said first relatively deep region and having a second impurity concentration greater than

5,264,719

15

said first impurity concentration and providing a drain contact region.

27. An integrated MOS/JFET transistor device according to claim 23, wherein said extended drain region and said double, further including an ohmic contact region of said first conductivity type formed in a surface adjoining portion of said semiconductor material, said ohmic contact region overlapping said top gate.

28. An integrated MOS/JFET transistor device according to claim 23, wherein said extended drain region has an impurity concentration greater than $1 \times 10^{12} \text{ cm}^{-2}$.

29. A high voltage MOS transistor comprising:
semiconductor material of a first conductivity type having a surface;

source and drain regions of a second conductivity type adjoining spaced apart portions of the surface of said semiconductor material;

an extended drain region of said second conductivity type extending laterally from said drain region through said semiconductor material to a surface-adjoining portion of the surface of said semiconductor material;

a top gate semiconductor layer of said first conductivity type adjoining said drain region and adjoining said extended drain region along the surface of said semiconductor material to said surface-adjoining portion of the surface of said semiconductor material, said top gate semiconductor layer and said semiconductor material being subject to the application of a reverse-bias voltage;

an insulating layer on the surface of the semiconductor material and covering at least that portion of the surface of said semiconductor material between said source region and said surface-adjoining portion of said extended drain region; and

a gate electrode disposed on said insulating layer and being electrically isolated from that portion of the surface of said semiconductor material thereunder which forms a channel laterally between said source region and said surface-adjoining portion of said extended drain region, said gate electrode controlling, by field-effect, the flow of current thereunder through said channel.

30. A high voltage MOS transistor according to claim 29, wherein said extended drain region extends laterally each way from said drain region to surface-adjoining portions of the surface of said semiconductor material, and wherein said top gate semiconductor layer extends laterally in a plurality of different directions from said drain region and adjoins said extended drain region along the surface of said semiconductor material to said surface-adjoining portions of the surface of said semiconductor material.

31. A high voltage MOS transistor according to claim 29, wherein said extended drain region surrounds said drain region and extends to a surrounding surface adjoining position.

32. A high voltage MOS transistor according to claim 29, wherein said drain region comprises a first relatively deep region of a first impurity concentration and a second relatively shallow region formed in a surface portion of said first relatively deep region and having a second impurity concentration greater than said first impurity concentration and providing a drain contact region.

33. A high voltage MOS transistor according to claim 29, wherein said extended drain region has an impurity concentration greater than $1 \times 10^{12} \text{ cm}^{-2}$.

34. A high voltage MOS transistor according to claim 29, further including an ohmic contact region of said

16

first conductivity type formed in a surface adjoining portion of said semiconductor material, said ohmic contact region overlapping said top gate layer.

35. A high voltage diode comprising:

semiconductor material of a first conductivity type having a surface,

a first, surface-adjoining region of a second conductivity type;

a second surface-adjoining region of said first conductivity type spaced apart from said first, surface-adjoining region;

a third region of said second conductivity type extending laterally from said first, surface-adjoining region; and

a fourth, surface-adjoining region of said first conductivity type overlying an intermediate portion of said third, laterally extending and surface-adjoining region.

36. A high voltage diode according to claim 35, wherein said third region surrounds said first, surface-adjoining region and extends to a surrounding surface adjoining position.

37. A high voltage diode according to claim 35, wherein said first region comprises a first relatively deep region of a first impurity concentration and a second relatively shallow region formed in a surface portion of said first relatively deep region and having a second impurity concentration greater than said first impurity concentration.

38. A high voltage diode according to claim 35, wherein said third region has an impurity concentration greater than $1 \times 10^{12} \text{ cm}^{-2}$.

39. A lateral bipolar transistor having a high voltage base-collector diode comprising:

semiconductor material of a first conductivity type having a surface and forming a base of said bipolar transistor,

a first, surface-adjoining collector region of a second conductivity type forming a base-collector junction with said semiconductor material;

a second surface-adjoining base region of said first conductivity type spaced apart from said first, surface-adjoining collector region;

a third, extended collector region of said second conductivity type extending laterally from said first, surface-adjoining collector region, so that said base-collector junction extends laterally from said first, surface adjoining collector region;

a fourth, surface-adjoining region of said first conductivity type overlying an intermediate portion of said third, laterally extending and surface-adjoining extended collector region; and

a fifth, surface-adjoining emitter region of said second conductivity type formed in said second surface-adjoining base region and defining therewith an emitter-base junction.

40. A lateral bipolar transistor according to claim 39, wherein said third region surrounds said first, surface-adjoining region and extends to a surrounding surface adjoining position.

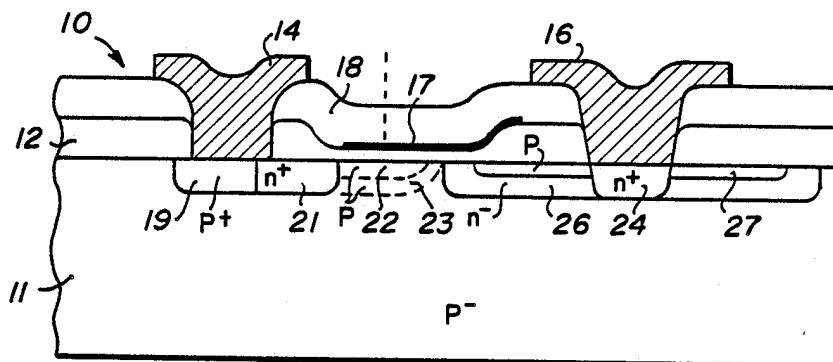
41. A lateral bipolar transistor according to claim 39, wherein said first region comprises a first relatively deep region of a first impurity concentration and a second relatively shallow region formed in a surface portion of said first relatively deep region and having a second impurity concentration greater than said first impurity concentration.

42. A lateral bipolar transistor according to claim 39, wherein said third, extended collector region has an impurity concentration greater than $1 \times 10^{12} \text{ cm}^{-2}$.

* * * * *

United States Patent [19]**Eklund**[11] **Patent Number:** **4,811,075**[45] **Date of Patent:** **Mar. 7, 1989**[54] **HIGH VOLTAGE MOS TRANSISTORS**[75] **Inventor:** **Klas H. Eklund**, Los Gatos, Calif.[73] **Assignee:** **Power Integrations, Inc.**, Mountain View, Calif.[21] **Appl. No.:** **41,994**[22] **Filed:** **Apr. 24, 1987**[51] **Int. Cl.⁴** **H01L 27/02; H01L 29/78; H01L 29/80**[52] **U.S. Cl.** **357/46; 357/22; 357/23.4; 357/23.8**[58] **Field of Search** **357/23.8, 23.4, 46, 357/22**[56] **References Cited****U.S. PATENT DOCUMENTS**4,626,879 12/1986 Colak 357/23.8
4,628,341 12/1986 Thomas 357/23.8**OTHER PUBLICATIONS**Sze, *Physics of Semiconductor Devices* Wiley & Sons
N.Y. c. 1981 pp. 431-438, 486-491.*Primary Examiner*—Andrew J. James*Assistant Examiner*—Jerome Jackson*Attorney, Agent, or Firm*—Thomas E. Schatzel[57] **ABSTRACT**

An insulated-gate, field-effect transistor and a double-sided, junction-gate field-effect transistor are connected in series on the same chip to form a high-voltage MOS transistor. An extended drain region is formed on top of a substrate of opposite conductivity-type material. A top layer of material having a conductivity-type opposite that of the extended drain and similar to that of the substrate is provided by ion-implantation through the same mask window as the extended drain region. This top layer covers only an intermediate portion of the extended drain which has ends contacting a silicon dioxide layer thereabove. The top layer is either connected to the substrate or left floating. Current flow through the extended drain region can be controlled by the substrate and the top layer, which act as gates providing field-effects for pinching off the extended drain region therebetween. A complementary pair of such high-voltage MOS transistors having opposite conductivity-type are provided on the same chip.

7 Claims, 2 Drawing Sheets

U.S. Patent

Mar. 7, 1989

Sheet 1 of 2

4,811,075

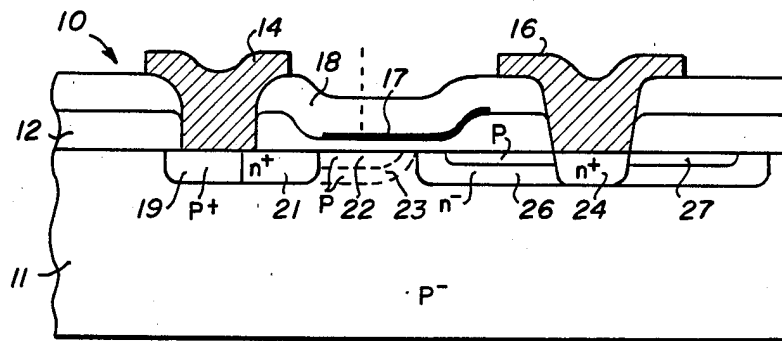


Fig. 1

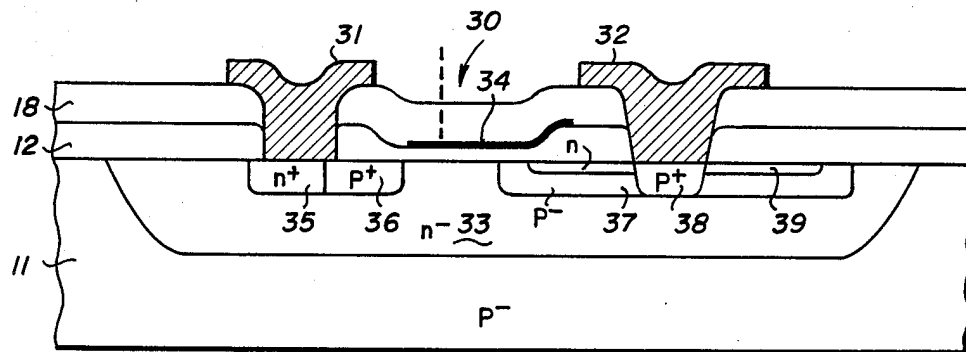


Fig. 2

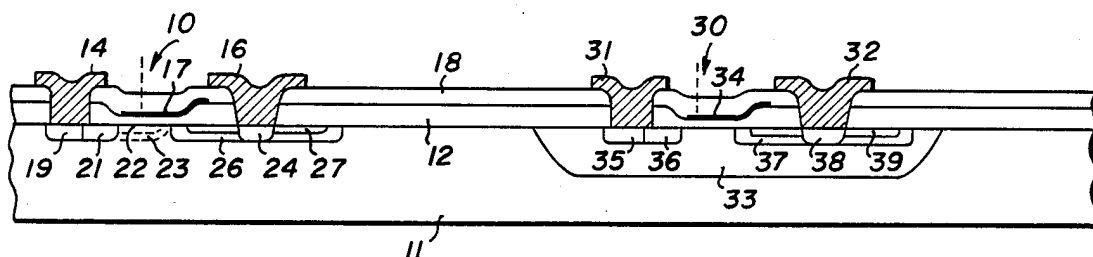


Fig. 3

U.S. Patent

Mar. 7, 1989

Sheet 2 of 2

4,811,075

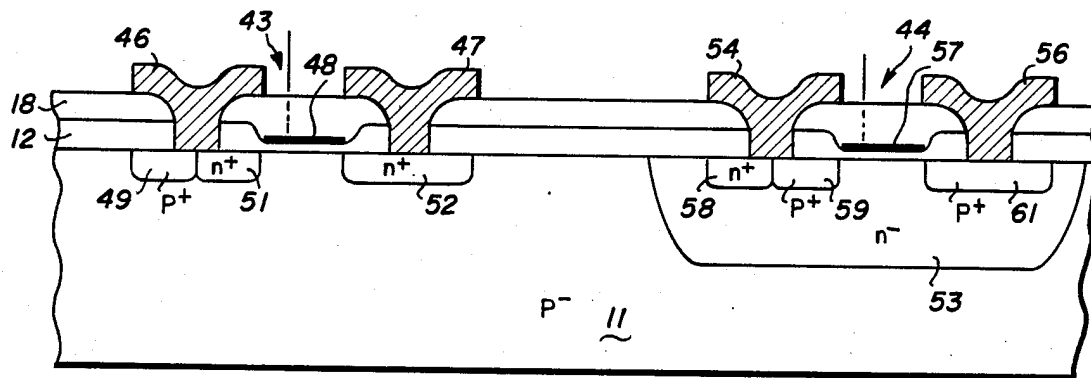


Fig. 4

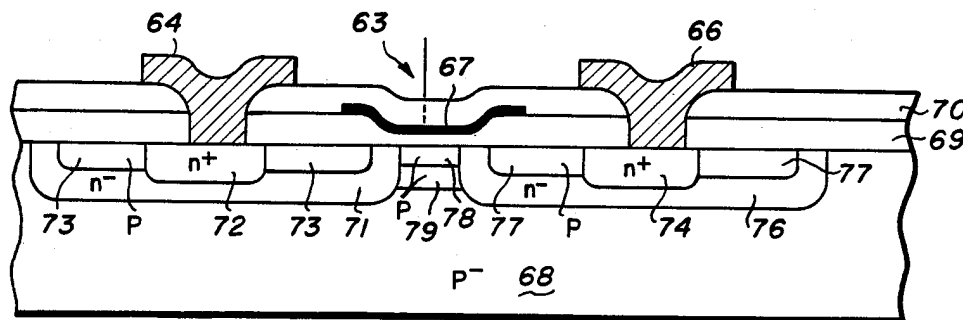


Fig. 5

4,811,075

1

HIGH VOLTAGE MOS TRANSISTORS

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates generally to high voltage metal-oxide semiconductor (MOS) transistors of the field-effect type. More specifically, the transistors can be made as either discrete or integrated devices of either n-channel or p-channel conductivity. The integrated devices can easily be combined with low voltage control logic on the same chip. Further devices of opposite conductivity can be combined in a complementary manner on the same chip.

2. Description of the Prior Art

Self isolation technology is used for making high voltage MOS devices, particularly integrated high voltage devices in combination with low voltage control logic on the same chip. The voltage is sustained by an offset gate, as a lightly doped extended drain region is used. Such devices can be considered as an IGFET or MOSFET in series with a single sided JFET. Two of such high voltage devices having opposite conductivity types can be used as a complementary pair on the same chip, with the device having an extended p-type drain being imbedded in an n-well in a p-substrate.

The voltage capability of such high voltage devices is determined by the doping of the substrate, the length of the extended drain region and the net number of charges therein. For optimum performance, the net number of charges should be around $1 \times 10^{12}/\text{cm}^2$. Such devices have been used for making display drivers in the one hundred to two hundred volt range, but the current capabilities of the devices are poor. The main advantage is that low voltage control logic easily can be combined on the same chip. For these devices, a general figure of merit can be determined by the product of $R_{on} \times A$ (where R_{on} is the on-resistance in the linear region and A is the area taken up by the device). For an n-channel device in the voltage range of two hundred fifty to three hundred volts, $R_{on} \times A$ is typically $10\text{--}15 \Omega \text{ mm}^2$. A discrete vertical D-MOS device in the same voltage range has a figure of merit of $3 \Omega \text{ mm}^2$, but is much more difficult to combine with low voltage control logic on the same chip. Thus, the application of these high voltage devices is restricted to current level below 100 mA, such as display drivers. Even such drivers are more costly due to poor area efficiency of the high voltage devices.

SUMMARY OF THE PRESENT INVENTION

An object of the present invention is to provide a more efficient high voltage MOS transistor.

Another object of the invention is to provide a high voltage MOS transistor that is compatible with five volt logic.

A further object of the invention is to provide a three hundred volt n-channel device with a figure of merit, $R_{on} \times A$, of about $2.0 \Omega \text{ mm}^2$,

Briefly, the present invention includes an insulated gate, field-effect transistor (IGFET or MOSFET) and a double-sided junction gate field-effect transistor (JFET) connected in series on the same chip to form a high voltage MOS transistor. In a preferred embodiment of the invention, a complementary pair of such high voltage MOS transistors having opposite conductivity type are provided on the same chip.

2

Advantages of the invention include more efficient high voltage MOS transistors, compatibility with five volt logic, and for an n-channel device, voltage capability of three hundred volts with a figure of merit, $R_{on} \times A$, of about $2.0 \Omega \text{ mm}^2$.

These and other objects and advantages of the present invention will no doubt become obvious to those of ordinary skill in the art after having read the following detailed description of the preferred embodiments which are illustrated in the various drawing figures.

IN THE DRAWINGS

FIG. 1 is a diagrammatic view of a high voltage MOS transistor of the n-channel type embodying the present invention.

FIG. 2 is a diagrammatic view of a high voltage MOS transistor of the p-channel type embodying the present invention.

FIG. 3 is a diagrammatic view of the transistors shown in FIGS. 1 and 2 forming a complementary pair on the same chip.

FIG. 4 is a diagrammatic view of low voltage, C-MOS implemented devices that can be combined on the same chip with the complementary pair of high voltage MOS transistors shown in FIG. 3.

FIG. 5 is a diagrammatic view of a symmetric high-voltage n-channel device wherein the source region and the drain region are similar.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Looking now at FIG. 1, an n-channel type, high voltage MOS transistor, indicated generally by reference numeral 10, is formed on a p-substrate 11 covered by a silicon dioxide layer 12. A metal source contact 14 and a metal drain contact 16 extend through the silicon dioxide layer to the substrate. A polysilicon gate 17 is positioned between the source contact and the drain contact at a location where the silicon dioxide layer is very thin so that the gate is slightly offset and insulated from the substrate. The polysilicon gate is the gate electrode, and an insulation layer 18 covers the gate and the silicon dioxide layer.

Beneath the source contact 14, a pocket 19 of p+ material and a pocket 21 of n+ material are diffused into the p-substrate 11. The pocket 21 extends from beneath the source contact to the gate 17. Beneath the gate is a threshold voltage implant 22 of p-type material for adjusting the threshold voltage and a punch through implant 23 of p-type material for avoiding punch through voltage breakdown. Beneath the drain contact 16, a pocket 24 of n+ material is diffused into the substrate. An extended drain region 26 of n-material is formed by diffusion or ion implantation on top of the p-substrate, and extends from beneath gate 17 to the pocket 24 and a similar distance to the opposite side of the pocket. A top layer 27 of p-material is provided by ion-implantation through the same mask window as the extended drain region to cover an intermediate portion thereof, while the end portions of the drain region are uncovered to contact the silicon dioxide layer 12. The top layer is either connected to the substrate or left floating.

The gate 17 controls by field-effect the current flow thereunder laterally through the p-type material to the n-type material in the extended drain region 26. Further flow through the extended drain region can be controlled by the substrate 11 and the top layer 27, which

4,811,075

3

act as gates providing field-effects for pinching off the extended drain region therebetween. Thus, the transistor 10 can be considered as an insulated gate, field-effect transistor (IGFET or MOSFET) connected in series with a double-sided, junction-gate field-effect transistor (JFET). While the insulated gate, field-effect transistor shown is a conventional MOS type, it should be understood that it could also be a lateral D-MOS or a depletion MOS type.

By adding the top layer 27 over the extended drain region 26 and connecting this top layer to the substrate 11, the net number of charges in the extended drain region can be increased from $1 \times 10^{12}/\text{cm}^2$ to around $2 \times 10^{12}/\text{cm}^2$, or approximately double. This drastically reduces the on-resistance of the transistor 10. The pinch off voltage of the extended drain region can be reduced from typically around forty volts to below ten volts. Thus, a conventional short channel, thin gate oxide MOS transistors can be used as the series transistor instead of a D-MOS device. This results in the following benefits. First, the threshold voltage of a conventional MOS transistor is typically much lower than for a D-MOS device (0.7 volts compared to two four volts for the D-MOS device) and thus, is directly compatible with five volt logic. The D-MOS device usually requires an additional power supply of ten to fifteen volts for driving the gate. Second, the conventional MOS transistor has less on resistance and thus, further reduces the total on resistance.

As the p-type top layer 27 can be made very shallow with a depth of one micron or less, the doping density in that layer will be in the range of 5×10^{16} – $1 \times 10^{17}/\text{cm}^3$. At doping levels above $10^{16}/\text{cm}^3$, the mobility starts to degrade and a decrease in mobility will increase the critical electrical field for breakdown, thus giving a higher breakdown voltage for fixed geometry. The number of charges in the top layer is around $1 \times 10^{12}/\text{cm}^2$ and to first order approximation independent of depth.

The combined benefits of the above features result in a voltage capability of three hundred volts with a figure of merit, $R_{on} \times A$, of about $2.0 \Omega \text{ mm}^2$ for the transistor 10. Currently used integrated MOS transistors have a figure of merit of about 10 – $15 \Omega \text{ mm}^2$, while the best discrete vertical D-MOS devices on the market in a similar voltage range have a figure of merit of 3 – $4 \Omega \text{ mm}^2$.

With reference to FIG. 2, a p-channel type, high voltage MOS transistor is indicated generally by reference numeral 30. Since the layers of substrate, silicon dioxide, and insulation for this transistor are similar to those previously described for transistor 10, they will be given like reference numerals. A p-substrate 11 is covered by a silicon dioxide layer 12 and an insulation layer 18. A metal source contact 31 and a metal drain contact 32 extend through the insulation layer and the silicon dioxide layer to an n-well 33 that is embedded in the substrate. A polysilicon gate 34, which is an electrode, is positioned between the source contact and the drain contact at a location where the silicon dioxide layer is very thin so that the gate is slightly offset and insulated from the n-well. The gate and the silicon dioxide layer are covered by the insulation layer 18.

A pocket 35 of n+ type material and a pocket 36 of p+ type material are provided in the n-well 33 beneath the metal source contact 31. The pocket 36 extends to the gate 34. An extended drain region 37 of p-type material is formed in the n-well and extends from be-

4

neath the gate to a pocket 38 located beneath the drain contact 32, and the extended drain region continues a similar distance on the opposite side of the drain contact. A top layer 39 of n-material is provided by ion-implantation through the same window of the mask as the extended drain region to cover an intermediate portion thereof. The end portions of the extended drain region are uncovered so as to contact the silicon dioxide layer 12. The top layer is either connected to the n-well or left floating.

The gate 34 controls by field-effect the current flow thereunder laterally through the n-type material to the p-type material in the extended drain region 37. Further flow through the extended drain region can be controlled by the n-well 33 and the top layer 39, which act as gates providing field-effects for pinching off the extended drain region therebetween. Thus, the transistor 30 can be considered as an insulated-gate field-effect transistor (IGFET or MOSFET) connected in series with a double-sided, junction-gate field-effect transistor (JFET). The n-well under the extended drain region has to be depleted before breakdown occurs between the p+ drain contact pocket 38 and the n-well.

Looking now at FIG. 3, an n-channel transistor 10, similar to that shown in FIG. 1, and a p-channel transistor 30, similar to that shown in FIG. 2, are shown as a complementary pair on the same substrate 11 and isolated from each other. Since the details of each transistor has been previously described with reference to FIGS. 1 and 2, no further description is considered necessary.

As shown in FIG. 4, low voltage, C-MOS implemented devices 43 and 44 can be combined on the same p-substrate 11 as the high voltage devices 10 and 30, shown in FIG. 3. These low voltage devices enable low voltage logic and analog function to control the high voltage devices. The device 43 is an n-channel type having a source contact 46, a drain contact 47 and a polysilicon gate 48. A p+ pocket 49 and an n+ pocket 51 are provided in the p- substrate beneath the source contact. The n+ pocket extends to beneath the gate. An n+ pocket 52 is provided beneath the drain contact. The gate 48 is insulated from the substrate by the silicon dioxide layer 12, but the gate controls the current flow through the substrate between pockets 51 and 52. The gate is covered by the insulation layer 18. An n-well 53 is provided in the substrate to accommodate the low voltage, p-channel device 44. This device includes a source contact 54, a drain contact 56 and a polysilicon gate 57. An n+ pocket 58 and a p+ pocket 59 are provided in the n-well beneath the source contact and a p+ pocket 61 is provided in the n-well beneath the drain contact. The gate 57 is insulated from the n-well and extends thereabove between pockets 59 and 61.

It should be noted that the term "substrate" refers to the physical material on which a microcircuit is fabricated. If a transistor is fabricated on a well of n or p type material within a primary substrate of opposite type material, the well material can be considered a secondary substrate. Similarly, if a transistor is fabricated on an epitaxial layer or spi-island that merely supports and insulates the transistor, the epitaxial layer or epi-island can be considered a secondary substrate. An epi-island is a portion of an epitaxial layer of one conductivity type that is isolated from the remaining portion of the epitaxial layer by diffusion pockets of an opposite conductivity type. When complimentary transistors are formed on the same chip, the well in which one compli-

4,811,075

5

mentary transistor is embedded is formed by the same diffusion as the extended drain region for the other transistor.

FIG. 5 shows a symmetrical n-channel device 63 having a source contact 64 and a drain contact 66. A polysilicon gate 67 is insulated from a substrate 68 by a silicon dioxide layer 69 and the gate is covered by an insulation layer 20. An n-type extended source region 71 is provided beneath the source contact and an n+ type pocket 72. A top layer 73 of p-type material is positioned over an intermediate portion of the extended source region, while the end portions of the extended source region contact the silicon dioxide layer thereabove. Beneath the drain contact is an n+ type pocket 74 and an n-type extended drain region 76. A top layer 73 of p-type material is positioned over an intermediate portion of the extended drain region and end portions of the extended drain region contact the silicon dioxide layer. An implant 78 of the p-type material is provided under the gate 67 between the extended source region and the extended drain region for sustaining the threshold voltage. A similar implant 79 for sustaining the punch-through voltage is provided beneath the implant 78. Since the symmetrical channel device has both an extended source and an extended drain, the source can sustain the same high potential as the drain. A symmetric p-channel device could be made in a similar way using opposite conductivity type materials.

From the foregoing description, it will be seen that an efficient, high voltage MOS transistor has been provided. This transistor is compatible with five volt logic which easily can be integrated on the same chip. The transistor has a voltage capability of three hundred volts for an n-channel device, and has a figure of merit, $R_{on} \times A$, of about $2.0 \Omega \text{mm}^2$. The transistor is formed by an insulated-gate field-effect transistor and a double-sided junction-gate field-effect transistor connected in series on the same chip. These transistors can be made as either discrete devices or integrated devices of either n-channel or p-channel conductivity. The integrated devices can be easily combined with low voltage control logic on the same chip. Further devices of opposite conductivity can be combined in a complementary manner on the same chip.

Although the present invention has been described in terms of the presently preferred embodiment, it is to be understood that such disclosure is not to be interpreted as limiting. Various alterations and modifications will no doubt become apparent to those of ordinary skill in the art after having read the above disclosure. Accordingly, it is intended that the appended claims be interpreted as covering all alterations and modifications as fall within the true spirit and scope of the invention.

I claim:

1. A high voltage MOS transistor comprising:
 - a semiconductor substrate of a first conductivity type having a surface
 - a pair of laterally spaced pockets of semiconductor material of a second conductivity type within the substrate and adjoining the substrate surface,
 - a source contact connected to one pocket,
 - a drain contact connected to the other pocket,
 - an extended drain region of the second conductivity type extending laterally each way from the drain contact pocket to surface-adjoining positions,
 - a surface adjoining layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain contact pocket and the surface-adjoining positions,

6

said top layer of material and said substrate being subject to application of a reverse-bias voltage, an insulating layer on the surface of the substrate and covering at least that portion between the source contact pocket and the nearest surface-adjoining position of the extended drain region, and a gate electrode on the insulating layer and electrically isolated from the substrate region thereunder which forms a channel laterally between the source contact pocket and the nearest surface-adjoining position of the extended drain region, said gate electrode controlling by field-effect the flow of current thereunder through the channel.

2. The high-voltage MOS transistor of claim 1 wherein, said top layer has a depth of one micron or less.
3. The high-voltage MOS transistor of claim 1 wherein, said top layer has a doping density higher than $5 \times 10^{16} / \text{cm}^3$ so that the mobility starts to degrade.
4. The high voltage MOS transistor of claim 1 having one channel conductivity type in combination with a complementary high voltage MOS transistor of an opposite channel conductivity type combined on the same chip and isolated from each other.
5. The high voltage MOS transistor of claim 1 combined on the same chip with a low voltage CMOS implemented device.
6. The combination of claim 5 further including, a complementary high voltage MOS transistor, and a complementary low voltage CMOS implemented device on the same chip and isolated from each other.
7. A high voltage MOS transistor comprising:
 - a semiconductor substrate of a first conductivity type having a surface,
 - a pair of laterally spaced pockets of semiconductor material of a second conductivity type within the substrate and adjoining the substrate surface,
 - a source contact connected to one pocket,
 - an extended source region of the second conductivity type extending laterally each way from the source contact pocket to surface-adjoining positions,
 - a surface adjoining layer of material of the first conductivity type on top of an intermediate portion of the extended source region between the surface-adjoining positions,
 - said top layer and said substrate being subject to application of a reverse-bias voltage,
 - a drain contact connected to the other pocket,
 - an extended drain region of the second conductivity type extending laterally each way from the drain contact pocket to surface-adjoining positions,
 - a surface adjoining layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain contact pocket and the surface-adjoining positions,
 - said top layer of material and said substrate being subject to application of a reverse-bias voltage,
 - an insulating layer on the surface of the substrate and covering at least that portion between the nearest surface-adjoining positions of the extended source region and the extended drain region, and
 - a gate electrode on the insulating layer and electrically isolated from the substrate region thereunder which forms a channel laterally between the nearest surface-adjoining positions of the extended source region and the extended drain region, said gate electrode controlling by field-effect the current flow thereunder through the channel.

* * * * *

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

POWER INTEGRATIONS, INC., a :
Delaware corporation, :
 :
Plaintiff, :
 :
v. : C.A. No. 04-1371-JJF
 :
FAIRCHILD SEMICONDUCTOR :
INTERNATIONAL, INC., a Delaware :
corporation, and FAIRCHILD :
SEMICONDUCTOR CORPORATION, a :
Delaware corporation, :
 :
Defendants. :

O R D E R

At Wilmington, this 31 day of March 2006, for the reasons
discussed in the Memorandum Opinion issued this date;

IT IS HEREBY ORDERED that the following terms and/or phrases
in U.S. Patent Nos. 4,811,075 (the "'075 patent"), 6,107,851 (the
"'851 patent"), 6,229,366 (the "'366 patent"), 6,249,876 (the
"'876 patent") are assigned the following meanings:

1. The term "**MOS transistor**" means "a metal oxide
transistor."

2. The term "**substrate**" means "the physical material
on which a transistor or microcircuit is fabricated."

3. The phrase "**a pair of laterally spaced pockets of
semiconductor material of a second conductivity type within the
substrate**" means "two laterally spaced pockets of semiconductor
material of the opposite conductivity type from the substrate."

4. The phrase "**a surface adjoining layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain contact pocket and the surface adjoining positions**" is construed according to its plain meaning, and further construction by the Court is not required.

5. The phrase "**said top layer of material**" is construed according to its plain meaning when read in the context of the claim, and further construction by the Court is not required.

6. The term "**reverse bias voltage**" means "a voltage applied across a rectifying junction with a polarity that provides a high-resistance path."

7. The phrase "**substrate region thereunder which forms a channel**" is construed according to its plain meaning when read in the context of the claim, and further construction by the Court is not required.

8. The term "**frequency jittering**" means "varying the switching frequency of a switch mode power supply about a target frequency in order to reduce electromagnetic interference."

9. The term "**coupled**" means that "two circuits are coupled when they are connected such that voltage, current or control signals pass from one to another."

10. The term "**primary voltage**" means a "base or initial voltage" and the term is not defined by reference to the

source from which it may be generated.

11. The term "**secondary voltage**" means "a subsequent or additional voltage."

12. The term "**combining**" means "adding together."

13. The term "**supplemental voltage**" means "a voltage in addition to the primary voltage."

14. The term "**soft start circuit**" is a means-plus-function element. The functions of the various "soft start circuits" are construed in accordance with the plain meaning of the claims setting forth such soft start circuit functions. The corresponding structures related to the "soft start circuit" are shown in Figures 3, 6 and 9 of the '366 patent and described in the specification of the '366 patent at col. 6, ll. 7-17; col. 6, l. 35-col. 7, l. 18; col. 11, ll. 40-50 and col. 12, ll. 5-10.

15. The phrase "**frequency variation circuit**" means "a structure that provides the frequency variation signal."

16. The phrase "**frequency variation signal**" means "an internal signal that cyclically varies in magnitude during a fixed period of time and is used to modulate the frequency of the oscillation signal within a predetermined frequency range."


UNITED STATES DISTRICT JUDGE

Appendix 1 – Side-by-side comparison of the '719 and '075 patents.

'719 Patent claim 8

8. A high voltage MOS transistor comprising:
 a semiconductor substrate of a first conductivity type having a surface,
 a pair of laterally spaced source and drain pockets of semiconductor material of a second conductivity type within the substrate and adjoining the substrate surface,
 an extended drain region of the second conductivity type extending laterally each way from said drain pocket to surface-adjoining positions,
 a surface adjoining, top layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain pocket and the surface-adjoining positions,
 said top layer of material and said substrate being subject to application of a reverse-bias voltage,
 an insulating layer on the surface of the substrate and covering at least that portion between the source pocket and the nearest surface-adjoining position of the extended drain region, and
 a gate electrode on the insulating layer and electrically isolated from the substrate region thereunder which forms a channel laterally between the source pocket and the nearest surface-adjoining position of the extended drain region, said gate electrode controlling by field-effect the flow of current thereunder through the channel.

'075 Patent claim 1

1. A high voltage MOS transistor comprising:
 a semiconductor substrate of a first conductivity type having a surface
 a pair of laterally spaced pockets of semiconductor material of a second conductivity type within the substrate and adjoining the substrate surface,
 a source contact connected to one pocket,
 a drain contact connected to the other pocket,
 an extended drain region of the second conductivity type extending laterally each way from the drain contact pocket to surface-adjoining positions,
 a surface adjoining layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain contact pocket and the surface-adjoining positions,
 said top layer of material and said substrate being subject to application of a reverse-bias voltage,
 an insulating layer on the surface of the substrate and covering at least that portion between the source contact pocket and the nearest surface-adjoining position of the extended drain region, and
 a gate electrode on the insulating layer and electrically isolated from the substrate region thereunder which forms a channel laterally between the source contact pocket and the nearest surface-adjoining position of the extended drain region, said gate electrode controlling by field-effect the flow of current thereunder through the channel.

UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

FAIRCHILD SEMICONDUCTOR
CORPORATION, a Delaware corporation,
and INTERSIL CORPORATION, a
Delaware corporation,

Plaintiffs,

v.

POWER INTEGRATIONS, INC., a
Delaware corporation,

Defendants.

C.A. No. 2:06-CV-151 (TJW)

ORDER GRANTING POWER INTEGRATIONS' MOTION TO DISMISS

ON THIS DAY, came on to be considered Power Integrations, Inc.'s Motion to Dismiss, or in the Alternative, to Transfer This Case to Delaware in the above-styled and numbered cause. After considering said motion, the Court is of the opinion that said motion should be GRANTED, and that all matters in this suit against Power Integrations, Inc. are dismissed with prejudice.

**UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS**

FAIRCHILD SEMICONDUCTOR
CORPORATION, a Delaware corporation,
INTERSIL AMERICAS, INC., a Delaware
corporation and INTERSIL CORPORATION,
a Delaware corporation
Plaintiffs,

V.

POWER INTEGRATIONS, INC., a Delaware
corporation.
Defendant

2:06-cv-151 (TJW)

POWER INTEGRATIONS, INC.'S CORPORATE DISCLOSURE STATEMENT

Pursuant to Rule 7.1 of the Federal Rules of Civil Procedure, Defendant Power Integrations, Inc. hereby states that it is a publicly held corporation organized under the laws of Delaware. No publicly held corporation owns 10% or more of Power Integration, Inc.'s stock.

Dated: June 19, 2006

Respectfully submitted,

OF COUNSEL

By: /s/ Michael E. Jones

Frank E. Scherkenbach
Fish & Richardson P.C.
225 Franklin Street
Boston, Massachusetts 02110-2804
Telephone: (617) 542-5070
Facsimile: (617) 542-8906

Michael E. Jones
State Bar No. 10929400
mikejones@potterminton
POTTER MINTON
A Professional Corporation
110 N. College, Suite 500
Tyler, TX 75702
Telephone: (903) 597-8311
Facsimile: (903) 593-0846

Attorneys for Defendant
POWER INTEGRATIONS, INC.

CERTIFICATE OF SERVICE

The undersigned hereby certifies that all counsel of record who are deemed to have consented to electronic service are being served with a copy of this document via the Court's CM/ECF system per Local Rule CV-5(a)(3) on June 19, 2006. Any other counsel of record will be served by facsimile transmission and first class mail.

/s/ Michael E. Jones

Michael E. Jones

UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

FAIRCHILD SEMICONDUCTOR
CORPORATION, a Delaware corporation,
and INTERSIL CORPORATION, a
Delaware corporation,

Plaintiffs,

v.

POWER INTEGRATIONS, INC., a
Delaware corporation,

Defendants.

C.A. No. 2-06CV-151 JTW

**POWER INTEGRATIONS' MOTION TO DISMISS OR, IN THE ALTERNATIVE, TO
TRANSFER THIS CASE TO DELAWARE**

Fairchild does not have standing to prosecute this case because it does not own U.S. Patent No. 5,264,719 ("the '719 patent") and is not the exclusive licensee of the patent. Fairchild's recent efforts to buy a cause of action on the '719 patent from Intersil are insufficient as a matter of law, and no amount of hand-waving on the part of the plaintiffs can cure that fatal defect. Therefore, pursuant to Rule 12(b)(1) of the Federal Rules of Civil Procedure, Power Integrations hereby moves to dismiss this case for lack of standing.

In the alternative, Power Integrations asks that the Court transfer this action to the District of Delaware, where the parties are already engaged in a dispute regarding the '719 patent. Specifically, the parties are seeking to determine whether the '719 patent was conceived before a Power Integrations patent asserted in the Delaware action. The Delaware case is set for trial this year, and all parties in the present suit are involved in the Delaware matter—Power

Integrations is the Delaware plaintiff, Fairchild Semiconductor is the defendant, and Intersil is a third party alleging prior inventorship and working with Fairchild to attempt to prove prior inventorship. As a result, this District is not the proper venue in which to address the '719 patent.

I. FACTUAL BACKGROUND

On October 20, 2004, Power Integrations, Inc. ("Power Integrations") filed suit against Fairchild Semiconductor Corporation and Fairchild Semiconductor International, Inc. (collectively "Fairchild") in the District Court for the District of Delaware, alleging infringement of four U.S. patents. [See Declaration of Mike Jones ("Jones Decl.") Ex. A.¹] Fairchild claims that one of the four patents, U.S. Patent No. 4,811,075 ("the '075 patent"), is invalid in view of the '719 patent, the only patent asserted in this case. Fairchild and Power Integrations have taken extensive discovery with respect to the '719 patent in the Delaware action, and the dispute in Delaware turns on who was the first to invent the technology in the '075 and '719 patents. A Delaware jury will resolve this critical issue later this year, as the trial on validity issues is set to begin on December 4. [Ex. B (Pretrial Conference Tr.) at 30-31.]

During the course of the Delaware litigation, Fairchild bought a license "to enforce" the '719 patent against a single entity: Power Integrations. [See Fairchild's Amended Complaint ("Amended Complaint") Ex. E.] By the terms of the March 30, 2006 agreement, Intersil granted Fairchild "the sole and exclusive right . . . to assert, litigate and prosecute claims of [i]nfringement under the ['719] patent[] against [Power Integrations]." [Amended Complaint Ex. E (Patent License Agreement of Mar. 30, 2006 ("PLA")) at §§ 1.2, 3.1.] However, Fairchild's hunting license does not provide any underlying right beyond the right to sue—it

¹ All citations are to the accompanying Declaration of Mike Jones, unless noted otherwise.

does not grant Fairchild the exclusive right to make, use, or sell the alleged invention of the '719 patent.²

On April 11, 2006, Fairchild issued a press release announcing the license and the institution of this suit, noting that Fairchild “recently secured exclusive rights to assert the [’719] patent against Power Integrations.” [Ex. C (April 11, 2006 Press Release – *Fairchild Semiconductor Files Patent Infringement Lawsuit Against Power Integrations, Inc.*)] On May 18, 2006, Intersil and Fairchild executed a Supplemental Agreement attempting to modify the PLA to make yet another entity, Intersil Americas, the original party to the PLA. [Amended Complaint Ex. F (Agreement of May 18, 2006).] None of these actions conferred standing on Fairchild.

II. LEGAL AUTHORITY

To have standing to assert patent infringement, “the plaintiff must demonstrate that it held enforceable title to the patent at the inception of the lawsuit.” *Paradise Creations, Inc. v. U V Sales, Inc.*, 315 F.3d 1304, 1309 (Fed. Cir. 2003). Where the plaintiff lacks a cognizable injury at the time it filed suit, such defect in standing cannot be cured after the inception of the lawsuit. *Id.* at 1310. In order to bring an action for damages resulting from infringement, the patentee must not only have legal title to the patent, but must have been its owner at the time of the infringement. *Crown Die & Tool Co. v. Nye Tool & Machine Works*, 261 U.S. 24, 41 (1923); *Arachnid, Inc. v. Merit Indus., Inc.*, 939 F.2d 1574, 1579 (Fed. Cir. 1991) (“[O]ne seeking to recover money damages for infringement of a United States patent . . . must have held the legal title to the patent during the time of the infringement.”); *Heidelberg Harris, Inc. v. Loebach*, 145 F.3d 1454, 1458 (Fed. Cir. 1998) (“[A] plaintiff cannot sue for patent infringement occurring

² As part of a broader cross-license with Intersil, Fairchild took a license to practice the '719 patent in certain limited capacities several years ago. But that license is not exclusive and, as Fairchild has implicitly acknowledged by entering into at least two later agreements specific to the '719 and Power Integrations, has no bearing on the instant dispute. Plaintiffs have not asserted—and cannot assert—that the earlier Fairchild-Intersil license in any way confers standing in this case.

prior to the time the plaintiff actually obtained legal title to the asserted patent.”); *Mas-Hamilton Group v. LaGard, Inc.*, 156 F. 3d 1206, 1210 (Fed. Cir. 1998) (only the owner of the patent at the time of the infringement can bring an action for damages resulting from that infringement) (dictum).

A patentee may divide its “bundle of rights” and convey, or share, the right to sue infringers. The patentee may, by instrument in writing, assign, grant, convey (1) the entire patent, (2) an undivided part or share of the entire patent, or (3) all rights under the patent in a specified geographical region. *Waterman v. Mackenzie*, 138 U.S. 252, 255 (1891). Such transfers constitute an assignment, and they vest the assignee with title in the patent and a right to sue infringers, either as sole plaintiff or as co-plaintiff depending on the nature and extent of the rights conferred. *Id.* However, a transfer of less than one of these three interests is a mere license, giving the licensee no title in the patent, and no right to sue for infringement in the licensee’s own name. *Id.* Fairchild has none of these three interests.

A narrow exception to the rule that only patentees and successors in interest may sue for infringement applies when a party obtains an exclusive license to a patent and holds “all substantial rights” under the patent. *See Textile Productions, Inc. v. Mead Corp.*, 134 F.3d 1481, 1483-85 (Fed. Cir. 1998); *Vaupel Textilmaschinen KG v. Meccanica Euro Italia S.P.A.*, 944 F.2d 870, 875 (Fed. Cir. 1991). To establish independent standing as an exclusive licensee, though, a party must have received both the right to exclude others from making, using, or selling the patented technology and the patent holder’s promise that no other party may practice the patented technology. *Rite-Hite Corp. v. Kelley Co.*, 56 F.3d 1538, 1552 (Fed. Cir. 1995).

However, this narrow exception does not apply to non-exclusive licensees; even if the patent holder is a party to the suit, a non-exclusive licensee does not have independent standing to sue for infringement. *Kalman v. Berlyn Corp.*, 914 F.2d 1473, 1481-82 (Fed. Cir. 1990)

(stating a non-exclusive licensee lacks standing to sue for infringement even if joined with the patent holder and further noting that no “licensee who joins the patentee [has] standing to sue an infringer”). Furthermore, a non-exclusive licensee who has not been granted the right to exclude others has no legally recognized interest that would entitle it to bring or join an infringement action. *Abbott Lab. v. Diamedix Corp.*, 47 F.3d 1128, 1131 (Fed. Cir. 1995). A licensee may only bring an infringement suit to protect a property interest it received from the patentee. See *Ortho Pharmaceutical Corp. v. Genetics Institute, Inc.*, 52 F.3d 1026, 1034 (1995) (“[I]t is the licensee’s beneficial ownership of a right to prevent others from making, using, or selling the patented technology that provides the foundation for co-plaintiff standing.”). Thus, a contract clause cannot by itself grant standing to a licensee if the licensee would otherwise not have standing to bring the suit. *Id.* (“[A] right to sue clause cannot negate the requirement that . . . a licensee must have beneficial ownership of some of the patentee’s proprietary rights.”).

III. ARGUMENT

A. Fairchild Does Not Have Standing and Cannot Sue Power Integrations on the ’719 Patent.

Fairchild has no standing to sue for infringement because Fairchild is not, and never was, the patentee or successor in interest to the ’719 patent, and at no time has Fairchild held all substantial rights to the patent. Patent standing rules are strict: a party seeking to recover for alleged patent infringement must either have held legal title to the patent at the time of the alleged infringement, or have been assigned the right to recover for that infringement by the legal title holder together with an assignment of all substantial rights under the patent. *Crown Die & Tool Co.*, 261 U.S. at 41; *Ortho Pharm.*, 52 F.3d at 1034. Only a patentee may bring an action for patent infringement, and Fairchild is not the patentee. Legal title appears to have been held at all times by Intersil (or Intersil’s predecessor Harris Corporation), making Intersil the only party

with any right to recover for alleged patent infringement, regardless of Fairchild's purported "license to enforce" the patent against Power Integrations.

To overcome the rule that only patentees and successors in interest may sue for infringement, Fairchild would need an exclusive license and would need to demonstrate a sufficient proprietary injury to one of the rights that flows from the patent. *Rite-Hite*, 56 F.3d at 1552. In essence, though, Fairchild has a "bare license," because it has no exclusive right to keep others from making, using, or selling products making use of the patented technology, and Fairchild suffers no legally cognizable harm when a third-party makes, uses, or sells the patented technology. *See Abbott*, 47 F.3d at 1131. As noted above, a bare licensee has no standing at all. *See Rite-Hite*, 56 F.3d at 1552; *Ortho Pharm.*, 52 F.3d at 1034. Fairchild therefore has no legally recognized interest that entitles it to bring or join an infringement action.

Intersil's contractual grant of the "exclusive right to sue" is not sufficient to confer standing to Fairchild. "A patentee may not give a right to sue to a party who has no proprietary interest in the patent." *Ortho Pharm.*, 52 F.3d at 1034 (collecting cases describing non-exclusive licensees lack standing to enforce a patent); *Rite-Hite*, 56 F.3d at 1553. *See also Phila. Brief Case Co. v. Specialty Leather Prods. Co.*, 145 F. Supp. 425, 429-30 (D.N.J. 1956), *aff'd*, 242 F.2d 511 (3rd Cir. 1957) (contract clause cannot give right to sue where licensee would otherwise have no such right). The Patent License Agreement attempts to convey to Fairchild "the sole and exclusive right . . . to assert, litigate and prosecute claims of [i]nfringement under the ['719 and related] patents against [Power Integrations]" [Amended Complaint Ex. E (Patent License Agreement of Mar. 30, 2006) at §§ 1.2, 3.1], but the license agreement simply cannot supersede the legal requirement that the licensee have all substantial rights in order to have standing to sue for infringement.

The Federal Circuit has explicitly rejected the possibility that a patentee could grant a hunting license along the lines of the license contemplated between Fairchild and Intersil. *See Prima Tek II, LLC v. A-Roo Co.*, 222 F.3d 1372, 1381 (Fed. Cir. 2000). The court in *Prima Tek II* further noted that “[i]n evaluating whether a particular license agreement transfers all substantial rights in a patent to the licensee, we pay particular attention to whether the agreement conveys *in full* the right to exclude others from making, using and selling the patented invention in the exclusive territory.” *Id.* at 1379 (emphasis in original, citations omitted). Just last month, the Federal Circuit affirmed these principals:

[T]he plaintiff must be within the class of persons legally protected by the statute under which the individual seeks relief. For example, in *Ortho Pharmaceutical Corp. v. Genetics Institute, Inc.*, 52 F.3d 1026, 1030-31 (Fed.Cir.1995), we held that nonexclusive patent licensees lack Article III standing to sue for infringement because “economic injury alone does not provide standing to sue under the patent statute a licensee must hold some of the proprietary sticks from the bundle of patent rights,” otherwise the licensee “suffers no legal injury from infringement and, thus, has no standing” *See also Intellectual Prop. Dev., Inc. v. TCI Cablevision of Cal., Inc.*, 248 F.3d 1333, 1345 (Fed.Cir.2001) (“[A] nonexclusive license . . . confers no constitutional standing on the licensee under the Patent Act to bring suit or even to join a suit with the patentee because a nonexclusive (or ‘bare’) licensee suffers no legal injury from infringement.”).

Willis v. Government Accountability Office, --- F.3d ----, 2006 WL 1329929 (Fed. Cir. May 17, 2006). The Court should therefore decline to expend its resources on Fairchild’s ill-conceived distraction from the Delaware case.

Moreover, Intersil’s presence in this suit does not overcome Fairchild’s lack of independent standing. Adding the patent holder as a co-plaintiff would only defeat a challenge on the grounds of standing if Fairchild had the exclusive rights to make, use and sell the patented technology, *Abbott*, 47 F.3d at 1131, but as Fairchild does not have such exclusive rights, it lacks standing to bring a cause of action for infringement. The Court should therefore dismiss this action for lack of standing.

B. If the Court Does Not Dismiss This Action, It Should Transfer the Case to Delaware to Be Resolved In The Court Which is Already Addressing the Patent-in-Suit.

In the alternative, Power Integrations asks the Court to transfer this action to the United States District Court for the District of Delaware, where a previously filed case involving the same parties and an identical dispute regarding who was first to invent the technology is already pending. There is a substantial overlap between this action and the Delaware case set for trial this December, as the outcome of both suits depends on the Delaware case's inventorship findings, and both the Fifth Circuit and the Federal Circuit both follow a first-to-file rule for cases having substantial overlap. Further, the interest of justice suggests transfer under the federal venue statute. Therefore, if the Court does not dismiss this case outright, it should transfer to the matter to Delaware.

1. The Key Issue With Respect to the Sole Patent-in-Suit, an Inventorship Dispute, is Already Before the Delaware Court.

In support of its invalidity claim with respect to the '075 patent in Delaware, Fairchild asserted that the '719 patent, the only patent in this case, is key invalidating prior art to the '075 patent. [Ex. D ('719 patent claim chart from Fairchild's invalidity contentions).] Fairchild and Power Integrations have taken extensive discovery with respect to the '719 patent, and the dispute in Delaware turns on who was the first to invent the technology in the '075 and '719 patents. The Delaware jury will resolve this critical issue later this year.

The '719 Patent was filed on May 24, 1991, over four years after the '075 Patent's April 1987 filing date. During prosecution of the '719 patent, the Applicant copied large portions of the claims of the '075 patent into the '719 patent. [Ex. E at I-000228 ("[A]lthough not identically copied, [the claim] is considered to be generic to the invention defined in claim 1 of U.S. Patent No. 4,811,075 to Eklund." (underlining in original)).] A brief comparison of claim 8

of the '719 Patent to claim 1 of the '075 Patent demonstrates this copying of the '075 patent claim language. [Appendix 1; Ex. F-G.] Thus, the same questions regarding conception and inventorship that are central to the Delaware trial would also arise in this suit.

2. The First-To-File Rule Compels the Transfer of This Case.

In patent cases, “the forum of the first-filed case is favored, unless considerations of judicial and litigant economy, and the just and effective disposition of disputes, require otherwise.” *Genentech, Inc. v. Eli Lilly & Co.*, 998 F.2d 931, 937 (Fed. Cir. 1993), *overruled on other grounds*, *Wilton v. Seven Falls, Inc.*, 515 U.S. 277 (1995); *accord Save Power Ltd. v. Syntek Finance Corp.*, 121 F.3d 947, 950 (5th Cir. 1997) (“The Fifth Circuit adheres to the general rule that the court in which an action is first filed is the appropriate court to determine whether subsequently filed cases involving substantially similar issues should proceed.”) The Federal Circuit regards the application of the first-to-file rule as an issue that “is important to national uniformity in patent practice.” *Genentech*, 998 F.2d at 937. Application of the rule requires a three-part analysis by the court in a later-filed action:

1. The court must confirm that the case before it was filed later than an earlier case in another district. *Genentech*, 998 F.2d at 937; *accord Syntek Finance*, 121 F.3d at 950-51.
2. The court must then determine whether the earlier-filed case is likely to raise issues that substantially overlap with the case on its own docket. *Syntek Finance*, 121 F.3d at 950-51.
3. If so, the court must transfer the action before it to the first-filed court unless it finds that it would be “unjust or inefficient” to do so. *Genentech*, 998 F.2d at 938; *accord Mann Mfg., Inc. v. Hortex, Inc.*, 439 F.2d 403 (5th Cir. 1971) (transfer required absent “compelling” reasons to favor later action).

After the second case is transferred, the first-filed court decides whether that later action “must be dismissed, stayed, or transferred and consolidated.” *Sutter Corp. v. P&P Indus., Inc.*, 125

F.3d 914, 920 (5th Cir. 1997). In favoring transfer of related cases, the rule is designed to avoid the waste and duplication that would result from piecemeal resolution of similar issues. *West Gulf Maritime Assoc. v. ILA Deep Sea Local 24*, 751 F.2d 721, 728-29 (5th Cir. 1985); cf. *Optical Recording Corp. v. Capitol-EMI Music, Inc.*, 803 F. Supp. 971 (D. Del. 1992) (proceeding with later-filed case because the Delaware court was already familiar with the technology and patents at issue in both cases).

a. The Delaware Action Is The First-Filed Action.

Power Integrations filed suit against Fairchild on October 20, 2004, in Delaware, over 17 months before the current action was brought. Fairchild has not only answered the complaint in the Delaware case, but the parties have already conducted extensive discovery, are finished with claim construction, and have completed technical expert discovery. In fact, the parties recently had a pre-trial conference, and the Delaware Court provided trial dates for later this year (September for some issues and December for others). [Ex. B at 30-31.]

b. There Is Substantial Overlap in the Subject Matter of the Patents at Issue.

Cases do not need to have exactly the same subject matter to meet the “substantial overlap” test. “[R]egardless of whether or not the suits here are identical, if they overlap on the substantive issues, the cases would be required to be consolidated in . . . the jurisdiction first seized of the issues.” *Mann Mfg.*, 439 F.2d at 408 n.6; see also *Syntek Finance*, 121 F.3d at 950 (“The rule does not, however, require that cases be identical.”)

The Fifth Circuit has addressed the meaning of “substantial overlap” in the context of patent litigation in *Mann Mfg.* 439 F.2d at 405-408. There, Goodrich sued in the Southern District of New York seeking a declaratory judgment that a number of its products did not infringe a patent owned by Mann. *Id.* at 405. After Goodrich commenced that action, Mann

sued Goodrich and Hortex on the same patent in the Western District of Texas and then sued on another related patent. *Id.* at 405-406. The Fifth Circuit acknowledged that these two cases involved distinct patents, but despite the difference in patent claims, the Court found that the cases shared substantial issues and held that the New York court was the proper court to determine how to proceed with respect to the later added patent. *Id.* at 407-08.

Here, the Delaware and Texas cases bear even more similarities than in *Mann Mfg.*, as both cases address the same technology and share disputes regarding nearly identical claims. The similarity is particularly evident when comparing claim 8 from the '719 Patent against claim 1 of the '075 Patent (shown side-by-side in Appendix 1). The parties have taken extensive fact and expert discovery on the question of inventorship in the Delaware case, and the Delaware Court has already issued a claim construction order. [Ex. H (Claim Construction Order).] The identical question of inventorship, likely determinative for validity purposes, will be decided at trial in Delaware later this year on the basis of the same fact witnesses, documents, and expert testimony that would apply here. As such, to proceed with both the Texas and Delaware cases separately would result in precisely the kind of wasteful duplication of time and effort that the first-to-file rule is designed to prevent. *West Gulf*, 751 F.2d at 729 (“The concern manifestly is to avoid the waste of duplication . . . and to avoid piecemeal resolution of issues that call for a uniform result.”). Allowing this case to proceed in Texas would also risk conflicting outcomes on a single issue. To avoid this confusion and injustice, Power Integrations asks this Court to transfer the action to Delaware.

c. There Are No Compelling Circumstances That Justify Disregarding the First-To-File Rule.

Once the first-to-file rule applies, the issues should be decided in the first-filed suit, unless it would be “unjust or inefficient” to do so. *Genentech*, 998 F.2d at 938. In deciding

whether justice and efficiency require disregarding the first-to-file rule, the Federal Circuit considers such factors as: (1) the convenience and availability of witnesses, (2) the absence of jurisdiction over all parties, (3) the possibility of consolidation with related litigation, and (4) whether the first-filed case involves the real parties in interest. As discussed below, none of these factors weighs against transfer to Delaware.

First, the convenience and availability of witnesses do not favor the Eastern District of Texas. All three parties in this case are Delaware corporations, with their principal places of business alleged to be in either California or Maine. All of the patents in question, including those from the Delaware case, list the inventors' residence as either California or Florida. In fact, Power Integrations is not aware of a single fact witness located in the state of Texas.

Second, there are no jurisdictional reasons to disregard the first-to-file rule. Not only are Fairchild and Intersil Delaware corporations, but Fairchild also answered and counterclaimed in the Delaware case without asserting a defense based on a lack of personal jurisdiction or on the inconvenience of that forum. As such, Fairchild has agreed to jurisdiction and waived any right to object. *See Golden v. Cox Furniture Mfg. Co., Inc.*, 683 F.2d 115, 118 (5th Cir. 1982) (party waives right to object to personal jurisdiction if it does not make motion under Rule 12 or assert defense in answer); *see also* Fed. R. Civ. P. 12(h)(1). Intersil responded to subpoenas in the Delaware case and, as a Delaware corporation, cannot contest personal jurisdiction in Delaware.

The third factor also provides no basis for declining this transfer request, as there is no related litigation in the Eastern District of Texas with which the two actions could be consolidated. In fact, the opposite is true. As to the fourth factor, whether the first-filed case involves the real parties in interest, defendants will likely argue that Intersil is not a party to the Delaware action. However, Intersil has been working with Fairchild in Delaware case, shares

local counsel with Fairchild in Delaware, and has produced documents and things related to the '719 patent in Delaware. Intersil has also participated in and paid the inventor of the '719 patent to sit for a deposition, in addition to preparing and presenting alleged corroborating witnesses on the '719 patent. As such, Intersil has been an active participant in the Delaware litigation and is well aware that the inventorship contest between the '075 patent and the '719 patent will be decided in the Delaware case.

3. The Interest of Justice Requires Hearing this Action in Delaware.

Even if this Court does not transfer using the first-to-file rule, it should transfer the case to the District of Delaware because it is a more convenient and cost effective place to resolve the instant dispute. The potential for inconsistent rulings from the plaintiffs' forum shopping imposes significant inconvenience on Power Integrations, and to the public at large, in the form of uncertainty. Further, having presided over the Delaware case, the Delaware court will be intimately familiar with the technology and issues in the present suit, including specifically the inventorship contest, which plaintiffs apparently want to challenge all over again here. In addition, the need to re-litigate the inventorship contest imposes an inconvenience and burden on Power Integrations.

a. Cases Are Transferred at the Court's Discretion, Focusing on Convenience and Justice.

A district court may transfer any civil case "[f]or the convenience of parties and witnesses, in the interest of justice, . . . to any other district or division where it might have been brought." 28 U.S.C. § 1404(a). In exercising its discretion to transfer a pending case, courts consider "all relevant factors to determine whether or not on balance the litigation would more conveniently proceed and the interests of justice be better served by transfer to a different

forum.” *Peteet v. Dow Chemical Co.*, 868 F.2d 1428, 1436 (5th Cir. 1989) (internal quotations and citations omitted).

b. Both Convenience and Justice Favor Transfer to Delaware.

The potential for inconsistent findings imposes a great inconvenience on Power Integrations and burdens the public at large. The Delaware case will proceed to judgment first, and that judgment is *res judicata*. Because the parties can rely on the Delaware court’s findings, in particular the determination on the inventorship issue, all preparations made meanwhile to re-litigate the issues in this District would be wasted. Absent such consistent treatment, it could take years to untangle the various issues presented with multiple constructions and inventorship contentions on these related patents. Indeed, given the stage of the Delaware case, it is likely that issues from that case would be pending on appeal at the same time that plaintiffs ask this Court to decide those same issues. The public would have no idea what it could and could not do in this field.

Moreover, plaintiffs have known for over a year that inventorship would be decided in the Delaware case, and they could have filed a counterclaim asserting the ’719 patent against Power Integrations early in the Delaware case. Instead, they chose to wait until the Delaware case was nearly completed, and then filed this suit in another forum, despite the fact that rulings and findings from the Delaware case are important, and in some cases determinative, in their present suit.

Finally, having presided over the Delaware case, the District of Delaware will be intimately familiar with the technology and issues in the present suit, including specifically claim constructions and the inventorship contest. The Delaware court will also be in the best position to decide evidentiary issues such as what evidence, rulings, and stipulations from the old case

may be employed in what ways in the present suit. This Court should therefore transfer the instant case to Delaware under Section 1404(a), to the extent it does not do so under the first-filed rule or does not dismiss the suit outright for lack of standing.

III. CONCLUSION

For the reasons stated above, this Court should grant Power Integrations' motion to dismiss for lack of standing or, in the alternative, transfer the case to Delaware to be resolved by a Court already dealing with the '719 patent and familiar with the technology at issue in both cases.

Dated: June 19, 2006

Respectfully submitted,

OF COUNSEL

Frank E. Scherkenbach
Fish & Richardson P.C.
225 Franklin Street
Boston, Massachusetts 02110-2804
Telephone: (617) 542-5070
Facsimile: (617) 542-8906

By: /s/ Michael E. Jones
Michael E. Jones
State Bar No. 10929400
mikejones@potterminton
POTTER MINTON
A Professional Corporation
110 N. College, Suite 500
Tyler, TX 75702
Telephone: (903) 597-8311
Facsimile: (903) 593-0846

Attorneys for Defendant
POWER INTEGRATIONS, INC.

CERTIFICATE OF SERVICE

The undersigned hereby certifies that all counsel of record who are deemed to have consented to electronic service are being served with a copy of this document via the Court's CM/ECF system per Local Rule CV-5(a)(3) on June 19, 2006. Any other counsel of record will be served by facsimile transmission and first class mail.

/s/ Michael E. Jones

Michael E. Jones

UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS

FAIRCHILD SEMICONDUCTOR
CORPORATION, a Delaware corporation,
INTERSIL AMERICAS, INC., a Delaware
corporation and INTERSIL CORPORATION,
a Delaware corporation
Plaintiffs,

v.

POWER INTEGRATIONS, INC., a Delaware
corporation.
Defendant

2:06cv-151 (TJW)

**DECLARATION OF MICHAEL E. JONES IN SUPPORT OF POWER
INTEGRATIONS, INC.'S MOTION TO DISMISS, OR IN THER ALTERNATIVE, TO
TRANSFER THIS CASE TO DELAWARE**

I, Michael E. Jones, declare same based upon information and belief:

1. I am a shareholder at Potter Minton PC in Tyler, Texas. I am one of the attorneys representing defendant Power Integrations, Inc. in the above-captioned matter filed by Plaintiffs Fairchild Semiconductor Corporation ("Fairchild"), Intersil Americas, Inc. and Intersil Corporation ("Intersil").

2. Attached hereto as Exhibit "A" is a true and correct copy of the First Amended Complaint for Patent Infringement filed by Power Integrations against Fairchild Semiconductor Corporation and Fairchild Semiconductor International, Inc. in the United States District Court for the District of Delaware on June 30, 2005 ("the Delaware Lawsuit").

3. I am informed and believe that attached hereto as Exhibit "B" is a true and correct copy of the transcript of the Pretrial Conference held on May 31, 2006 in the Delaware Lawsuit.

4. I am informed and believe that attached hereto as Exhibit "C" is a true and correct copy of Fairchild's press release dated April 11, 2006.

5. I am informed and believe that attached hereto as Exhibit "D" is a true and correct copy of a claim chart regarding the '719 patent asserted in this case which is part of Fairchild's invalidity contentions in the Delaware case as set forth in its Supplemental Responses to Power Integrations' First Set of Interrogatories, dated June 30, 2005.

6. I am informed and believe that attached hereto as Exhibit "E" is a true and correct copy of an excerpt from the '719 file history concerning the '075 patent claim language.


7. I am informed and believe that attached hereto as Exhibit "F" is a true and correct copy of the '719 Patent.

8. I am informed and believe that attached hereto as Exhibit "G" is a true and correct copy of the '075 Patent.

9. I am informed and believe that attached hereto as Exhibit "H" is a true and correct copy of Claim Construction Order issued on March 31, 2006 in the Delaware Lawsuit.

I declare under penalty of perjury that the foregoing is true and correct to the best of my information and belief.

Signed: June 19, 2006



Michael E. Jones

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

POWER INTEGRATIONS, INC., a
Delaware corporation,

Plaintiff,

v.

FAIRCHILD SEMICONDUCTOR
INTERNATIONAL, INC., a Delaware
corporation, and FAIRCHILD
SEMICONDUCTOR CORPORATION, a
Delaware corporation

Defendants.

C.A. No. 047-1371-JJF

JURY TRIAL REQUESTED

FIRST AMENDED COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Power Integrations, Inc. hereby alleges as follows:

THE PARTIES

1. Power Integrations, Inc. (“Power Integrations”) is incorporated under the laws of the state of Delaware, and has a regular and established place of business at 5245 Hellyer Avenue, San Jose, California, 95138.

2. Upon information and belief, defendant Fairchild Semiconductor International, Inc. is incorporated under the laws of the state of Delaware, with its headquarters located at 82 Running Hill Road, South Portland, Maine, 04106. Upon information and belief, defendant Fairchild Semiconductor Corporation is incorporated under the laws of the state of Delaware, with its headquarters located at 82 Running Hill Road, South Portland, Maine, 04106. (Fairchild Semiconductor International, Inc. and Fairchild Semiconductor Corporation hereinafter collectively “Fairchild Semiconductor.”)

JURISDICTION AND VENUE

3. This action arises under the patent laws of the United States, Title 35 U.S.C. § 1 *et seq.* This Court has subject matter jurisdiction under 28 U.S.C. §§ 1331 and 1338(a).

4. Upon information and belief, this Court has personal jurisdiction over defendants because defendants are incorporated, doing business and advertising in this judicial District.

5. Upon information and belief, venue is proper in this Court pursuant to 28 U.S.C. §§ 1391(b), (c) and 1400 because the defendants are subject to personal jurisdiction in this judicial District.

GENERAL ALLEGATIONS

6. Power Integrations' products include its integrated pulse width modulation ("PWM") integrated circuits that are used in power supplies for electronic devices such as cellular telephones, LCD monitors and computers. These products are sold throughout the United States, including Delaware.

7. Upon information and belief, defendants manufacture PWM integrated circuits devices (e.g., devices intended for use in power conversion applications such as LCD monitor power supplies or battery chargers for portable electronics), and directly and through their affiliates, uses, imports, sells, and offers to sell the same throughout the United States, including Delaware.

FIRST CAUSE OF ACTION

INFRINGEMENT OF U.S. PATENT NO. 6,107,851

8. The allegations of paragraphs 1-7 are incorporated as though fully set forth herein.

9. Power Integrations is now, and has been since its issuance, the assignee and sole owner of all right, title, and interest in United States Patent No. 6,107,851, entitled "Offline Converter with Integrated Softstart and Frequency Jitter" ("the '851

patent”), which was duly and legally issued on August 22, 2000. A true and correct copy of the ’851 patent is attached hereto as Exhibit A.

10. Upon information and belief, defendants have been and are now infringing, inducing infringement, and contributing to the infringement of the ’851 patent by making, using, importing, selling, and offering to sell devices, including PWM integrated circuit devices, and/or inducing or contributing to the importation, use, offer for sale and sale by others of such devices covered by one or more claims of the ’851 patent, all to the injury of Power Integrations.

11. Defendants’ acts of infringement have injured and damaged Power Integrations.

12. Defendants’ infringement has caused irreparable injury to Power Integrations and will continue to cause irreparable injury until defendants are enjoined from further infringement by this Court.

13. Upon information and belief, Defendants’ infringement has been, and continues to be, willful so as to warrant enhancement of damages awarded as a result of its infringement.

SECOND CAUSE OF ACTION

INFRINGEMENT OF U.S. PATENT NO. 6,249,876

14. The allegations of paragraphs 1-7 are incorporated as though fully set forth herein.

15. Power Integrations is now, and has been since its issuance, the assignee and sole owner of all right, title, and interest in United States Patent No. 6,249,876, entitled “Frequency Jittering Control for Varying the Switching Frequency of a Power Supply” (“the ’876 patent”), which was duly and legally issued on June 19, 2001. A true and correct copy of the ’876 patent is attached hereto as Exhibit B.

16. Upon information and belief, defendants have been and are now infringing, inducing infringement, and contributing to the infringement of the ’876 patent

by making, using, importing, selling, and offering to sell devices, including PWM integrated circuit devices and/or inducing or contributing to the importation, use, offer for sale and sale by others of such devices covered by one or more claims of the '876 patent, all to the injury of Power Integrations.

17. Defendants' acts of infringement have injured and damaged Power Integrations.

18. Defendants' infringement has caused irreparable injury to Power Integrations and will continue to cause irreparable injury until defendants are enjoined from further infringement by this Court.

19. Upon information and belief, Defendants' infringement has been, and continues to be, willful so as to warrant enhancement of damages awarded as a result of its infringement.

THIRD CAUSE OF ACTION

INFRINGEMENT OF U.S. PATENT NO. 6,229,366

20. The allegations of paragraphs 1-7 are incorporated as though fully set forth herein.

21. Power Integrations is now, and has been since its issuance, the assignee and sole owner of all right, title, and interest in United States Patent No. 6,229,366, entitled "Off-Line Converter with Integrated Softstart and Frequency Jitter" ("the '366 patent"), which was duly and legally issued on May 8, 2001. A true and correct copy of the '366 patent is attached hereto as Exhibit C.

22. Upon information and belief, defendants have been and are now infringing, inducing infringement, and contributing to the infringement of the '366 patent by making, using, importing, selling, and offering to sell devices, including PWM integrated circuit devices and/or inducing or contributing to the importation, use, offer for

sale and sale by others of such devices covered by one or more claims of the '366 patent, all to the injury of Power Integrations.

23. Defendants' acts of infringement have injured and damaged Power Integrations.

24. Defendants' infringement has caused irreparable injury to Power Integrations and will continue to cause irreparable injury until defendants are enjoined from further infringement by this Court.

25. Upon information and belief, Defendants' infringement has been, and continues to be, willful so as to warrant enhancement of damages awarded as a result of its infringement.

FOURTH CAUSE OF ACTION

INFRINGEMENT OF U.S. PATENT NO. 4,811,075

26. The allegations of paragraphs 1-7 are incorporated as though fully set forth herein.

27. Power Integrations is now, and has been since its issuance, the assignee and sole owner of all right, title, and interest in United States Patent No. 4,811,075, entitled "High Voltage MOS Transistors" ("the '075 patent"), which was duly and legally issued on March 7, 1989. A true and correct copy of the '075 patent is attached hereto as Exhibit D.

28. Upon information and belief, defendants have been and are now infringing, inducing infringement, and contributing to the infringement of the '075 patent by making, using, importing, selling, and offering to sell devices, including PWM integrated circuit devices and/or inducing or contributing to the importation, use, offer for sale and sale by others of such devices covered by one or more claims of the '075 patent, all to the injury of Power Integrations.

29. Defendants' acts of infringement have injured and damaged Power Integrations.

30. Defendants' infringement has caused irreparable injury to Power Integrations and will continue to cause irreparable injury until defendants are enjoined from further infringement by this Court.

31. Upon information and belief, Defendants' infringement has been, and continues to be, willful so as to warrant enhancement of damages awarded as a result of its infringement.

PRAYER FOR RELIEF

WHEREFORE, Plaintiff requests the following relief:

- (a) judgment against defendants as to willful infringement of the '851 patent;
- (b) judgment against defendants as to willful infringement of the '876 patent;
- (c) judgment against defendants as to willful infringement of the '366 patent;
- (d) judgment against defendants as to willful infringement of the '075 patent;
- (e) a permanent injunction preventing defendants and their officers, directors, agents, servants, employees, attorneys, licensees, successors, assigns, and customers, and those in active concert or participation with any of them, from making, using, importing, offering to sell or selling any devices that infringe any claim of the '851, '876, '366, or '075 patents;
- (f) judgment against defendants for money damages sustained as a result of defendants' infringement of the '851, '876, '366, and '075 patents;
- (g) that any such money judgment be trebled as a result of the willful nature of Defendants' infringement;
- (h) costs and reasonable attorneys' fees incurred in connection with this action pursuant to 35 U.S.C § 285; and
- (i) such other and further relief as this Court finds just and proper.

JURY DEMAND

Plaintiff requests trial by jury.

Dated: June 30, 2005

FISH & RICHARDSON P.C.

By: */s/ John F. Horvath*

William J. Marsden, Jr. (#2247)
Sean P. Hayes (#4413)
John F. Horvath (#4557)
919 N. Market Street, Suite 1100
P.O. Box 1114
Wilmington, DE 19801
Telephone: (302) 652-5070
Facsimile: (302) 652-0607

Frank E. Scherkenbach
225 Franklin Street
Boston, MA 02110-2804
Telephone: (617) 542-5070
Facsimile: (617) 542-8906

Michael Kane
60 South Sixth Street
3300 Dain Rauscher Plaza
Minneapolis, MN 55402
Telephone: (612) 335-5070
Facsimile: (612) 288-9696

Howard G. Pollack
Gina M. Steele
Michael R. Headley
500 Arguello Street, Suite 500
Redwood City, CA 94063
Telephone: (650) 839-5070
Facsimile: (650) 839-5071

Attorneys for Plaintiff
POWER INTEGRATIONS, INC.

*Power Intergrations, Inc. v.
Fairchild Semiconductor International, Inc.*

*Hearing
May 31, 2006*

*Hawkins Reporting Service
715 N King Street
Suite 3
Wilmington, DE 19801
(302) 658-6697*

*Original File 5PWRIN~1.TXT, 52 Pages
Min-U-Script® File ID: 3175811218*

Word Index included with this Min-U-Script®

Page 1

IN THE UNITED STATES DISTRICT COURT
 FOR THE DISTRICT OF DELAWARE
 POWER INTEGRATIONS, INC.,)
 Plaintiff,)

v.)
 FAIRCHILD SEMICONDUCTOR)
 INTERNATIONAL, INC., and)
 FAIRCHILD SEMICONDUCTOR)
 CORPORATION,)

Defendants.)
 United States District Court
 844 King Street
 Wilmington, Delaware
 Wednesday, May 31, 2006
 12:30 p.m.

BEFORE: THE HONORABLE JOSEPH J. FARNAN, JR.

United States District Court Judge

APPEARANCES:

SEAN P. HAYES, ESQ.
 FRANK SCHERKENBACH, ESQ.
 MICHAEL HEADLEY, ESQ.
 FISH & RICHARDSON
 For Power Integrations
 G. HOPKINS GUY, ESQ.
 ORRICLE, HERRINGTON

and
 BAS DE BLANK, ESQ.
 JOHN G. DAY, ESQ.
 ASHBY & GEDDES
 For Fairchild

Hawkins Reporting Service

715 North King Street - Wilmington, Delaware 19801
 (302)658-6697 FAX(302)658-8418

Page 2

(302)658-6697 FAX(302)658-8418

3 1 THE COURT: Be seated, please.

[2] Good afternoon.

[3] (All respond: "Good afternoon.")

[4] THE COURT: I've reviewed the [5] proposed pretrial order, and this afternoon [6] I'll be entering an order that essentially [7] denies the motions for summary judgment and [8] also grants partial summary judgment to [9] Fairchild with regard to the damages evidence.

[10] If there's any questions about that [11] after you read it, you could write me a letter [12] and we'll try to explain essentially what it [13] boils down to, the discovery ruling and then [14] the setting of a date.

[15] With regard to the pretrial order, [16] I sound like a broken record sometimes at these [17] conferences, but you list witnesses, for [18] instance, on behalf of Power Integrations, you [19] have like seven people that you say are going [20] to testify and then there's a list that is a [21] little more extensive and there's the cryptic [22] statement that these folks may be called in [23] rebuttal, they may come to Wilmington for [24] lunch, I don't know what they're doing in the

Page 4

[1] pretrial order, but, you know, you got to [2] pretry the case.

[3] So what has to happen is both sides [4] have to — and it's important for the [5] allocation of time, you have to tell me who the [6] witnesses are going to be and

then I can make [7] decisions about whether there's too many, [8] they're accumulative, there's some question [9] about the offer of their testimony. But I need [10] to know exactly who the witnesses are going to [11] be and it would seem not illogical that they [12] would be — that they'd be listed in the order [13] you intend to call them and a little bit about [14] what they're going to say.

[15] There's no surprises in this case, [16] so there's no rebuttal witnesses, other than a [17] planned rebuttal witness to an answer, and I [18] call that more of an answering witness but it's [19] fairly characterized as a rebuttal witness. [20] But we would know who they are and it's just a [21] question of putting it on logically and [22] consistent with the order of proof so the jury [23] gets, well, this is what they said with the [24] burden and this is what they answered and this [25] (302)658-6697 FAX(302)658-8418

Page 5

[1] is our rebuttal or answer to that, but that has [2] to be set out.

[3] And then you know exhibits would be [4] — there's a certain volume of exhibits in a [5] patent case that I allow to come in just for [6] the record because you think you might need it [7] later on but they never get shown to the jury [8] and they're part of the pretrial order and [9] admitted in the record. But I really need to [10] know exactly the — and I never put lawyers to [11] this test, but, you know, sometimes you can [12] actually tell us with what witnesses they're [13] coming in and who's testifying about them but [14] maybe that's too difficult. But at least [15] you'll be able to say exactly what exhibits are [16] going to be presented with testimony before the [17] jury and that gives me some idea of how to make [18] decisions again about time, also about any [19] objections that may be offered. Both of those [20] are going to have to be tightened up in this [21] proposed order. And I guess depending on when [22] we pick a trial date I'll give you an amount of [23] time to get that done.

[24] With regard to the case, the

[25] (302)658-6697 FAX(302)658-8418

Page 6

[1] validity case, the invalidity case, I'm [2] seriously thinking about separating that from [3] infringement and damages. And without knowing [4] something that would be prejudicial or unduly [5] prejudicial, I'm inclined to do that.

[6] MR. GUY: If I may be heard on [7] that, Your Honor?

[8] THE COURT: Yes.

[9] MR. SPEAKER: We have suggested [10] bifurcation — Fairchild has sug-

gested. What [11] we would like to do there is because of some [12] issues that are ongoing right now with respect [13] to damages, we still have a number of [14] depositions to take. The experts have not been [15] deposed, the two damages experts. We need to [16] propound or provide a 30(B)6 deposition on U.S. [17] manufacturing, should be a limited deposition.

[18] Also, there has been an undisclosed [19] expert that — or unnamed expert that is [20] provided, expert reports in end of April, early [21] May, so that would tend to move that issue of [22] damages, all the damages related issues out.

[23] The other point though is that the [24] damages experts, particularly the plaintiff's

[25] (302)658-6697 FAX(302)658-8418

Page 7

[1] damages experts, relies upon Power Integrations [2] financial statements, their filings, annual [3] reports, and quarterly reports with the SCC.

[4] There is currently an ongoing [5] investigation apparently going on at Power [6] Integrations. They have not filed their 2005 [7] annual reports. They have notified the SCC [8] that all prior reports are unreliable. I want [9] to make that clear that all prior SCC reports, [10] annual reports, quarterly reports going back to [11] 1999 are unreliable. They'll need to be [12] restated. And in addition, Your Honor, they [13] expect to have those — according to the [14] information we have and it's not subject to [15] discovery, but they would have that information [16] to NASDAQ by August the 2nd. I don't know [17] whether they'll meet that or not.

[18] They have been up in front of the [19] NASDAQ board twice on delisting issues [20] regarding their failure to provide these [21] reports. So this is a fundamental issue that's [22] going on. The damages experts have relied upon [23] these. It relates to back dating of stock [24] options. It's our understanding that both the

[25] (302)658-6697 FAX(302)658-8418

Page 8

[1] chairman and the chief financial officer have [2] been fired related to this issue. We know that [3] they've resigned and left the company at the [4] same time this was going on. So this is a [5] material issue and, again, it all relates to [6] damages and I'd ask the Court to consider that [7] in terms of bifurcation in terms of pushing the [8] damages component off.

[9] Thank you, Your Honor.

[10] THE COURT: Thank you.

[11] MR. SCHERKENBACH: I didn't hear

[12] any substantive argument as to why the [13] issues couldn't be divided in the way you [14] suggest. I'm perfectly happy with that. It [15] makes quite a bit of sense to do it. So [16] infringement and damages in one trial, validity [17] in other. [18] I don't know if Your Honor has in [19] mind the same jury or different juries. I [20] might have some concerns if we're talking about [21] different juries or if there is a substantial [22] subrogation but I suppose we could talk about [23] that. [24] To respond to Mr. Guy's point, the [25] (302)658-6697 FAX(302)658-8418

Page 9

[1] further discovery is minor. The two damages [2] experts need to be deposed. We've been trying [3] to schedule that for some time. That will [4] happen shortly. [5] The witness Mr. Guy referred to [6] relating to Manufacturing, you may have seen [7] this, Your Honor, in the pretrial papers, but [8] there had been an issue in the case about the [9] extent to which Fairchild manufactured the [10] accused products in the U.S. Fairchild is [11] saying essentially they never did that and [12] Power Integrations is a little skeptical. [13] It turns out Mr. Kim, the elusive [14] Mr. Kim whose deposition we finally got, you [15] may recall you ordered that. He said, well, [16] actually, in fact, they did manufacture in the [17] U.S. This just came out in the last several [18] weeks. We were surprised because we've been [19] told the contrary. And Fairchild then went [20] back to the drawing board, investigated it and [21] said, yes, it turns out that several million of [22] the accused parts have in fact been [23] manufactured in the U.S. [24] So we agreed that as a result of [25] (302)658-6697 FAX(302)658-8418

Page 10

[1] that we now get at least one further deposition [2] on the extent to which the U.S. manufacturing [3] actually occurred. It's one deposition. There [4] will be some additional, I think, document [5] discovery that's required but it's not the sort [6] of thing that's going to cause any sort of [7] significant delay. [8] The financial statement point, if I [9] can comment on that. There's some truth [10] certainly what Mr. Guy is saying. On the other [11] hand, with all due respect, in our view is a [12] sideshow. It doesn't have anything to do with [13] the damages information that's relevant to this [14] case. [15] Yes, there are some SCC statements [16] and filings that are going to be revised. The [17] portions that the SCC filings were relied on by [18] either expert have nothing to do with stock [19] options, date of grants, so forth. That's [20]

really just a sideshow and shouldn't derail [21] what the scope is in the case. [22] **MR. GUY:** Your Honor, first of all [23] with respect to the U.S. manufacturing issue, [24] we were unaware that this was going on and what [25] (302)658-6697 FAX(302)658-8418

Page 11

[1] happened in that case is approximately single [2] digit percentage, five percent or so, certain [3] parts, one part in particular was manufactured [4] in the U.S. very, very briefly. [5] Mr. Kim's testimony was he did not [6] know whether there was U.S. manufacturing or [7] not; however, a document was produced during [8] that deposition and that's what triggered the [9] investigation. [10] With respect to the issue about the [11] stock option and issues like that, it has to do [12] with what their true expenses are. It has to [13] do with what their true costs in the case are [14] and they're claiming huge loss profits and huge [15] price erosion claims here basically over a [16] rather minor amount of U.S. sales. [17] Even if you take their numbers, I [18] think they say that 23 percent of our product [19] comes into the United State, and this is about [20] \$27 million worth of worldwide, so we're [21] talking about maybe \$6 million in the U.S. and [22] yet their damages claim is \$45 million to be [23] trebled to total some \$135 million. [24] **THE COURT:** So the damages claim, I [25] (302)658-6697 FAX(302)658-8418

Page 12

[1] thought I read, was like 5 or 6 million in lost [2] profits and then there was this price erosion [3] claim in twenties of million. [4] **MR. GUY:** Yes. [5] **THE COURT:** How does it get to 45 [6] million? Does that add up to something more? [7] **MR. GUY:** Yes, if you add it all up [8] it ends up being — the last page under Tab 2 [9] there's 5.9 million lost profits, lost profits, [10] damages and price erosion is 29, almost 30 [11] million, and reasonable royalty is another 6 [12] million. [13] **THE COURT:** Okay. [14] **MR. GUY:** So that's about 40 [15] million. [16] **THE COURT:** I was leaving out the [17] reasonable royalty because that wasn't [18] implicated in your argument about the relevance [19] of the cost factor of whatever is going on with [20] the filings. [21] **MR. GUY:** I think it does in terms [22] of a hypothetical negotiation about what a [23] reasonable buyer and reasonable seller would [24] come to about what

their true profit is. I [25] (302)658-6697 FAX(302)658-8418

Page 13

[1] think it would be relevant to that even for [2] reasonable royalty. Assuming that's correct, [3] we still have \$36 million in lost profits and [4] price erosion and their financial statements [5] clearly depend upon that. That's what they [6] are. They report their profit a loss. [7] With all due respect to [8] Mr. Scherkenbach, he can't stand up here and [9] tell you what the restatement will be, how much [10] will the amounts vary. All we know are the two [11] key members of Power Integrations have been [12] fired over this and that they have filed [13] statements with the SCC saying that it's going [14] to be material. [15] **THE COURT:** You're from a large [16] firm. This is 2006. This is corporate [17] America. [18] **MR. GUY:** Yes. [19] **THE COURT:** I don't mean to [20] belittle it, but a couple executives get fired, [21] a few restatements, a few false filings, I [22] mean, you know, I don't even know anymore. [23] **MR. GUY:** Your Honor, that's [24] exactly right and neither do we and nor does [25] (302)658-6697 FAX(302)658-8418

Page 14

[1] Mr. Scherkenbach. [2] **THE COURT:** I don't know if that's [3] real important stuff anymore. I used to be a [4] prosecutor. I thought I understood what crime [5] was. I really did. I thought I had a handle [6] on it for about 20 years. I'm not sure I [7] understand what crime is anymore. You can rape [8] somebody and go to jail for three years, and [9] I'm not belittling it, but if you steal a few [10] million you get 25 years. I'm not working the [11] numbers well. I'm glad I'm getting out of this [12] profession soon. [13] **MR. SCHERKENBACH:** Don't say that. [14] **THE COURT:** I shouldn't be glad I'm [15] getting out? [16] **MR. SCHERKENBACH:** No, don't say [17] you're getting out of this profession. [18] **THE COURT:** I'm going to take up [19] boating. Everybody is real nice. They help [20] you. [21] **MR. SCHERKENBACH:** Judge Maher used [22] to say he was going to take up mullet spotting. [23] (Brief discussion off the record.) [24] **THE COURT:** But I understand what [25] (302)658-6697 FAX(302)658-8418

Page 15

[1] you're saying and I'm going to give you a [2] chance to get some information, but like, you [3] know, damages are an important issue here and [4] I want you to have as good a handle on what [5] evidence is available.

[6] I'm one that's not going to be too [7] persuaded by a lot of what goes on in corporate [8] governs. I'm interested in damages would be [9] the second route because you can't get to [10] damages unless you have a verdict on [11] infringement, so that's important.

[12] And then if you have a verdict on [13] infringement, it's important to know whether [14] the patents are valid. That's the way I kind [15] of look at things. I don't see any crime going [16] on in infringement invalidity, unless I live [17] another year maybe I will. Because I feel bad [18] for you lawyers and what they're doing with the [19] patent and trademark office.

[20] Anyway, let me say this, I'm going [21] to give you a chance. I think what you're [22] really asking me, Judge, can you hold off. [23] Because I'm not going to try this case in the [24] summer anyway. I have two other patent cases.

[25] (302)658-6697 FAX(302)658-8418

Page 16

[1] You're looking at a fall trial date so we have [2] some time.

[3] But I do want you to tell me — let [4] me tell you my thought about separation of [5] issues rather than bifurcation. I'm willing to [6] separate issues because I have concerns in [7] patent trials, having done a number of them, [8] that there's a lot of overlapping evidence that [9] becomes prejudicial, unduly prejudicial. I've [10] convinced myself, which is pretty easy to do [11] when you talk to yourself, that it's important [12] that if you separate infringement invalidity [13] that they ought to have a different jury. And [14] the first injury ought to hear about [15] infringement and possibly damages.

[16] The second jury ought to hear that [17] the person accusing the patent of being invalid [18] has been found to infringe. That's all they [19] need to know. These defendants were found to [20] infringe and they claim that the patents are [21] invalid, so you're going to get to decide [22] whether the patents are invalid. And, again, [23] in my mind I've reasoned that that's a real [24] fair way to try a patent case.

[25] (302)658-6697 FAX(302)658-8418

Page 17

[1] Now, there's obviously issues on [2] both sides they'd rather have some sort of [3] overlap, maybe and maybe not. But the real [4] issue I focus on is whether or not it violates [5] the Seventh Amen-

dment about jury trials. [6] Federal circuit doesn't seem to have the [7] stomach to take that issue up. But they have [8] said that separation of issues is not a bad [9] thing from when Chief Judge Maher was there [10] he's kind of like when he wrote early on and [11] others have what they've written is that they [12] think it's a good idea.

[13] And so the only issues I can focus [14] on is whether or not a second jury violates [15] lays someone jury trial right. I guess as long [16] as it's still a jury how can it do that? [17] I haven't been able to find a way or heard a good [18] argument that it does.

[19] So let me say this, in your case [20] you got to work on your witness list. You got [21] to work on your exhibit list. So it's really a [22] pretried case. You have to understand you're [23] going to have separation of issues. I'm [24] inclined strongly toward infringement and

[25] (302)658-6697 FAX(302)658-8418

Page 18

[1] damages and then validity. And I'm inclined to [2] two separate juries with some spread of time [3] between the infringement and damages verdict. [4] Of course if it's four defendants then you [5] don't try the validity because you don't go [6] after a patent that you don't infringe. But if [7] there is infringement, then we would have the [8] validity case maybe in a month or so after [9] that.

[10] And, again, let me make this clear, [11] I don't do that so that there's pressure on [12] people to settle. I don't worry about [13] settlement. I just do it because it gives you [14] time to think about your case and get ready and [15] you're not coming right off the trial on the [16] first set of issues. So then we would have [17] that second trial.

[18] Now, I'm willing to listen to [19] anything you want to tell me about — you [20] obviously think that damages ought to be put [21] off even further, as I understand it.

[22] **MR. GUY:** Yes, Your Honor. At [23] least until the numbers are set. I understand [24] your point about crime. I understand the

[25] (302)658-6697 FAX(302)658-8418

Page 19

[1] issue. But the point being here is that all we [2] know is the numbers that both experts have [3] relied upon are unreliable and we need to know [4] what those numbers are. And hopefully we'll [5] have it by August, but at the same time —

[6] **THE COURT:** You said August 2. [7] We're thinking about a fall trial.

[8] **MR. GUY:** We need to talk about a [9] trial date, if you're talking October, [10] November, I think it would be plenty of time [11] but I understand there may be

conflicts.

[12] **MR. SCHERKENBACH:** Your Honor, on [13] this financial point, you've indicated that [14] you're inclined to give them some further [15] discovery. I guess we can live with that. I'm [16] frankly disappointed in it because what they [17] want to do is have a fifth day of depositions [18] with my CEO who they've had for four days.

[19] You may remember there was a [20] dispute over the fourth day. But it's a [21] sideshow. If we have to do that to stay on [22] track here we're willing to do it.

[23] **THE COURT:** I'm inclined, based on [24] what I'm being told today, if the supplemental

[25] (302)658-6697 FAX(302)658-8418

Page 20

[1] filings or substitute filings are about matters [2] that are different than are being argued here [3] today and you can demonstrate they're just [4] nothing relevant to what's going on in this [5] trial I may not be inclined.

[6] **MR. SCHERKENBACH:** I appreciate [7] that clarification. I think we at least will [8] be able to make that showing and we'd like an [9] opportunity to do it. It's stock option [10] related. It's non-operating expense. It has [11] nothing to do with the operating profit. It [12] doesn't affect the revenues. It doesn't affect [13] the cost of manufacturing or other costs.

[14] So the thing that the patent [15] damages experts rely on are not going to change [16] a bit as a result of this and we'll be able to [17] show that to you.

[18] In terms of separating the issues, [19] just to respond to your proposal, infringement [20] and damages in one trial to one jury, validity [21] to a later jury. I'll be able to accept that [22] on behalf of Power Integrations. I'm not going [23] to make a Seventh Amendment argument. I [24] understand one probably could be made, but

[25] (302)658-6697 FAX(302)658-8418

Page 21

[1] we're not going to get an answer to that anyway [2] in time to matter.

[3] I think as long as the second jury [4] though is told that what the outcome — without [5] embellishment of what the outcome in the first [6] case was, I think that's important.

[7] **THE COURT:** When I've done it I [8] have the jury understand that there has been an [9] infringement finding but nothing else. We [10] don't talk about the damages award if there is [11] one. We just say there's been an infringement [12] finding but under the law now there's a [13] challenge to the validity of the patent

that's [14] been found to infringe. It puts it real nicely [15] before the jury. They understand that. But it [16] gives you eight new people who hear the [17] validity fresh so there's not any prejudice to [18] the presentation of either sides validity case.

[19] **MR. SCHERKENBACH:** And, again, I [20] can accept that on behalf of my client. I've [21] been through that before with Judge Robinson. [22] I thought it worked reasonably well. Despite [23] what defendants tend to think, it tends to be [24] pretty fair.

[25] (302)658-6697 FAX(302)658-8418

Page 22

[1] My major concern is drawing it out. [2] You mentioned fall, that's great. I'm very [3] much hoping we can get September for the first [4] trial, some time in September, and a delay of [5] maybe no longer then until December or so for [6] the second one. We don't want to drag it out.

[7] **THE COURT:** I was thinking I can [8] sort of give you a range.

[9] **MR. SCHERKENBACH:** That would be [10] great.

[11] **THE COURT:** And I want to give you [12] some dates to revise, what I need revised and [13] presented. Let me go to my manually electronic [14] calendar here.

[15] September has been eaten up by [16] Lucent versus Extreme. They're back for a [17] retrial. I have to hear them. That's a [18] retrial. I granted a motion for a new trial [19] and we set that date a long time ago, so [20] there's really difficulty in getting in [21] September.

[22] However, October, the early part of [23] October is available.

[24] **MR. GUY:** That's fine with us, Your

[25] (302)658-6697 FAX(302)658-8418

Page 23

[1] Honor.

[2] **MR. SCHERKENBACH:** My wife is going [3] to kill me. We're expecting our third on the [4] 8th. I was hoping I could avoid a direct train [5] wreck.

[6] I, also, I'm in trial with Judge [7] Robinson the beginning 30th of October for [8] three weeks, so if we could work around that, [9] maybe start a little after the eight and [10] continue it in that way. I don't actually have [11] the days of the week. Actually, here I do. [12] Okay.

[13] **THE COURT:** I'll tell you what's [14] going on in October. The week of October 2nd [15] — and I don't want you here if your wife is [16] giving birth to your third child on October [17] 8th, so they're the two blank weeks I have in [18] October. Starting the week of October 16th [19] Affymetrix wants to sue Illum-

ina, and Sun Power [20] Company from Puerto Rico wants to sue another [21] power company and they're double scheduled to [22] share the trial day.

[23] And then the week of the 23rd of [24] October, a company called Trilogen wants to

[25] (302)658-6697 FAX(302)658-8418

Page 24

[1] sues Martese for patent infringement and they'd [2] like to be here for seven days.

[3] So other than those first two weeks [4] that sort of eats up October. But we could go [5] to the week — the first week of November, [6] which is actually — it's available and then we [7] could go thirty days later in December.

[8] Now, remember, when there's [9] separation of issues you don't need as much [10] trial time as you needed if you have everything [11] together, obviously. You could go the week of [12] December 4th. So you could have the week of [13] November 6th and then the week of December 4th. [14] It my run in to the following week on either [15] scheduling but that would be fine.

[16] So if those dates work, that would [17] give you enough time to have the August 2nd [18] filing and some discovery if it's ordered [19] and —

[20] **MR. GUY:** Your Honor, my [21] understanding then we'd only have one week to [22] do damages and infringement?

[23] **THE COURT:** Well, maybe only three [24] days.

[25] (302)658-6697 FAX(302)658-8418

Page 25

[1] No, I didn't want you to grab your [2] chest.

[3] **MR. GUY:** I do workout. It's not [4] too dangerous to hear things like that.

[5] **THE COURT:** Typically here [6] infringement, validity and damages you get ten [7] trial days. That's why we're able to try as [8] many cases we do. If we gave everybody what [9] they wanted, we'd never do what we do.

[10] Actually, the week of November 6th. [11] What I was saying is I have the ability to go [12] in to the next week if you eat up more than [13] let's say five or six days. We can do that on [14] the infringement, damages. And, again, on the [15] December date I can go in to next week. But I [16] can't allocate time until I actually see a good [17] pretrial order and a number of witness and I [18] can measure how much time I'm going to give [19] each witness based on what they're going to [20] say.

[21] So the answer is don't be nervous [22] about that. I'm only saying that's the week [23] we'll start. There's enough time

to get seven [24] days if we need it.

[25] (302)658-6697 FAX(302)658-8418

Page 26

[1] **MR. SCHERKENBACH:** I have a mark-
man [2] hearing that's already scheduled on November [3] 15th.

[4] **THE COURT:** You'll be out of here by [5] November 15th, I'll guarantee it, unless the [6] jury is deliberating. There's no way you would [7] be here on infringement and damages November [8] 15th.

[9] **MR. GUY:** We need to raise one [10] other issue, Your Honor, and that has to do [11] with some jury insufficiency in the pretrial [12] order, Power Integrations disclosure. There [13] are 38 products that are accused of infringing [14] 18 claims. And just to March through that, [15] Your Honor, I think — and just 18 claims, Your [16] Honor, in three days is huge.

[17] **THE COURT:** Mr. Scherkenbach has [18] been here before. He knows we're not going to [19] have 38 products.

[20] **MR. GUY:** Well, there are four [21] groups of product, Your Honor, that statements [22] at face value isn't very helpful. We will pair [23] down the number of claims further.

[24] **THE COURT:** The claims are going to [25] (302)658-6697 FAX(302)658-8418

Page 27

[1] be paired down.

[2] **MR. GUY:** The claims will be paired [3] down. The products we'll break down in to only [4] three or four groups. 38 is not a real [5] meaningful number. I'm not prepared to say [6] we'll drop whole groups of products. I think [7] the case can easily be tried in groups, in [8] fact, the experts on both sides have dealt with [9] them in that way, so it's not a real —

[10] **THE COURT:** Four categories of [11] products are different than 38 products. 18 [12] claims is 18 claims. That has to be cut back [13] which you're acknowledging.

[14] **MR. GUY:** Absolutely. We have four [15] patents so it works out one per — I think one [16] of them you only have two claims that's [17] asserted. If we're pairing it back to one [18] claim per patent, that would certainly make it [19] doable. But still these technologies are [20] different. Even though three of them are [21] circuit patents, they do different things. So [22] it is important we recognize that what we're [23] asking the jury to do is to consider at least [24] 16 different permutations of four product

[25] (302)658-6697 FAX(302)658-8418

Page 28

[1] groups versus at least four patent

claims and [2] four different patent. So I'm anxious to see [3] how it's going to be paired down and I think we [4] can have a meaningful understanding in a more [5] thorough pretrial conference state once we know [6] that.

[7] **THE COURT:** You know, there's no [8] order prohibiting both of you from talking [9] about that.

[10] **MR. GUY:** We have asked, Your [11] Honor.

[12] **THE COURT:** Well, it's, you know, [13] actually having a discussion about what might [14] be reasonable and then if you have dispute [15] bring it to me. But here's what I'm — I'm not [16] discussing that today because I recognize that [17] there's some ugliness in other parts of [18] pretrial order, but usually what sets the tone [19] is who's going to be the witness and what [20] they're going to testify about and what [21] exhibits you're going to use.

[22] When I get done addressing those [23] two categories of the pretrial order, I think a [24] little more will become apparent, a little more

[25] (302)658-6697 FAX(302)658-8418

Page 29

[1] of what you have to do will become apparent. [2] If you haven't gotten it done by addressing [3] witnesses and the exhibits.

[4] And when you address witness [5] exhibits they should be addressed in the [6] present understanding of infringement, damages [7] and invalidity. And that should go a long way [8] in pairing down. And you should have [9] discussion with each other, and then if you [10] can't agree then I may have to weigh in.

[11] **MR. SCHERKENBACH:** Can I go back to [12] scheduling for a moment?

[13] **THE COURT:** Yes, you can.

[14] **MR. SCHERKENBACH:** People seem to [15] get a little bit interest in November. That is [16] when I'm in trial if front of Judge Robinson, [17] so October 30 to November 24th. I think that [18] case is highly likely to go. What I would [19] request is that we take the first week of [20] October.

[21] **THE COURT:** You're in a four week [22] trial?

[23] **MR. SCHERKENBACH:** It's two [24] defendants, multiple patents. I think that [25] (302)658-6697 FAX(302)658-8418

Page 30

[1] will be paired back to probably two weeks at [2] the end of the day. Judge Robinson did [3] bifurcate damages. Nonetheless, the first two [4] weeks in November won't work for me. I'd be [5] happy to take the first week of October

because [6] I don't believe damages and infringement will [7] take more than five trial days by anyone's [8] stretch of the imagination and then we can [9] perhaps take the first week in December for [10] validity trial if necessary. That would work.

[11] **MR. GUY:** That's fine with me, Your [12] Honor, as long as we have the ability to [13] overflow into the second week of October if [14] need be.

[15] **MR. SCHERKENBACH:** I think that's [16] fine. Once Your Honor sees the revised [17] pretrial you can make that decision as to [18] whether it requires that much trial time. I [19] don't believe it will.

[20] **THE COURT:** All right. October [21] 2nd, for present purposes, will be the [22] commencement of — Monday, October 2nd will be [23] the commencement of infringement and damages, [24] and December the 4th will be the commencement

[25] (302)658-6697 FAX(302)658-8418

Page 31

[1] of invalidity.

[2] And both sides understand that [3] there will be time allocations set, which I [4] don't know what they'll be yet because I don't [5] know what the witness list looks like or the [6] exhibit list.

[7] **MR. GUY:** We also have an issue of [8] inequitable conduct in this case. That will be [9] tried during the invalidity section?

[10] **THE COURT:** I don't send that, for [11] any purpose, to the jury. I'll listen to the [12] evidence and then I'll issue a decision post [13] trial.

[14] And if you need to present a [15] witness outside of what's presented to the [16] jury, I'll spend the time to hear that one or [17] two witnesses after the jury section is over [18] some day or at a day after the jury evidence is [19] complete.

[20] **MR. SCHERKENBACH:** Very good.

[21] **THE COURT:** Here's what I'm going [22] to do, I'm going to set a second pretrial [23] conference and a date to submit a revised [24] pretrial order along the lines that I've

[25] (302)658-6697 FAX(302)658-8418

Page 32

[1] indicated here.

[2] The second pretrial order will be [3] due Friday, September 1, and then the second [4] pretrial conference — what are your schedules [5] looking like in September? Do you want to come [6] a couple weeks before the trial?

[7] **MR. SCHERKENBACH:** Yes, Your Honor. [8] Fine for Power Integrations really any time in [9] September.

[10] **MR. GUY:** I have a conflict on the [11] 11th, that's it.

[12] **THE COURT:** Okay. So let's see, [13] the 11th — I guess traveling is better in the [14] middle of the week, right, then getting near [15] the end. So do you want to come for the second [16] pretrial conference on either the 13th or the [17] 14th of September?

[18] **MR. GUY:** 14th would be better, [19] Your Honor.

[20] **MR. SCHERKENBACH:** That's fine with [21] me, Your Honor.

[22] **THE COURT:** All right. We'll do it [23] on the 14th of September, which is a Thursday, [24] and we'll do it at I guess 1:30. Does that

[25] (302)658-6697 FAX(302)658-8418

Page 33

[1] work?

[2] **MR. SCHERKENBACH:** Yes, Your Honor.

[3] **MR. GUY:** Your Honor, we have an [4] issue of motions in liminae in the case. Can [5] we take up the hearing on the motion in liminae [6] or briefing schedule for the September 1st [7] date?

[8] **THE COURT:** Yes, you can agree to [9] that. What I typically will do is at the [10] pretrial conference that actually is [11] anticipation of a set trial I will give you my [12] rulings at that pretrial conference. So you [13] should give me enough time to read whatever it [14] is you're going to write before that pretrial [15] conference. So if it's the 14th, you probably [16] should get it here that Monday or the Friday [17] before and then we'll take a look at it and [18] give you the rulings on the pretrial [19] conference.

[20] **MR. GUY:** So, in other words, you [21] would like to have briefing completed by [22] September the 4th, that would be the Monday the [23] week before?

[24] **THE COURT:** No, just the Monday —

[25] (302)658-6697 FAX(302)658-8418

Page 34

[1] **MR. GUY:** The 11th?

[2] **THE COURT:** That would be fine if [3] you got it here by then. You know, it's [4] granted or denied. It doesn't take a lot of [5] effort if you get excellent briefing. The [6] decision is as good as what the argument is, [7] right?

[8] **MR. GUY:** Absolutely.

[9] **THE COURT:** Unless minimally [10] skewed.

[11] **MR. SCHERKENBACH:** Can I ask Your [12] Honor how you're handling the issue of experts [13] beyond the scope of report? Is it the same way [14] you have been in the past?

[15] **THE COURT:** Absolutely.

[16] **MR. SCHERKENBACH:** I think that [17] will help resolve a number of things. [18] **THE COURT:** Right. That's one of [19] my, what is it, we all get 27 great ideas and [20] I'm working on 4,011. That was one of the [21] great ideas. It really works. I've now [22] ordered new trial. It's not good if you play [23] around with the expert report.

[24] You know that practice.

[25] (302)658-6697 FAX(302)658-8418

Page 35

[1] **MR. GUY:** Perhaps I should hear it [2] clearer from you, Your Honor.

[3] **THE COURT:** I'll give it to you [4] straight up here. Everybody argues over expert [5] reports and then the expert gets to trial and [6] of course there's something alleged to be [7] different, some new opinion, some nuance on an [8] opinion, particularly after the other side has [9] taken advantage of the opportunity for [10] deposition under the rule.

[11] My practice is in a trial, a [12] serious trial with a jury, or even in a bench, [13] I guess, but particularly the jury, I don't [14] have time to go back and read the report and [15] make an evidentiary ruling on the expert's [16] testimony, so you have to interpose your [17] objection.

[18] If you think the witness is [19] testifying outside of the report and deposition [20] or if it's just a report of the report, if post [21] trial you maintain that objection and I take a [22] look at it and in fact there is some variance, [23] and I mean "some," it doesn't have to be a lot, [24] something that I think could have affected the

[25] (302)658-6697 FAX(302)658-8418

Page 36

[1] other side to their detriment because it wasn't [2] disclosed, I simply say that there's a mistrial [3] and the other side pays the cost of the first [4] trial and we go to a second trial.

[5] It puts a lot of burden on the [6] attorneys but it's, you know, how can you have [7] experts — I mean discovery. I used to find [8] after trial that in fact the witness deviated [9] substantially and what do you do then? You [10] know, you're kind of interested in keeping the [11] verdict and things like that but it really [12] isn't fair during a trial in my experience, so [13] that's the practice.

[14] **MR. GUY:** Your Honor, both sides [15] filed supplemental expert reports in light of [16] other fact discovery that was ongoing and we [17] still have an issue, certainly if there's a [18] debate 30 days before the trial in which the [19] expert reports are filed by that point, any [20] variance from that is certainly understandable. [21] You're not addressing

issues where there's been [22] an ongoing fact discovery and expert report [23] comes in to supplement?

[24] **THE COURT:** No. You all, as I

[25] (302)658-6697 FAX(302)658-8418

Page 37

[1] understand it, have a little more you want to [2] do. So get it done, pick a date, if you can't [3] pick a date I'll give you one. It will be some [4] time in August.

[5] **MR. SCHERKENBACH:** For damages I [6] think that's fine. This doesn't bear on [7] liability at all?

[8] **THE COURT:** No, liability from what [9] I saw in the proposed pretrial order is clear. [10] So you will get that date. And what you're not [11] allowed to do is to send a letter like a week [12] before trial saying the witness just told me [13] this and I'm going to add this or something. [14] So whatever that date is, that's what you're [15] locked in to as a report and deposition.

[16] **MR. GUY:** Your Honor, just so we're [17] clear, we had an expert who did add additional [18] prior art at a deposition. As long as that's [19] in a report by this cutoff date, that should be [20] okay. We'll certainly make sure that whatever [21] he testified to is actually contained in that [22] report.

[23] **THE COURT:** That's pushing the [24] envelope a little bit because damages, by your

[25] (302)658-6697 FAX(302)658-8418

Page 38

[1] request, has opened up a little bit.

[2] **MR. GUY:** Yes, Your Honor.

[3] **THE COURT:** We have expert dates [4] and I know we all get up every day and have a [5] better idea than we had yesterday, but in [6] litigation we really have to tell the expert [7] that there's a date where you can't think [8] anymore. And I'm trying to say this very [9] simply.

[10] So if a new piece of prior art came [11] in but there's been a cutoff date, they're [12] stuck with that cutoff date. We have to limit [13] the discovery and the opinion offering.

[14] Now, if in this case, because the [15] trial date is some time off, you can both agree [16] that you want to — but I wouldn't let that be [17] an August date on liability. That's too close [18] to the trial date. But if by July or something [19] you want to extent it and you want to [20] supplement reports, get them all cleaned up, [21] but you got to on expert opinion testimony [22] there has to be a date when it ends.

[23] In a medical malpractice case and [24] the guy comes in, the doctor, a surgeon, wants

[25] (302)658-6697 FAX(302)658-8418

Page 39

[1] to talk about an operation he had last week, [2] how are you supposed to prepare for that? At [3] some point — because he learned something. I [4] believe he did. Then they say you can [5] foreclose. You have to foreclose.

[6] **Mr. GUY:** Your Honor, we can [7] certainly set a date this summer in which [8] everything will be final and we have the other [9] discovery to do. I just want to make sure that [10] to the extent the expert has provided testimony [11] on something, that we can make sure it's in, [12] we'll go back and make sure if any supplement [13] report is due we can probably do it by the end [14] of June, first of July and give them plenty of [15] time.

[16] **THE COURT:** Do you have a problem [17] with that?

[18] **MR. SCHERKENBACH:** We do because [19] the deposition has happened. It's done and [20] over with. This is actually one of the motions [21] in liminae. Not that I expect the Court to [22] even look at them at this point, but there's a [23] particular person they have in mind who [24] substantially changed his opinions at

[25] (302)658-6697 FAX(302)658-8418

Page 40

[1] deposition and without supplementing the report [2] and we were told, well, you've had a chance to [3] ask questions, ask him questions at deposition, [4] that's too bad.

[5] So what I'm sure they'd now love to [6] do is have a date in the future that they can [7] put it in a report. I guess we'll depose him [8] again. We object to that. That's over. It's [9] a very limited window to do damages expert [10] reports — discovery, excuse me, reports are [11] done. Finish those, a will bit of clean up and [12] that should be that.

[13] Maybe this is something Your Honor [14] decides in motion in liminae and if we lose we [15] have to go back to the drawing board. We're [16] doing a mock trial next weekend. I need to [17] know what the case looks like, what it's going [18] to be. I think I do on the liability side and [19] we're preparing for trial. I should not have [20] to be redoing liability expert discovery.

[21] **THE COURT:** I'll tell you what that [22] motion in liminae gets you a decision, then [23] you'll know whether you can — see, one of the [24] things, if what I'm hearing is factual, if the

[25] (302)658-6697 FAX(302)658-8418

Page 41

[1] witness changed at the deposition what the [2] opinions of the report were,

that's an [3] egregious violation of the scheduling order [4] because how would you ever prepare for a [5] deposition except from the report, and then [6] when you showed up if there were new opinions [7] that weren't in the report, what would be the [8] sense of a deposition?

[9] **MR. GUY:** Your Honor, he did not [10] change his view in the report originally. What [11] he did was he supplemented with additional [12] prior art and also with an obviousness argument [13] that he provided them with a clear shot at it [14] at the deposition.

[15] **THE COURT:** That's my point. Let's [16] assume he added a piece of prior art and [17] modified his opinion. It's like the surgeon [18] that comes in and says last week I had a [19] cardiac operation, let me tell you what I did. [20] So I go to the deposition, you know, I'm [21] prepared and done and happy, and all of a [22] sudden he starts talking about prior art [23] because it's not in his report, how did I [24] prepare for that? So how did I intelligently

[25] (302)658-6697 FAX(302)658-8418

Page 42

[1] conduct the deposition, which is my opportunity [2] to get further information about the opinions [3] in the report?

[4] **MR. GUY:** They were certainly aware [5] on notice that there was obviousness issue. [6] There was certainly notice on prior art. They [7] certainly had an opportunity and all we wish to [8] do is preserve what is already in a deposition [9] for trial.

[10] **THE COURT:** I'm asking you, we're [11] just having a conversation here, we're not a [12] accusing anybody.

[13] **MR. GUY:** Furthermore —

[14] **THE COURT:** How would I have [15] prepared for that deposition if I didn't know [16] about the new piece of prior art?

[17] **MR. GUY:** You would have gone in [18] and you would have prepared for obviousness. [19] You would have learned about the additional [20] prior art. You would have asked questions [21] related to obviousness.

[22] **THE COURT:** I would have done that?

[23] **MR. GUY:** Furthermore, I forgot [24] this, but it was in part in response to their [25] (302)658-6697 FAX(302)658-8418

Page 43

[1] rebuttal report. So it's a lot more involved [2] in this than just we surprised them. They [3] certainly had an opportunity to cross the [4] expert. They had an opportunity to go in. If [5] they needed more time, they had that, also.

[6] So all we're trying to do is [7] preserve what's in a deposition. It was right [8] after the markman hearing, so it would have [9] been late February or March. So they had ample [10] opportunity. There's no surprise like on a [11] witness stand when someone talks about what [12] they did last week. We have all summer, Your [13] Honor, to address this if there's an issue. We [14] just want to be able to get the evidence in for [15] a validity issue which isn't going to trial [16] until December, so there's ample opportunity [17] here to address this rather than trying to [18] strike some evidence that they feel that they [19] don't like.

[20] I would also add that at least in [21] one instance that where we were aware of the [22] art through one of their experts, so, you know, [23] it does take a little bit of iteration here to [24] get all the evidence in and all the expert

[25] (302)658-6697 FAX(302)658-8418

Page 44

[1] reports right. We certainly will not deviate [2] from the expert reports once they're final. [3] And we can make that final date July.

[4] **THE COURT:** See, there could be a [5] book written, or at least a chapter, that you [6] and I could do in a patent trial treatise. [7] Because my view would be, and I'm not an [8] advocate, is that the deposition is the trial [9] date in the context of the scheduling order for [10] expert discovery. That's the drop dead [11] examination day.

[12] But you have the view of 95 percent [13] of the lawyers that come here, which is [14] understandable because you need some iteration, [15] you need to play a little bit, you got to find [16] out, then they put a rebuttal and I have to [17] respond to that.

[18] But that, in my view, runs [19] completely against all of the rules of [20] procedure. So why did I do a scheduling order [21] and have expert discovery dates? They're like [22] the world ends on those dates. There is no [23] other day. And they're drop dead dates.

[24] So when that witness comes in and [25] (302)658-6697 FAX(302)658-8418

Page 45

[1] has a new piece of prior art, which is the [2] practice, I mean, that's what the lawyers do, [3] then you open up the date.

[4] **MR. GUY:** I understand but I think [5] it's one of degree. We're not talking about we [6] submitted two pieces of prior art.

[7] **THE COURT:** You're getting nervous. [8] Don't get nervous I'm going to foreclose. [9] You're getting nervous. We're just having a [10] conversation about the real world versus Civil [11] Procedure 1 in

law school. There's actually [12] people that think that there are dates that [13] count.

[14] I might let you have this in. I [15] have to see what was said. But how do we get [16] lawyers to understand that they are drop dead [17] dates and there is no iteration beyond that [18] date? I mean, the world ended for purposes of [19] that discovery. And it doesn't matter whether [20] they learned which was until then truly not [21] able to be found by them some new information, [22] how do we package a trial if we keep having 95 [23] percent of the lawyers think that the dates [24] have some sort of elasticity in them, you know,

[25] (302)658-6697 FAX(302)658-8418

Page 46

[1] they can be just pushed a little bit? It's [2] really hard. But we're not going to solve that [3] today.

[4] What's the motion in liminae I got [5] to look at?

[6] **MR. SCHERKENBACH:** No. 2, Your [7] Honor, on Power Integrations list. This is tab [8] 16 the second item.

[9] **THE COURT:** We'll get you a quick [10] answer from Tab 16 on No. 2.

[11] **MR. SCHERKENBACH:** I assume you'd [12] like us to — do you want short letter briefs [13] on this or —

[14] **THE COURT:** Sure. Because the [15] motions are only listed.

[16] **MR. SCHERKENBACH:** Yes, just [17] identifies the issues. So we can get you a [18] short letter brief in say a week.

[19] **THE COURT:** That's fine. And then [20] we'll get you the answer.

[21] **MR. GUY:** Your Honor, would we be [22] also allowed to — they've done much the same [23] and we would like to file a similar motion in [24] liminae on the same issue if they're going to

[25] (302)658-6697 FAX(302)658-8418

Page 47

[1] do it this way.

[2] **THE COURT:** In the legal profession [3] it's always fair to punch back.

[4] **MR. GUY:** Just wanted to make sure.

[5] **THE COURT:** Sure.

[6] **MR. SCHERKENBACH:** Which one is [7] that, Mr. Guy?

[8] **THE COURT:** How would we maintain [9] the adversary system if we didn't punch back? [10] It would just collapse. We'd have lawyers with [11] low blood pressure or something.

[12] Which one do you want to punch back [13] with?

[14] **MR. GUY:** Under our Tab 17.

[15] **THE COURT:** This is the limit now. [16]

This is dropping dead. I'm not going to look [17] at any others.

[18] **MR. GUY:** In terms of?

[19] **THE COURT:** In terms of opening up [20] any kind of expert discovery beyond the damages [21] that you've argued you can't get done because [22] of the August 2 filings, anticipate filing.

[23] **MR. GUY:** In our motions in [24] liminae —

[25] (302)658-6697 FAX(302)658-8418

Page 48

[1] **MR. SCHERKENBACH:** And I don't [2] believe Your Honor to raise one that relates to [3] this issue.

[4] **THE COURT:** Let them look at my [5] filing. Give them a chance.

[6] **MR. GUY:** The first one is defense [7] motion in liminae, motion to exclude untimely [8] reports in an undisclosed expert.

[9] **THE COURT:** They got you pretty [10] good there, Scherk.

[11] **MR. SCHERKENBACH:** The expert. If [12] that's the one you want, that's great. No. 1, [13] fine.

[14] **MR. GUY:** Motion with respect to [15] their expert, Troxel, I believe all of those [16] deal with there is an untimely report there as [17] well. I think it's item No. 3 under 2.

[18] **THE COURT:** No. 1, 2. Item No. 3.

[19] **MR. SCHERKENBACH:** I don't think [20] we're talking about damages related stuff. [21] This is liability.

[22] **THE COURT:** If you throw damages in [23] there, you get a yellow flag for piling on.

[24] **MR. GUY:** That was the damage

[25] (302)658-6697 FAX(302)658-8418

Page 49

[1] expert, Your Honor, so we're going to preserve [2] those.

[3] **THE COURT:** We've already said [4] that's a different category. We're going to [5] wait until after August 2 to let you have at [6] each other on damages. This is only liability, [7] that be the context of infringement, validity, [8] expert reports.

[9] All right, your time up. It's a [10] game clock. So you have No. 1, Tab 17 and [11] there's No. 2, Tab 16, and we'll get letters [12] and you'll agree to that schedule for about a [13] week to get them in here and we'll give you [14] expeditious decision so you know where you are.

[15] **MR. SCHERKENBACH:** Thank you, Your [16] Honor.

[17] **THE COURT:** Okay. I think that's [18] all we can do today. I will expect that the [19] one date I got to give you is let's just make [20] it —

[21] **MR. GUY:** I'm sorry, Your Honor, [22] the first letter brief would be due June 7th; [23] is that right?

[24] **THE COURT:** I'm not getting in to

[25] (302)658-6697 FAX(302)658-8418

Page 50

[1] that. You're going to talk with each other and [2] come up with an exchange schedule.

[3] **MR. SCHERKENBACH:** The date for [4] damages wrap up?

[5] **THE COURT:** We need a date for [6] that. It has to be in August because we'll [7] need a couple weeks before the pretrial for any [8] disputes.

[9] **MR. SCHERKENBACH:** The 4th is a [10] Friday. Does that work?

[11] **MR. GUY:** The quarterly reports [12] don't come out until the 2nd.

[13] **MR. SCHERKENBACH:** Okay, the 11th.

[14] **MR. GUY:** You're going to be able [15] to give us a deposition on any changes in that [16] time? Maybe we should push it to the 18th, [17] Your Honor.

[18] **THE COURT:** That would put it [19] beyond the —

[20] **MR. GUY:** It's August the 18th.

[21] **THE COURT:** Oh, August 18th. [22] August 18th is fine with me.

[23] So August 18th is the damages [24] cutoff.

[25] (302)658-6697 FAX(302)658-8418

Page 51

[1] **MR. SCHERKENBACH:** That would be [2] fine, Your Honor.

[3] **MR. GUY:** Be fine, Your Honor.

[4] **THE COURT:** Okay. We'll put this [5] all in an order and get it entered and then [6] look to see those motions in liminae letters.

[7] **MR. SCHERKENBACH:** Thank you, Your [8] Honor.

[9] **THE COURT:** Thank you. We'll be in [10] recess.

[11] (Court adjourned at 1:32 p.m.)

[12] (302)658-6697 FAX(302)658-8418

Page 52

State of Delaware)
New Castle County)
CERTIFICATE OF REPORTER
I, Stacy L. Vickers, Registered
Professional Reporter and Notary Public, do hereby
certify that the foregoing record is a true and
accurate transcript of my stenographic notes taken
on May 31, 2006, in the above-captioned matter.
IN WITNESS WHEREOF, I have hereunto set my
hand and seal this 14th day of June, 2006, at
Wilmington.
Stacy L. Vickers, RPR
Cert.#: 115-RPR
Hawkins Reporting Service
715 North King Street - Wilmington, Delaware 19801
(302)658-6697 FAX(302)658-8418

Lawyer's Notes

\$

\$135 million 11:23
\$27 million 11:20
\$36 million 13:3
\$45 million 11:22
\$6 million 11:21

1

1 32:3; 45:11; 48:12, 18; 49:10
11th 32:11, 13; 34:1; 50:13
13th 32:16
14th 32:17, 18, 23; 33:15
15th 26:3, 5, 8
16 27:24; 46:8, 10; 49:11
16th 23:18
17 47:14; 49:10
18 26:14, 15; 27:11, 12
18th 50:16, 20, 21, 22, 23
1999 7:11
1:30 32:24
1:32 51:11
1st 33:6

2

2 12:8; 19:6; 46:6, 10; 47:22; 48:17, 18; 49:5, 11
20 14:6
2005 7:6
2006 13:16
23 11:18
23rd 23:23
24th 29:17
25 14:10
27 34:19
29 12:10
2nd 7:16; 23:14; 24:17; 30:21, 22; 50:12

3

3 48:17, 18
30 12:10; 29:17; 36:18
30(B)6 6:16
302)658-6697 4:25; 5:25; 6:25; 7:25; 8:25; 9:25; 10:25; 11:25; 12:25; 13:25; 14:25; 15:25; 16:25; 17:25; 18:25; 19:25; 20:25; 21:25; 22:25; 23:25; 24:25; 25:25; 26:25; 27:25; 28:25; 29:25; 30:25; 31:25; 32:25; 33:25; 34:25; 35:25; 36:25; 37:25; 38:25; 39:25; 40:25; 41:25; 42:25;

43:25; 44:25; 45:25; 46:25; 47:25; 48:25; 49:25; 50:25; 51:12
30th 23:7
38 26:13, 19; 27:4, 11

4

4,011 34:20
40 12:14
45 12:5
4th 24:12, 13; 30:24; 33:22; 50:9

5

5 12:1
5.9 12:9

6

6 12:1, 11
6th 24:13; 25:10

7

7th 49:22

8

8th 23:4, 17

9

95 44:12; 45:22

A

ability 25:11; 30:12
able 5:15; 17:17; 20:8, 16, 21; 25:7; 43:14; 45:21; 50:14
Absolutely 27:14; 34:8, 15
accept 20:21; 21:20
according 7:13
accumulative 4:8
accused 9:10, 22; 26:13
accusing 16:17; 42:12
acknowledging 27:13
actually 5:12; 9:16; 10:3; 23:10, 11; 24:6; 25:10, 16; 28:13; 33:10; 37:21; 39:20; 45:11
add 12:6, 7; 37:13, 17; 43:20
added 41:16
addition 7:12
additional 10:4; 37:17; 41:11; 42:19

address 29:4; 43:13, 17
addressed 29:5
addressing 28:22; 29:2; 36:21
adjourned 51:11
admitted 5:9
advantage 35:9
adversary 47:9
advocate 44:8
affect 20:12, 12
affected 35:24
Affymetrix 23:19
again 5:18; 8:5; 16:22; 18:10; 21:19; 25:14; 40:8
against 44:19
ago 22:19
agree 29:10; 33:8; 38:15; 49:12
agreed 9:24
alleged 35:6
allocate 25:16
allocation 4:5
allocations 31:3
allow 5:5
allowed 37:11; 46:22
almost 12:10
along 31:24
always 47:3
Amendment 17:5; 20:23
America 13:17
amount 5:22; 11:16
amounts 13:10
ample 43:9, 16
annual 7:2, 7, 10
answered 4:24
anticipate 47:22
anticipation 33:11
anxious 28:2
anymore 13:22; 14:3, 7; 38:8
apparent 28:24; 29:1
apparently 7:5
appreciate 20:6
approximately 11:1
April 6:20
argued 20:2; 47:21
argues 35:4
argument 8:12; 12:18; 17:18; 20:23; 34:6; 41:12
around 23:8; 34:23
art 37:18; 38:10; 41:12, 16, 22; 42:6, 16, 20; 43:22; 45:1, 6
asserted 27:17
assume 41:16; 46:11
Assuming 13:2
attorneys 36:6
August 7:16; 19:5, 6; 24:17; 37:4; 38:17; 47:22; 49:5; 50:6, 20, 21, 22, 23
available 15:5; 22:23; 24:6

avoid 23:4
award 21:10
aware 42:4; 43:21

B

back 7:10, 23; 9:20; 22:16; 27:12, 17; 29:11; 30:1; 35:14; 39:12; 40:15; 47:3, 9, 12
bad 15:17; 17:8; 40:4
based 19:23; 25:19
basically 11:15
bear 37:6
become 28:24; 29:1
becomes 16:9
beginning 23:7
behalf 20:22; 21:20
belittle 13:20
belittling 14:9
bench 35:12
better 32:13, 18; 38:5
beyond 34:13; 45:17; 47:20; 50:19
bifurcate 30:3
bifurcation 6:10; 8:7; 16:5
birth 23:16
bit 4:13; 8:15; 20:16; 29:15; 37:24; 38:1; 40:11; 43:23; 44:15; 46:1
blank 23:17
blood 47:11
board 7:19; 9:20; 40:15
boating 14:19
book 44:5
both 4:3; 5:19; 7:24; 17:2; 19:2; 27:8; 28:8; 31:2; 36:14; 38:15
break 27:3
Brief 14:23; 46:18; 49:22
briefing 33:6, 21; 34:5
briefly 11:4
briefs 46:12
bring 28:15
burden 4:24; 36:5
buyer 12:23

C

calendar 22:14
call 4:13, 18
called 23:24
came 9:17; 38:10
can 4:6; 5:11; 10:9; 14:7; 15:22; 17:13, 16; 19:15; 20:3; 21:20; 22:3, 7; 25:13, 15, 18; 27:7; 28:4; 29:11; 13; 30:8, 17; 33:4, 8; 34:11; 36:6; 38:15; 39:4, 6, 11, 13; 40:6, 23; 44:3; 46:1, 17; 49:18

cardiac 41:19
case 4:2, 15; 5:5, 24; 6:1, 1; 9:8; 10:14, 21; 11:1, 13; 15:23; 16:24; 17:19, 22; 18:8, 14; 21:6, 18; 27:7; 29:18; 31:8; 33:4; 38:14, 23; 40:17
cases 15:24; 25:8
categories 27:10; 28:23
category 49:4
cause 10:6
CEO 19:18
certain 5:4; 11:2
certainly 10:10; 27:18; 36:17, 20; 37:20; 39:7; 42:4, 6, 7; 43:3; 44:1
chairman 8:1
challenge 21:13
chance 15:2, 21; 40:2; 48:5
change 20:15; 41:10
changed 39:24; 41:1
changes 50:15
chapter 44:5
characterized 4:19
chest 25:2
chief 8:1; 17:9
child 23:16
circuit 17:6; 27:21
Civil 45:10
claim 11:22, 24; 12:3; 16:20; 27:18
claiming 11:14
claims 11:15; 26:14, 15, 23, 24; 27:2, 12, 12, 16; 28:1
clarification 20:7
clean 40:11
cleaned 38:20
clear 7:9; 18:10; 37:9, 17; 41:13
clearer 35:2
clearly 13:5
client 21:20
clock 49:10
close 38:17
collapse 47:10
coming 5:13; 18:15
commencement 30:22, 23, 24
comment 10:9
company 8:3; 23:20, 21, 24
complete 31:19
completed 33:21
completely 44:19
component 8:8
concern 22:1
concerns 8:20; 16:6
conduct 31:8; 42:1
conference 28:5; 31:23; 32:4, 16; 33:10, 12, 15, 19
conflict 32:10

conflicts 19:11
consider 8:6; 27:23
consistent 4:22
contained 37:21
context 44:9; 49:7
continue 23:10
contrary 9:19
conversation 42:11;
45:10
convinced 16:10
corporate 13:16; 15:7
cost 12:19; 20:13; 36:3
costs 11:13; 20:13
count 45:13
couple 13:20; 32:6; 50:7
course 18:4; 35:6
COURT 6:8; 8:6, 10;
11:24; 12:5, 13, 16; 13:15,
19; 14:2, 14, 18, 24; 19:6,
23; 21:7; 22:7, 11; 23:13;
24:23; 25:5; 26:4, 17, 24;
27:10; 28:7, 12; 29:13, 21;
30:20; 31:10, 21; 32:12,
22; 33:8, 24; 34:2, 9, 15,
18; 35:3; 36:24; 37:8, 23;
38:3; 39:16, 21; 40:21;
41:15; 42:10, 14, 22; 44:4;
45:7; 46:9, 14, 19; 47:2, 5,
8, 15, 19; 48:4, 9, 18, 22;
49:3, 17, 24; 50:5, 18, 21;
51:4, 9, 11
crime 14:4, 7; 15:15;
18:24
cross 43:3
currently 7:4
cut 27:12
cutoff 37:19; 38:11, 12;
50:24

D

damage 48:24
damages 6:3, 13, 15, 22,
22, 24; 7:1, 22; 8:6, 8, 16;
9:1; 10:13; 11:22, 24;
12:10; 15:3, 8, 10; 16:15;
18:1, 3, 20; 20:15, 20;
21:10; 24:22; 25:6, 14;
26:7; 29:6; 30:3, 6, 23;
37:5, 24; 40:9; 47:20;
48:20, 22; 49:6; 50:4, 23
dangerous 25:4
date 5:22; 10:19; 16:1;
19:9; 22:19; 25:15; 31:23;
33:7; 37:2, 3, 10, 14, 19;
38:7, 11, 12, 15, 17, 18,
22; 39:7; 40:6; 44:3, 9;
45:3, 18; 49:19; 50:3, 5
dates 22:12; 24:16; 38:3;
44:21, 22, 23; 45:12, 17,
23
dating 7:23
day 19:17, 20; 23:22;
30:2; 31:18, 18; 38:4;
44:11, 23

days 19:18; 23:11; 24:2,
7, 24; 25:7, 13, 24; 26:16;
30:7; 36:18
dead 44:10, 23; 45:16;
47:16
deal 48:16
dealt 27:8
debate 36:18
December 22:5; 24:7, 12,
13; 25:15; 30:9, 24; 43:16
decide 16:21
decides 40:14
decision 30:17; 31:12;
34:6; 40:22; 49:14
decisions 4:7; 5:18
defendants 16:19; 18:4;
21:23; 29:24
defense 48:6
degree 45:5
delay 10:7; 22:4
deliberating 26:6
delisting 7:19
demonstrate 20:3
denied 34:4
depend 13:5
depending 5:21
depose 40:7
deposed 6:15; 9:2
deposition 6:16, 17;
9:14; 10:1, 3; 11:8; 35:10,
19; 37:15, 18; 39:19; 40:1,
3; 41:1, 5, 8, 14, 20; 42:1,
8, 15; 43:7; 44:8; 50:15
depositions 6:14; 19:17
derail 10:20
Despite 21:22
detriment 36:1
deviate 44:1
deviated 36:8
different 8:19, 21; 16:13;
20:2; 27:11, 20, 21, 24;
28:2; 35:7; 49:4
difficult 5:14
difficulty 22:20
digit 11:2
direct 23:4
disappointed 19:16
disclosed 36:2
disclosure 26:12
discovery 7:15; 9:1;
10:5; 19:15; 24:18; 36:7,
16, 22; 38:13; 39:9; 40:10,
20; 44:10, 21; 45:19; 47:20
discussing 28:16
discussion 14:23; 28:13;
29:9
dispute 19:20; 28:14
disputes 50:8
divided 8:13
doable 27:19
doctor 38:24
document 10:4; 11:7
done 5:23; 16:7; 21:7;

28:22; 29:2; 37:2; 39:19;
40:11; 41:21; 42:22;
46:22; 47:21
double 23:21
down 26:23; 27:1, 3, 3;
28:3; 29:8
drag 22:6
drawing 9:20; 22:1;
40:15
drop 27:6; 44:10, 23;
45:16
dropping 47:16
due 10:11; 13:7; 32:3;
39:13; 49:22
during 11:7; 31:9; 36:12

E

early 6:20; 17:10; 22:22
easily 27:7
easy 16:10
eat 25:12
eaten 22:15
eats 24:4
effort 34:5
egregious 41:3
eight 21:16; 23:9
either 10:18; 21:18;
24:14; 32:16
elasticity 45:24
electronic 22:13
else 21:9
elusive 9:13
embellishment 21:5
end 6:20; 30:2; 32:15;
39:13
ended 45:18
ends 12:8; 38:22; 44:22
enough 24:17; 25:23;
33:13
entered 51:5
envelope 37:24
erosion 11:15; 12:2, 10;
13:4
essentially 9:11
Even 11:17; 13:1, 22;
18:21; 27:20; 35:12; 39:22
Everybody 14:19; 25:8;
35:4
evidence 15:5; 16:8;
31:12, 18; 43:14, 18, 24
evidentiary 35:15
exactly 4:10; 5:10, 15;
13:24
examination 44:11
excellent 34:5
except 41:5
exchange 50:2
exclude 48:7
excuse 40:10
executives 13:20
exhibit 17:21; 31:6

exhibits 5:3, 4, 15; 28:21;
29:3, 5
expect 7:13; 39:21; 49:18
expecting 23:3
expeditious 49:14
expense 20:10
expenses 11:12
experience 36:12
expert 6:19, 19, 20;
10:18; 34:23; 35:4, 5;
36:15, 19, 22; 37:17; 38:3,
6, 21; 39:10; 40:9, 20;
43:4, 24; 44:2, 10, 21;
47:20; 48:8, 11, 15; 49:1, 8
expert's 35:15
experts 6:14, 15, 24; 7:1,
22; 9:2; 19:2; 20:15; 27:8;
34:12; 36:7; 43:22
extent 9:9; 10:2; 38:19;
39:10
Extreme 22:16

F

face 26:22
fact 9:16, 22; 27:8; 35:22;
36:8, 16, 22
factor 12:19
factual 40:24
failure 7:20
fair 16:24; 21:24; 36:12;
47:3
Fairchild 6:10; 9:9, 10, 19
fairly 4:19
fall 16:1; 19:7; 22:2
false 13:21
FAX(302)658-8418 4:25;
5:25; 6:25; 7:25; 8:25;
9:25; 10:25; 11:25; 12:25;
13:25; 14:25; 15:25;
16:25; 17:25; 18:25;
19:25; 20:25; 21:25;
22:25; 23:25; 24:25;
25:25; 26:25; 27:25;
28:25; 29:25; 30:25;
31:25; 32:25; 33:25;
34:25; 35:25; 36:25;
37:25; 38:25; 39:25;
40:25; 41:25; 42:25;
43:25; 44:25; 45:25;
46:25; 47:25; 48:25;
49:25; 50:25; 51:12
February 43:9
Federal 17:6
feel 15:17; 43:18
few 13:21, 21; 14:9
fifth 19:17
file 46:23
filed 7:6; 13:12; 36:15, 19
filing 24:18; 47:22; 48:5
filings 7:2; 10:16, 17;
12:20; 13:21; 20:1, 1;
47:22
final 39:8; 44:2, 3

finally 9:14
financial 7:2; 8:1; 10:8;
13:4; 19:13
find 17:17; 36:7; 44:15
finding 21:9, 12
fine 22:24; 24:15; 30:11,
16; 32:8, 20; 34:2; 37:6;
46:19; 48:13; 50:22; 51:2,
3
Finish 40:11
fired 8:2; 13:12, 20
firm 13:16
first 10:22; 16:14; 18:16;
21:5; 22:3; 24:3, 5; 29:19;
30:3, 5, 9; 36:3; 39:14;
48:6; 49:22
five 11:2; 15:1; 25:13;
30:7
flag 48:23
focus 17:4, 13
following 24:14
foreclose 39:5, 5; 45:8
forgot 42:23
forth 10:19
found 16:18, 19; 21:14;
45:21
four 18:4; 19:18; 26:20;
27:4, 10, 14, 24; 28:1, 2;
29:21
fourth 19:20
frankly 19:16
fresh 21:17
Friday 32:3; 33:16; 50:10
front 7:18; 29:16
fundamental 7:21
further 9:1; 10:1; 18:21;
19:14; 26:23; 42:2
Furthermore 42:13, 23
future 40:6

G

game 49:10
gave 25:8
gets 4:23; 35:5; 40:22
gives 5:17; 18:13; 21:16
giving 23:16
glad 14:11, 14
goes 15:7
good 15:4; 17:12, 17;
25:16; 31:20; 34:6, 22;
48:10
governs 15:8
grab 25:1
granted 22:18; 34:4
grants 10:19
great 22:2, 10; 34:19, 21;
48:12
groups 26:21; 27:4, 6, 7;
28:1
guarantee 26:5
guess 5:21; 17:15; 19:15;
32:13, 24; 35:13; 40:7

GUY 6:6; 9:5; 10:10, 22;
12:4, 7, 14, 21; 13:18, 23;
18:22; 19:8; 22:24; 24:20;
25:3; 26:9, 20; 27:2, 14;
28:10; 30:11; 31:7; 32:10,
18; 33:3, 20; 34:1, 8; 35:1;
36:14; 37:16; 38:2, 24;
39:6; 41:9; 42:4, 13, 17,
23; 45:4; 46:21; 47:4, 7,
14, 18, 23; 48:6, 14, 24;
49:21; 50:11, 14, 20; 51:3
Guy's 8:24

H

hand 10:11
handle 14:5; 15:4
handling 34:12
happen 4:3; 9:4
happened 11:1; 39:19
happy 8:14; 30:5; 41:21
hard 46:2
hear 8:11; 16:14, 16;
21:16; 22:17; 25:4; 31:16;
35:1
heard 6:6; 17:17
hearing 26:2; 33:5;
40:24; 43:8
help 14:19; 34:17
helpful 26:22
here's 28:15; 31:21
highly 29:18
hold 15:22
Honor 6:7; 7:12; 8:9, 18;
9:7; 10:22; 13:23; 18:22;
19:12; 23:1; 24:20; 26:10,
15, 16, 21; 28:11; 30:12,
16; 32:7, 19, 21; 33:2, 3;
34:12; 35:2; 36:14; 37:16;
38:2; 39:6; 40:13; 41:9;
43:13; 46:7, 21; 48:2; 49:1,
16, 21; 50:17; 51:2, 3, 8
hopefully 19:4
hoping 22:3; 23:4
huge 11:14, 14; 26:16
hypothetical 12:22

I

idea 5:17; 17:12; 38:5
ideas 34:19, 21
identifies 46:17
illogical 4:11
Illumina 23:19
imagination 30:8
implicated 12:18
important 4:4; 14:3; 15:3,
11, 13; 16:11; 21:6; 27:22
inclined 6:5; 17:24; 18:1;
19:14, 23; 20:5
indicated 19:13; 32:1
inequitable 31:8
information 7:14, 15;

10:13; 15:2; 42:2; 45:21
infringe 16:18, 20; 18:6;
21:14
infringement 6:3; 8:16;
15:11, 13, 16; 16:12, 15;
17:24; 18:3, 7; 20:19; 21:9,
11; 24:1, 22; 25:6, 14;
26:7; 29:6; 30:6, 23; 49:7
infringing 26:13
injury 16:14
instance 43:21
insufficiency 26:11
Integrations 7:1, 6, 9; 12;
13:11; 20:22; 26:12; 32:8;
46:7
intelligently 41:24
intend 4:13
interest 29:15
interested 15:8; 36:10
interpose 35:16
into 11:19; 30:13
invalid 16:17, 21, 22
invalidity 6:1; 15:16;
16:12; 29:7; 31:1, 9
investigated 9:20
investigation 7:5; 11:9
involved 43:1
issue 6:21; 7:21; 8:2, 5;
9:8; 10:23; 11:10; 15:3;
17:4, 7; 19:1; 26:10; 31:7,
12; 33:4; 34:12; 36:17;
42:5; 43:13, 15; 46:24;
48:3
issues 6:12, 22; 7:19;
8:13; 11:11; 16:5, 6; 17:1,
8, 13, 23; 18:16; 20:18;
24:9; 36:21; 46:17
item 46:8; 48:17, 18
iteration 43:23; 44:14;
45:17

J

jail 14:8
Judge 14:21; 15:22; 17:9;
21:21; 23:6; 29:16; 30:2
July 38:18; 39:14; 44:3
June 39:14; 49:22
juries 8:19, 21; 18:2
jury 4:22; 5:7, 17; 8:19;
16:13, 16; 17:5, 14, 15, 16;
20:20, 21; 21:3, 8, 15;
26:6, 11; 27:23; 31:11, 16,
17, 18; 35:12, 13

K

keep 45:22
keeping 36:10
key 13:11
kill 23:3
Kim 9:13, 14
Kim's 11:5

kind 15:14; 17:10; 36:10;
47:20
knowing 6:3
knows 26:18

L

large 13:15
last 9:17; 12:8; 39:1;
41:18; 43:12
late 43:9
later 5:7; 20:21; 24:7
law 21:12; 45:11
lawyers 5:10; 15:18;
44:13; 45:2, 16, 23; 47:10
lays 17:15
learned 39:3; 42:19;
45:20
least 5:14; 10:1; 18:23;
20:7; 27:23; 28:1; 43:20;
44:5
leaving 12:16
left 8:3
legal 47:2
letter 37:11; 46:12, 18;
49:22
letters 49:11; 51:6
liability 37:7, 8; 38:17;
40:18, 20; 48:21; 49:6
light 36:15
likely 29:18
liminae 33:4, 5; 39:21;
40:14, 22; 46:4, 24; 47:24;
48:7; 51:6
limit 38:12; 47:15
limited 6:17; 40:9
lines 31:24
list 17:20, 21; 31:5, 6;
46:7
listed 4:12; 46:15
listen 18:18; 31:11
litigation 38:6
little 4:13; 9:12; 23:9;
28:24, 24; 29:15; 37:1, 24;
38:1; 43:23; 44:15; 46:1
live 15:16; 19:15
locked 37:15
logically 4:21
long 17:15; 21:3; 22:19;
29:7; 30:12; 37:18
longer 22:5
look 15:15; 33:17; 35:22;
39:22; 46:5; 47:16; 48:4;
51:6
looking 16:1; 32:5
looks 31:5; 40:17
lose 40:14
loss 11:14; 13:6
lost 12:1, 9, 9; 13:3
lot 15:7; 16:8; 34:4; 35:23;
36:5; 43:1
love 40:5
low 47:11

Lucent 22:16

M

Maher 14:21; 17:9
maintain 35:21; 47:8
major 22:1
makes 8:15
malpractice 38:23
manually 22:13
manufacture 9:16
manufactured 9:9, 23;
11:3
manufacturing 6:17;
9:6; 10:2, 23; 11:6; 20:13
many 4:7; 25:8
March 26:14; 43:9
markman 26:1; 43:8
Martese 24:1
material 8:5; 13:14
matter 21:2; 45:19
matters 20:1
may 5:19; 6:6, 21; 9:6, 15;
19:11, 19; 20:5; 29:10
maybe 5:14; 11:21;
15:17; 17:3, 3; 18:8; 22:5;
23:9; 24:23; 40:13; 50:16
mean 13:19, 22; 35:23;
36:7; 45:2, 18
meaningful 27:5; 28:4
measure 25:18
medical 38:23
meet 7:17
members 13:11
mentioned 22:2
middle 32:14
might 5:6; 8:20; 28:13;
45:14
million 9:21; 12:1, 3, 6, 9,
11, 12, 15; 14:10
mind 8:19; 16:23; 39:23
minimally 34:9
minor 9:1; 11:16
mistril 36:2
mock 40:16
modified 41:17
moment 29:12
Monday 30:22; 33:16, 22,
24
month 18:8
more 4:18; 12:6; 25:12;
28:4, 24, 24; 30:7; 37:1;
43:1, 5
motion 22:18; 33:5;
40:14, 22; 46:4, 23; 48:7,
7, 14
motions 33:4; 39:20;
46:15; 47:23; 51:6
move 6:21
much 13:9; 22:3; 24:9;
25:18; 30:18; 46:22
mullet 14:22

multiple 29:24
myself 16:10

N

NASDAQ 7:16, 19
near 32:14
necessary 30:10
need 4:9; 5:6, 9; 6:15;
7:11; 9:2; 16:19; 19:3, 8;
22:12; 24:9; 25:24; 26:9;
30:14; 31:14; 40:16;
44:14, 15; 50:5, 7
needed 24:10; 43:5
negotiation 12:22
neither 13:24
nervous 25:21; 45:7, 8, 9
new 21:16; 22:18; 34:22;
35:7; 38:10; 41:6; 42:16;
45:1, 21
next 25:12, 15; 40:16
nice 14:19
nicely 21:14
Nonetheless 30:3
nonoperating 20:10
nor 13:24
notice 42:5, 6
notified 7:7
November 19:10; 24:5,
13; 25:10; 26:2, 5, 7;
29:15, 17; 30:4
nuance 35:7
number 6:13; 16:7;
25:17; 26:23; 27:5; 34:17
numbers 11:17; 14:11;
18:23; 19:2, 4

O

object 40:8
objection 35:17, 21
objections 5:19
obviously 17:1; 18:20;
24:11
obviousness 41:12;
42:5, 18, 21
occurred 10:3
October 19:9; 22:22, 23;
23:7, 14, 14, 16, 18, 18,
24; 24:4; 29:17, 20; 30:5,
13, 20, 22
off 8:8; 14:23; 15:22;
18:15, 21; 38:15
offer 4:9
offered 5:19
offering 38:13
office 15:19
officer 8:1
once 28:5; 30:16; 44:2
one 8:16; 10:1, 3; 11:3;
15:6; 20:20, 20, 24; 21:11;
22:6; 24:21; 26:9; 27:15,
15, 17; 31:16; 34:18, 20;

37:3; 39:20; 40:23; 43:21,
22; 45:5; 47:6, 12; 48:2, 6,
12; 49:19
ongoing 6:12; 7:4; 36:16,
22
only 17:13; 24:21, 23;
25:22; 27:3, 16; 46:15;
49:6
open 45:3
opened 38:1
opening 47:19
operating 20:11
operation 39:1; 41:19
opinion 35:7, 8; 38:13,
21; 41:17
opinions 39:24; 41:2, 6;
42:2
opportunity 20:9; 35:9;
42:1, 7; 43:3, 4, 10, 16
option 11:11; 20:9
options 7:24; 10:19
order 4:1, 12, 22; 5:8, 21;
25:17; 26:12; 28:8, 18, 23;
31:24; 32:2; 37:9; 41:3;
44:9, 20; 51:5
ordered 9:15; 24:18;
34:22
originally 41:10
others 17:11; 47:17
ought 16:13, 14, 16;
18:20
out 5:2; 6:22; 9:13, 17, 21;
12:16; 14:11, 15, 17; 22:1,
6; 26:4; 27:15; 44:16;
50:12
outcome 21:4, 5
outside 31:15; 35:19
over 11:15; 13:12; 19:20;
31:17; 35:4; 39:20; 40:8
overflow 30:13
overlap 17:3
overlapping 16:8

P

p.m 51:11
package 45:22
page 12:8
pair 26:22
paired 27:1, 2; 28:3; 30:1
pairing 27:17; 29:8
papers 9:7
part 5:8; 11:3; 22:22;
42:24
particular 11:3; 39:23
particularly 6:24; 35:8,
13
parts 9:22; 11:3; 28:17
past 34:14
patent 5:5; 15:19, 24;
16:7, 17, 24; 18:6; 20:14;
21:13; 24:1; 27:18; 28:1, 2;
44:6

patents 15:14; 16:20, 22;
27:15, 21; 29:24
pays 36:3
people 18:12; 21:16;
29:14; 45:12
per 27:15, 18
percent 11:2, 18; 44:12;
45:23
percentage 11:2
perfectly 8:14
perhaps 30:9; 35:1
permutations 27:24
person 16:17; 39:23
persuaded 15:7
pick 5:22; 37:2, 3
piece 38:10; 41:16;
42:16; 45:1
pieces 45:6
piling 48:23
plaintiff's 6:24
planned 4:17
play 34:22; 44:15
plenty 19:10; 39:14
point 6:23; 8:24; 10:8;
18:24; 19:1, 13; 36:19;
39:3, 22; 41:15
portions 10:17
possibly 16:15
post 31:12; 35:20
Power 7:1, 5; 9:12; 13:11;
20:22; 23:19, 21; 26:12;
32:8; 46:7
practice 34:24; 35:11;
36:13; 45:2
prejudice 21:17
prejudicial 6:4, 5; 16:9, 9
prepare 39:2; 41:4, 24
prepared 27:5; 41:21;
42:15, 18
preparing 40:19
present 29:6; 30:21;
31:14
presentation 21:18
presented 5:16; 22:13;
31:15
preserve 42:8; 43:7; 49:1
pressure 18:11; 47:11
pretrial 4:1; 5:8; 9:7;
25:17; 26:11; 28:5, 18, 23;
30:17; 31:22, 24; 32:2, 4,
16; 33:10, 12, 14, 18; 37:9;
50:7
pretried 17:22
pretry 4:2
pretty 16:10; 21:24; 48:9
price 11:15; 12:2, 10;
13:4
prior 7:8, 9; 37:18; 38:10;
41:12, 16, 22; 42:6, 16, 20;
45:1, 6
probably 20:24; 30:1;
33:15; 39:13
problem 39:16

procedure 44:20; 45:11
produced 11:7
product 11:18; 26:21;
27:24
products 9:10; 26:13, 19;
27:3, 6, 11, 11
profession 14:12, 17;
47:2
profit 12:24; 13:6; 20:11
profits 11:14; 12:2, 9, 9;
13:3
prohibiting 28:8
proof 4:22
proposal 20:19
proposed 5:21; 37:9
propound 6:16
prosecutor 14:4
provide 6:16; 7:20
provided 6:20; 39:10;
41:13
Puerto 23:20
punch 47:3, 9, 12
purpose 31:11
purposes 30:21; 45:18
push 50:16
pushed 46:1
pushing 8:7; 37:23
put 5:10; 18:20; 40:7;
44:16; 50:18; 51:4
puts 21:14; 36:5
putting 4:21

Q

quarterly 7:3, 10; 50:11
quick 46:9
quite 8:15

R

raise 26:9; 48:2
range 22:8
rape 14:7
rather 11:16; 16:5; 17:2;
43:17
read 12:1; 33:13; 35:14
ready 18:14
real 14:3, 19; 16:23; 17:3;
21:14; 27:4, 9; 45:10
really 5:9; 10:20; 14:5;
15:22; 17:21; 22:20; 32:8;
34:21; 36:11; 38:6; 46:2
reasonable 12:11, 17,
23, 23; 13:2; 28:14
reasonably 21:22
reasoned 16:23
rebuttal 4:16, 17, 19; 5:1;
43:1; 44:16
recall 9:15
recess 51:10
recognize 27:22; 28:16
record 5:6, 9; 14:23

redoing 40:20
referred 9:5
regard 5:24
regarding 7:20
related 6:22; 8:2; 20:10;
42:21; 48:20
relates 7:23; 8:5; 48:2
relating 9:6
relevance 12:18
relevant 10:13; 13:1;
20:4
relied 7:22; 10:17; 19:3
relies 7:1
rely 20:15
remember 19:19; 24:8
report 13:6; 34:13, 23;
35:14, 19, 20, 20; 36:22;
37:15, 19, 22; 39:13; 40:1,
7; 41:2, 5, 7, 10, 23; 42:3;
43:1; 48:16
reports 6:20; 7:3, 3, 7, 8,
9, 10, 10, 21; 35:5; 36:15,
19; 38:20; 40:10, 10; 44:1,
2; 48:8; 49:8; 50:11
request 29:19; 38:1
required 10:5
requires 30:18
resigned 8:3
resolve 34:17
respect 6:12; 10:11, 23;
11:10; 13:7; 48:14
respond 8:24; 20:19;
44:17
response 42:24
restated 7:12
restatement 13:9
restatements 13:21
result 9:24; 20:16
retiral 22:17, 18
revenues 20:12
revise 22:12
revised 10:16; 22:12;
30:16; 31:23
Rico 23:20
right 6:12; 13:24; 17:15;
18:15; 30:20; 32:14, 22;
34:7, 18; 43:7; 44:1; 49:9,
23
Robinson 21:21; 23:7;
29:16; 30:2
route 15:9
royalty 12:11, 17; 13:2
rule 35:10
rules 44:19
ruling 35:15
rulings 33:12, 18
run 24:14
runs 44:18

S

sales 11:16
same 8:4, 19; 19:5; 34:13;

46:22, 24
saw 37:9
saying 9:11; 10:10;
13:13; 15:1; 25:11, 22;
37:12
SCC 7:3, 7, 9; 10:15, 17;
13:13
schedule 9:3; 33:6;
49:12; 50:2
scheduled 23:21; 26:2
schedules 32:4
scheduling 24:15; 29:12;
41:3; 44:9, 20
Scherk 48:10
SCHERKENBACH 8:11;
13:8; 14:1, 13, 16, 21;
19:12; 20:6; 21:19; 22:9;
23:2; 26:1, 17; 29:11, 14,
23; 30:15; 31:20; 32:7, 20;
33:2; 34:11, 16; 37:5;
39:18; 46:6, 11, 16; 47:6;
48:1, 11, 19; 49:15; 50:3,
9, 13; 51:1, 7
school 45:11
scope 10:21; 34:13
second 15:9; 16:16;
17:14; 18:17; 21:3; 22:6;
30:13; 31:22; 32:2, 3, 15;
36:4; 46:8
section 31:9, 17
seem 4:11; 17:6; 29:14
sees 30:16
seller 12:23
send 31:10; 37:11
sense 8:15; 41:8
separate 16:6, 12; 18:2
separating 6:2; 20:18
separation 16:4; 17:8,
23; 24:9
September 22:3, 4, 15,
21; 32:3, 5, 9, 17, 23; 33:6,
22
serious 35:12
seriously 6:2
set 5:2; 18:16, 23; 22:19;
31:3, 22; 33:11; 39:7
sets 28:18
settle 18:12
settlement 18:13
seven 24:2; 25:23
Seventh 17:5; 20:23
several 9:17, 21
share 23:22
short 46:12, 18
shortly 9:4
shot 41:13
show 20:17
showed 41:6
showing 20:8
shown 5:7
side 35:8; 36:1, 3; 40:18
sides 4:3; 17:2; 21:18;
27:8; 31:2; 36:14
sideshow 10:12, 20;

19:21
significant 10:7
similar 46:23
simply 36:2; 38:9
single 11:1
six 25:13
skeptical 9:12
skewed 34:10
solve 46:2
somebody 14:8
someone 17:15; 43:11
sometimes 5:11
soon 14:12
sorry 49:21
sort 10:5, 6; 17:2; 22:8;
24:4; 45:24
SPEAKER 6:9
spend 31:16
spotting 14:22
spread 18:2
stand 13:8; 43:11
start 23:9; 25:23
Starting 23:18
starts 41:22
State 11:19; 28:5
statement 10:8
statements 7:2; 10:15;
13:4, 13; 26:21
stay 19:21
steal 14:9
still 6:13; 13:3; 17:16;
27:19; 36:17
stock 7:23; 10:18; 11:11;
20:9
stomach 17:7
straight 35:4
stretch 30:8
strike 43:18
strongly 17:24
stuck 38:12
stuff 14:3; 48:20
subject 7:14
submit 31:23
submitted 45:6
subrogation 8:22
substantial 8:21
substantially 36:9; 39:24
substantiative 8:12
substitute 20:1
sudden 41:22
sue 23:19, 20
sues 24:1
suggest 8:14
suggested 6:9, 10
summer 15:24; 39:7;
43:12
Sun 23:19
supplement 36:23;
38:20; 39:12
supplemental 19:24;
36:15

supplemented 41:11
supplementing 40:1
suppose 8:22
supposed 39:2
sure 14:6; 37:20; 39:9,
11, 12; 40:5; 46:14; 47:4, 5
surgeon 38:24; 41:17
surprise 43:10
surprised 9:18; 43:2
surprises 4:15
system 47:9

T

Tab 12:8; 46:7, 10; 47:14;
49:10, 11
talk 8:22; 16:11; 19:8;
21:10; 39:1; 50:1
talking 8:20; 11:21; 19:9;
28:8; 41:22; 45:5; 48:20
talks 43:11
technologies 27:19
ten 25:6
tend 6:21; 21:23
tends 21:23
terms 8:7, 7; 12:21;
20:18; 47:18, 19
test 5:11
testified 37:21
testify 28:20
testifying 5:13; 35:19
testimony 4:9; 5:16;
11:5; 35:16; 38:21; 39:10
thinking 6:2; 19:7; 22:7
third 23:3, 16
thirty 24:7
thorough 28:5
though 6:23; 21:4; 27:20
thought 12:1; 14:4, 5;
16:4; 21:22
three 14:8; 23:8; 24:23;
26:16; 27:4, 20
throw 48:22
Thursday 32:23
tightened 5:20
today 19:24; 20:3; 28:16;
46:3; 49:18
together 24:11
told 9:19; 19:24; 21:4;
37:12; 40:2
tone 28:18
total 11:23
toward 17:24
track 19:22
trademark 15:19
train 23:4
traveling 32:13
treatise 44:6
trebled 11:23
trial 5:22; 8:16; 16:1;
17:15; 18:15, 17; 19:7, 9;
20:5, 20; 22:4, 18; 23:6,

22; 24:10; 25:7; 29:16, 22;
30:7, 10, 18; 31:13; 32:6;
33:11; 34:22; 35:5, 11, 12,
21; 36:4, 4, 8, 12, 18;
37:12; 38:15, 18; 40:16,
19; 42:9; 43:15; 44:6, 8;
45:22
trials 16:7; 17:5
tried 27:7; 31:9
triggered 11:8
Trilogen 23:24
Troxel 48:15
true 11:12, 13; 12:24
truly 45:20
truth 10:9
try 15:23; 16:24; 18:5;
25:7
trying 38:8; 43:6, 17
turns 9:13, 21
twenties 12:3
twice 7:19
two 6:15; 9:1; 13:10;
15:24; 18:2; 23:17; 24:3;
27:16; 28:23; 29:23; 30:1,
3; 31:17; 45:6
tying 9:2
Typically 25:5; 33:9

U

U.S 6:16; 9:10, 17, 23;
10:2, 23; 11:4, 6, 16, 21
ugliness 28:17
unaware 10:24
under 12:8; 21:12; 35:10;
47:14; 48:17
understandable 36:20;
44:14
understood 14:4
undisclosed 6:18; 48:8
unduly 6:4; 16:9
United 11:19
unless 15:10, 16; 26:5;
34:9
unnamed 6:19
unreliable 7:8, 11; 19:3
untimely 48:7, 16
up 5:20; 7:18; 12:6, 7, 8;
13:8; 14:18, 22; 17:7;
22:15; 24:4; 25:12; 33:5;
35:4; 38:1, 4, 20; 40:11;
41:6; 45:3; 47:19; 49:9;
50:2, 4
upon 7:1, 22; 13:5; 19:3
use 28:21
used 14:3, 21; 36:7
usually 28:18

V

valid 15:14
validity 6:1; 8:16; 18:1, 5,
8; 20:20; 21:13, 17, 18;

25:6; 30:10; 43:15; 49:7
value 26:22
variance 35:22; 36:20
vary 13:10
verdict 15:10, 12; 18:3;
36:11
versus 22:16; 28:1; 45:10
view 10:11; 41:10; 44:7,
12, 18
violates 17:4, 14
violation 41:3
volume 5:4

W

wait 49:5
wants 23:19, 20, 24;
38:24
way 8:13; 15:14; 16:24;
17:17; 23:10; 26:6; 27:9;
29:7; 34:13; 47:1
week 23:11, 14, 18, 23;
24:5, 5, 11, 12, 13, 14, 21;
25:10, 12, 15, 22; 29:19,
21; 30:5, 9, 13; 32:14;
33:23; 37:11; 39:1; 41:18;
43:12; 46:18; 49:13
weekend 40:16
weeks 9:18; 23:8, 17;
24:3; 30:1, 4; 32:6; 50:7
weigh 29:10
weren't 41:7
what's 20:4; 23:13;
31:15; 43:7; 46:4
who's 5:13; 28:19
whole 27:6
whose 9:14
wife 23:2, 15
willing 16:5; 18:18; 19:22
window 40:9
wish 42:7
without 6:3; 21:4; 40:1
witness 4:17, 18, 19; 9:5;
17:20; 25:17, 19; 28:19;
29:4; 31:5, 15; 35:18; 36:8;
37:12; 41:1; 43:11; 44:24
witnesses 4:6, 10, 16;
5:12; 29:3; 31:17
words 33:20
work 17:20, 21; 23:8;
24:16; 30:4, 10; 33:1;
50:10
worked 21:22
working 14:10; 34:20
workout 25:3
works 27:15; 34:21
world 44:22; 45:10, 18
worldwide 11:20
worry 18:12
worth 11:20
wrap 50:4
wreck 23:5
write 33:14

written 17:11; 44:5
wrote 17:10

Y

year 15:17
years 14:6, 8, 10
yellow 48:23
yesterday 38:5

Lawyer's Notes

06-15-2006 16:04

FISH & RICHARDSON P.C.
Wilmington, DE

[Yahoo!](#) [My Yahoo!](#) [Mail](#)

Search the Web

YAHOO! FINANCE [Sign In](#)
 New User? [Sign Up](#)

[Finance Home](#) - [Help](#)

[Home](#) [Investing](#) [News & Commentary](#) [Retirement & Planning](#) [Banking & Credit](#) [Loans](#) [Taxes](#)

[Special Editions](#) [Columnists](#) [Personal Finance](#) [Investing Ideas](#) [Markets](#) [Company Finances](#) [Providers](#)

Get Quotes

GO

Symbol Lookup | Finance Search

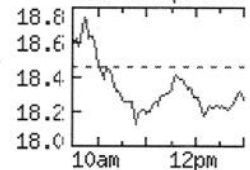


SCHWAB ACTIVE TRADER
 GO

7 Trades **Scottrade**

Related Q

FCS 11-Apr 1:1



FCS 18.23 -

[View Detailed](#)

Delayed 20 m

[Providers](#) - [Dis](#)

Press Release

Source: Fairchild Semiconductor

Fairchild Semiconductor Files Patent Infringement Lawsuit Against Power Integrations, Inc.

Tuesday April 11, 12:36 pm ET

SOUTH PORTLAND, Maine--(BUSINESS WIRE)--April 11, 2006--Fairchild Semiconductor (NYSE: [FCS](#) - [News](#)) announced today that it has filed a patent infringement lawsuit against Power Integrations, Inc. in the United States District Court for the Eastern District of Texas.

ADVERTISEMENT

[Cameras](#)

[MP3 Players](#)

[Shoes](#)

[Cell Phones](#)

[Handbags](#)

[Laptops](#)

The lawsuit asserts infringement of U.S. Patent No. 5,264,719 by Power Integrations' pulse width modulation (PWM) products. Fairchild intends to take all possible steps to seek a court order to stop Power Integrations from making, using, selling, offering for sale or importing the infringing products into the United States and to obtain monetary damages for Power Integrations' infringing activities.

Fairchild and Power Integrations have been in litigation since 2004 in the United States District Court for the District of Delaware. This lawsuit is a separate action filed in the United States District Court for the Eastern District of Texas.

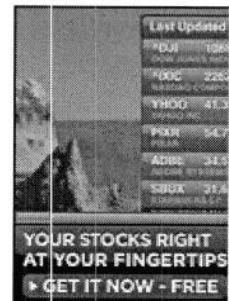
"What Power Integrations has not been able to achieve in the marketplace, they have sought to achieve in the court room. We are forced to respond in kind. However, in our case, Fairchild is asserting a patent that pre-dates Power Integrations' patents by at least fifteen months," said Tom Beaver, Fairchild's executive vice president for Worldwide Sales and Marketing. "We believe Power Integrations' products are infringing the '719 patent. We will take all possible steps to bring Power Integrations' infringement to a stop and to be made whole for the damages they are inflicting."

Intersil Corporation owns U.S. Patent No. 5,264,719, for High Voltage Lateral Semiconductor Devices, and is a co-plaintiff with Fairchild in the lawsuit. Fairchild has held license rights under the patent since 2001 and more recently secured exclusive rights to assert the patent against Power Integrations.

About Fairchild Semiconductor:

- [MagnaChip Name Executive as SVP Sales](#) - PR Newswire (
- [Fairchild Semiconductor Announces Conference First Quarter 2006 Results](#) - Business Wi
- [UPDATE - RESEARCH ALERT-Credit Sui Micro, 3 others - at \(Wed Apr 5\)](#)
- [Fairchild Semiconductor 2.0 Switch with Inc Highest 8kV ESD Ideal for Port Isola Portables](#) - Business

- By industry: [Semic Integrated Circuits](#)



Top Stor

- [Viox Plaintiff Gets to Appeal](#) - AP (11:22

Fairchild Semiconductor (NYSE: [FCS](#) - News) is the leading global supplier of high-performance power products critical to today's leading electronic applications in the computing, communications, consumer, industrial and automotive segments. As The Power Franchise®, Fairchild offers the industry's broadest portfolio of components that optimize system power. Fairchild's 9,000 employees design, manufacture and market power, analog & mixed signal, interface, logic, and optoelectronics products. Please contact us on the web at www.fairchildsemi.com.

Contact:

Fairchild Semiconductor:
Fran Harrison, 207-775-8576
Corporate Communications
Fax: 207-775-8161
fran.harrison@fairchildsemi.com

or

Agency Contact:

CHEN PR

Julianne Greenwood, 781-672-3137

Fax: 781-466-8989

jgreenwood@chenpr.com

Source: Fairchild Semiconductor

- [Gas Costs Expected to Rise High This Summer](#)
- [Stocks Slide on High Oil Prices](#) - AP (12:38 pm)
- [Skilling Denies Spouse Conspiracy](#) - AP (11:30 am)

- [Most-emailed article](#)
- [Most-viewed article](#)

RSS Feeds

Add headlines to your personalized My Yahoo! ([About My Yahoo!](#) and [RSS Feeds](#))

[FCS Headlines](#)

[Semiconductor - Integrations Headlines](#)

[More Finance RSS Feeds](#)

 [Email Story](#)

 [Set News Alert](#)

 [Print Story](#)

[Search News](#)

Sponsor Results

[Homeowners - Don't Miss Out](#)

\$145,000 mortgage for \$484 per month. Refinance while rates are still low.
www.lowermybills.com

[2.75% Fixed Student Loan Consolidation](#)

70% lower student loan payments - fixed rate, no fees, qualify in one minute.
www.nextstudent.com

[Donate Now - Food Saves Lives](#)

Your donation of \$30 will provide \$240 worth of food in East Africa. Help now.
www.worldvision.org

[\(What's This?\)](#)

Copyright © 2006 Yahoo! Inc. All rights reserved. [Privacy Policy](#) - [Terms of Service](#) - [Copyright Policy](#) - [Ad Feedback](#)
Copyright © 2006 [Business Wire](#). All rights reserved. All the news releases provided by Business Wire are copyrighted. Any forms of copying other than an individual user's personal reference without express written permission is prohibited. Further distribution of these materials by posting, archiving in a public web site or database, or redistribution in a computer network is strictly forbidden.

Exhibit B

To Fairchild's Supplemental Response to Power Integrations' First Set of Interrogatories
June 30, 2005

'075 Patent	U.S. Patent 5,264,719
1. A high voltage MOS transistor comprising:	<p>U.S. Patent 5,264,719 ("719 Patent") describes and claims "A high voltage MOS transistor comprising:". '719 Patent, Claim 8.</p> <p>The '719 Patent describes a high voltage MOS transistor. "The present invention provides an improved lateral drift region for both bipolar and MOS devices where improved breakdown voltage and low ON resistance are desired." '719 Patent, Abstract.</p> <p>"The present invention relates to lateral semiconductor devices and an improved method of making lateral semiconductor devices. More specifically, the invention relates to high voltage lateral devices with reduced ON resistance and a method of making such devices." '719 Patent, 1:12-16; see Figure 10 ("Figure 10 is a cross section of an MOS device, including the lateral drift region and top gate of the invention, in a preferred embodiment." '719 Patent, 3:18-20).</p>
a semiconductor substrate of a first conductivity type having a surface	<p>The '719 Patent describes and claims "a semiconductor substrate of a first conductivity type having a surface,". '719 Patent, Claim 8.</p> <p>An N-type semiconductor substrate (11) with a surface is shown in Figure 10. "Around the entire periphery of the drift region there is a curved portion 17_c which rounds up to the surface of the N⁻ substrate 11 to insure that the JFET channel in the drift region 17 contacts the MOS channel 11_b under the MOS gate 16." '719 Patent, 6:52-56.</p>
a pair of laterally spaced pockets of semiconductor material of a second conductivity type within the substrate and adjoining the substrate surface,	<p>The '719 Patent describes and claims "a pair of laterally spaced source and drain pockets of semiconductor material of a second conductivity type within the substrate and adjoining the substrate surface,". '719 Patent, Claim 8.</p> <p>P-type source and drain regions (14 and 12) (a pair of laterally spaced pockets of semiconductor material of second conductivity type) within substrate (11) and adjoining the substrate surface are shown in Figure 10. "For the MOS device, the drain 12 is surrounded by the P⁻ drift region 17 and N type top gate 21." '719 Patent, 6:50-52. "The P⁺ source 14 and</p>

Exhibit B

To Fairchild's Supplemental Response to Power Integrations' First Set of Interrogatories
June 30, 2005

'075 Patent	U.S. Patent 5,264,719
	N ⁺ body contact 11 _c are shown as is the dielectric 13 which serves as the gate oxide 13 _g beneath the MOS gate 16." '719 Patent, 6:59-61
a source contact connected to one pocket,	A source contact is necessarily connected to the source pocket (14) in order for the MOS device to operate.
a drain contact connected to the other pocket,	A drain contact is connected to the other pocket (drain pocket 12) in order for the MOS device to operate. "The two contacts, drain contact 12 _a and body contact 11 _c are shown for completeness." '719 Patent, 1:27-29. "FIG. 4 shows an MOS device where P ⁺ drain contact 12 _a is formed in P ⁻ type drain 12...." '719 Patent, 3:37-38.
an extended drain region of the second conductivity type extending laterally each way from the drain contact pocket to surface-adjointing positions,	<p>The '719 Patent describes and claims "an extended drain region of the second conductivity type extending laterally each way from said drain pocket to surface-adjointing positions,". '719 Patent, Claim 8.</p> <p>An extended drain region (17) of second conductivity type (P) extending laterally each way from drain contact pocket (12) to surface-adjointing positions is shown in Figure 10. "For the MOS device, the drain 12 is surrounded by the P⁻ drift region 17 and N type top gate 21. Around the entire periphery of the drift region there is a curved portion 17_e which rounds up to the surface of the N⁻ substrate 11 to insure that the JFET channel in the drift region 17 contacts the MOS channel 11_b under the MOS gate 16. The drift region 17 extends outward from the entire perimeter of the drain 12." '719 Patent, 6:50-57.</p>
a surface adjoining layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain contact pocket and the surface-adjointing positions,	<p>The '719 Patent describes and claims "a surface adjoining, top layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain pocket and the surface-adjointing positions,". '719 Patent, Claim 8.</p> <p>A surface adjoining top gate (21) of first conductivity type (N) on top of an intermediate portion of the extended drain region (17) between the drain contact pocket (12) and the surface adjoining positions is shown in Figure</p>

Exhibit B

To Fairchild's Supplemental Response to Power Integrations' First Set of Interrogatories
June 30, 2005

'075 Patent	U.S. Patent 5,264,719
	10. "For the MOS device, the P ⁺ drain 12 is surrounded by the P ⁻ drift region 17 and N type top gate 21." '719 Patent, 6:50-52.
said top layer of material and said substrate being subject to application of a reverse-bias voltage,	<p>The '719 Patent describes and claims "said top layer of material and said substrate being subject to application of a reverse-bias voltage,". '719 Patent, Claim 8.</p> <p>Top gate (21) (said top layer of material) and substrate (11) are subjected to application of a reverse-bias voltage. "This top gate allows the total channel doping to be increased because the top gate to channel depletion layer holds some additional channel charge when reverse biased in addition to that held by the bottom gate to channel depletion layer of the prior art structure." '719 Patent, 2:44-49.</p>
an insulating layer on the surface of the substrate and covering at least that portion between the source contact pocket and the nearest surface-adjointing position of the extended drain region, and	<p>The '719 Patent describes and claims "an insulating layer on the surface of the substrate and covering at least that portion between the source pocket and the nearest surface-adjointing position of the extended drain region, and". '719 Patent, Claim 8.</p> <p>A insulating dielectric layer (13) on the surface of substrate (11) and covering the portion between source contact pocket (14) and the nearest surface-adjointing position of extended drain region (17) is shown in Figure 10. "The P⁺ source 14 and N⁺ body contact 11_c are shown as is the dielectric 13 which serves as the gate oxide 13_g beneath the MOS gate 16." '719 Patent, 6:59-61.</p>
a gate electrode on the insulating layer and electrically isolated from the substrate region thereunder which forms a channel laterally between the source contact pocket and the nearest surface-adjointing position of the extended drain region, said gate electrode controlling by field-effect the flow of current thereunder through the channel.	<p>The '719 Patent describes and claims "a gate electrode on the insulating layer and electrically isolated from the substrate region thereunder which forms a channel laterally between the source pocket and the nearest surface-adjointing position of the extended drain region, said gate electrode controlling by field-effect the flow of current thereunder through the channel." '719 Patent, Claim 8.</p> <p>A gate electrode (16) on the insulating layer (13) and electrically isolated from the substrate (11) is shown in Figure 10. The gate electrode (16) controls by field-effect the flow of current through channel (11_b) between source contact pocket (14) and the nearest surface-adjointing</p>

Exhibit B

To Fairchild's Supplemental Response to Power Integrations' First Set of Interrogatories
June 30, 2005

'075 Patent	U.S. Patent 5,264,719
	position of the extended drain region (17). "Around the entire periphery of the drift region there is a curved portion 17 _e which rounds up to the surface of the N ⁻ substrate 11 to insure that the JFET channel in the drift region 17 contacts the MOS channel 11 _b under the MOS gate 16." '719 Patent, 6:52-56.
5. The high voltage MOS transistor of claim 1 combined on the same chip with a low voltage CMOS implemented device.	It is inherent or would have been obvious to combine the MOS transistor described by the '719 Patent on the same chip with a low voltage CMOS implemented device.

I hereby certify that this document is being deposited with the United States Postal Service "EXPRESS MAIL" SERVICE TO ADDRESSEE" address: 1111 and and Trade Department of Patents Date: 5/24/91 By: C. D. Jones Express Mail No.: FB 1236 905 9XU5

118/28508CO

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: James D. Beasom
SERIAL NO.: Rule 60 Continuation Application
of USSN: 242,405, Filed: September 8, 1988
FOR: HIGH VOLTAGE LATERAL SEMICONDUCTOR DEVICE

Honorable Commissioner of
Patents and Trademarks
Washington, D.C. 20231

May 24, 1991

PRELIMINARY AMENDMENT

Sir:

Preliminary to the examination of the above-identified application, the following Amendments and Remarks are respectfully submitted.

IN THE SPECIFICATION:

Page 2, eighth line from the bottom, change "drain body" to --drain-to-body--;

Page 3, line 4, change "channel body" to --channel-to-body--;

Page 3, fourth line from the bottom, change "12" to --contact 12A--;

Page 4, first full paragraph, fifth line, change "body drain" to --body-to-drain--;

Page 9, tenth line from the bottom, change "drain body" to --drain-to-body--;

Page 9, fourth line from the bottom, change "gate to drift" to --gate-to-drift--; after "junction", insert --17A--; after "gate" (last occurrence), insert --21--;

Page 10, top paragraph, line 2, after "channel", insert --17--;

Page 10, line 5, change "body to drain" to --body-to-drain--;

Page 10, line 6, change "gate to channel" to --gate-to-channel--;

Page 10, line 7, change "additon" to --addition--;

Page 10, line 13, after "region", insert --17--;

Page 10, bottom paragraph, line 3, change "body to drain" to --body-to-drain--;

Page 10, bottom paragraph, line 4, change "gate to drain" to --gate-to-drain--;

Page 10, bottom paragraph, line 5, after "11", insert --(as shown in Figures 6A, 6B to be described below)--; change "gate to drain" to --gate-to-drain--;

Page 11, line 1, change "body to drain" to --body-to-drain--;

Page 11, line 2, change "gate to drain" to --gate-to-drain--;

Page 11, second paragraph, line 3, after "region", insert --17--;

Page 11, second paragraph, line 6, after "and", insert --N--;

Page 11, second paragraph, line 8, change "effected" to
 --affected--;

Page 12, line 1, after "and", insert --,--;

Page 12, line 2, after ")", insert --,--;

Page 12, line 9, change "ion implanted" to
 --ion-implanted--;

Page 12, second paragraph, line 3, after "channel" (first
 occurrence), insert --17--;

Page 13, line 1, after "region", insert --17--; after
 "gate", insert --21--;

Page 13, line 2, after "oxide", insert --53--;

Page 13, line 13, after "gate" (last occurrence), insert
 --21--;

Page 14, line 7, after "17", insert --,--;

Page 14, second paragraph, line 8, change "so" to --as--;

Page 14, second paragraph, line 11, after "11", insert
 --, via contact region 11C--;

Page 15, first full paragraph, line 4, before "top", insert
 --N type--;

Page 15, line 8, change "gate to drift" to --gate-to-
 drift--;

Page 15, line 9, after "region" (last occurrence), insert
 --123--;

Page 15, line 10, after "negative", insert --,--;

Page 16, bottom paragraph, first line, change "base to" to
 --base-to-";

Page 16, bottom paragraph, line 4, after "gate", insert
 --126A--; after "region" (last occurrence), insert --123A--;

Page 16, bottom paragraph, line 6, after "region", insert
--123A--;

Page 16, bottom paragraph, line 7, change "ro" to --for--;

Page 17, line 3, after "shield", insert --121--;

Page 17, first full paragraph, line 5, after "region",
insert
--17--;

Page 18, first full paragraph, line 3, after "contact",
insert
--11C--;

Page 18, last paragraph, line 1, change "in" to --by way
of--; after "second", insert --(surface)--;

Page 18, last paragraph, line 2, change "217," to --217--;
before "prior", insert --(deeper)--; after "region" (last
occurrence), insert --217A--;

Page 18, last paragraph, line 3, change "as shown" to
--, refer to above--;

Page 18, last paragraph, line 4, after "region", insert
--11--; before "layer", insert --top gate--;

Page 19, line 2, change "region" to --body 11--;

Page 19, line 3, after "layers", insert --217, 250
respectively--;

Page 19, first full paragraph, line 3, change "region" to
--body 11--;

Page 19, first full paragraph, line 4, change "region" to
--first drift region 217--;

Page 19, first full paragraph, line 6, after "contact",
insert

--12A--; change "region" to --body 11--;

Page 19, first full paragraph, line 7, change "drain body" to

--drain-to-body--;

Page 19, first full paragraph, line 8, before "region", insert

--first drift--;

Page 20, line 3, change "layer" to --first drift region--;

Page 20, line 4, change "layer" (first occurrence) to --first drift region--; change "layer" (last occurrence) to --region--;

Page 20, line 5, change "layer" to --region 250--;

Page 20, first full paragraph, line 2, change "drain body" to

--drain-to-body--;

Page 20, first full paragraph, line 3, after "junction", insert --15--; change "P and N-" to --P N- --;

Page 20, first full paragraph, line 4, change "P to N" to --P N--; change "N and " to --N first drift region 217 and--;

Page 20, first full paragraph, line 5, change "regions" to --body 11--; after "layer", insert --250--;

Page 20, first full paragraph, line 6, change "layer" to --first drift region--;

Page 21, line 4, change "layer" to --first drift region--;

Page 21, first full paragraph, line 2, change "layers" to --regions--; change "250" to --221--;

Page 21, last paragraph, line 2, change "250" to --221--;

Page 21, last paragraph, line 3, change "region" to --body 11--; and

Page 21, last paragraph, line 4, change "region" (last occurrence) to --first drift region 217--.

IN THE CLAIMS:

Claim 1, delete without prejudice, and substitute therefor the following new claims.

--31. A semiconductor device comprising:

a semiconductor body of a first conductivity type having a first surface;

a first semiconductor region of a second conductivity type formed in a first portion of said first surface of said semiconductor body, and defining a first PN junction with said semiconductor body;

a second semiconductor region of said first conductivity type formed in a surface portion of said first semiconductor region and defining therewith a second PN junction, said second PN junction being spaced apart from said first PN junction by material of said first semiconductor region therebetween;

a third semiconductor region of said first conductivity type formed in a second surface portion of said semiconductor body, spaced apart from said first surface portion by a third surface portion thereof;

a fourth semiconductor region of said second conductivity type formed in a first surface part of said third surface portion of said semiconductor body spaced apart from said first surface portion of said semiconductor body by a second surface part of said third surface portion thereof and defining with said semiconductor body a third PN junction, said fourth semiconductor region being connected to said first semiconductor region and being contiguous with said third semiconductor region;

a fifth semiconductor region of said first conductivity type, and having an impurity concentration greater than that of said semiconductor body, formed in said fourth semiconductor region and defining therewith a fourth PN junction, said fifth semiconductor region being contiguous with said third semiconductor region;

an insulator layer formed on said first surface of said semiconductor body; and

a gate electrode formed on said insulator layer so as to overlies said second surface part of said third surface portion of said semiconductor body and material of said first and fourth semiconductor regions, that portion of said first semiconductor region lying beneath said gate electrode serving as a channel region of said device, said gate electrode having a gate voltage applied to induce a conductive channel through said first semiconductor region therebeneath; and wherein

when said device is reverse-biased, a first depletion region extends from said fourth PN junction into said fourth semiconductor region and said semiconductor body, and a second depletion region extends from said fifth PN junction into said fifth semiconductor region and said fourth semiconductor region;

said semiconductor body having a first ON resistance in a first current flow path therethrough between said second and third semiconductor regions, and said fifth semiconductor region providing a second ON resistance in a second current flow path along the surface of said semiconductor body from said second semiconductor region through said channel and said fourth and fifth semiconductor regions to said third semiconductor region, so that said fifth semiconductor region serves to provide a current flow path in parallel with said first current flow path, thereby effectively reducing the total ON resistance of the overall current flow path between said second and third semiconductor regions.

32. A semiconductor device according to claim 31, wherein a peripheral edge of said gate electrode is aligned with a peripheral edge of said fifth semiconductor region.

33. A semiconductor device according to claim 31, wherein said fourth semiconductor region overlaps said first semiconductor region.

34. A semiconductor device according to claim 31, wherein the impurity concentration said fifth semiconductor region is such that said fifth semiconductor region is completely depleted by said second depletion region at a reverse bias less than that at which said first and second depletion regions come together within and punch through said fourth semiconductor region.

35. A semiconductor device comprising:

a semiconductor body of a first conductivity type having a first surface;

a first semiconductor region of a second conductivity type formed in a first portion of said first surface of said semiconductor body, and defining a first PN junction with said semiconductor body;

a second semiconductor region of said first conductivity type formed in a surface portion of said first semiconductor region and defining therewith a second PN junction, said second PN junction being spaced apart from said first PN junction by material of said first semiconductor region therebetween;

a third semiconductor region of said first conductivity type formed in a second surface portion of said semiconductor body, spaced apart from said first surface portion by a third surface portion thereof;

a fourth semiconductor region of said second conductivity type formed in said third surface portion of said semiconductor body and defining with said semiconductor body a third PN junction, said fourth semiconductor region being connected to said first semiconductor region and being contiguous with said first and third semiconductor regions;

a fifth semiconductor region of said first conductivity type, and having an impurity concentration greater than that of said semiconductor body, formed in said fourth semiconductor region and defining therewith a fourth PN junction, said fifth semiconductor region being contiguous with said first and third semiconductor regions;

an insulator layer formed on said first surface of said semiconductor body; and

a gate electrode formed on said insulator layer so as to overlies material of said first and fourth semiconductor regions, that portion of said first semiconductor region lying beneath said gate electrode serving as a channel region of said device, said gate electrode having a gate voltage applied to induce a conductive channel through said first semiconductor region therebeneath; and wherein

when said device is reverse-biased, a first depletion region extends from said fourth PN junction into said fourth semiconductor region and said semiconductor body, and a second depletion region extends from said fifth PN junction into said fifth semiconductor region and said fourth semiconductor region.

36. A semiconductor device according to claim 34 wherein the impurity concentration said fifth semiconductor region is such that said fifth semiconductor region is completely depleted by said second depletion region at a reverse bias less than that at which said first and second depletion regions come together within and punch through said fourth semiconductor region.

37. A semiconductor device comprising:

a semiconductor body of a first conductivity type having a first surface;

a first semiconductor region of a second conductivity type formed in a first portion of said first surface of said semiconductor body, and defining a first PN junction with said semiconductor body;

a second semiconductor region of said first conductivity type formed in a second surface portion of said semiconductor body, spaced apart from said first surface portion by a third surface portion thereof and defining a second PN junction with said semiconductor body;

a third semiconductor region of said second conductivity type formed in a first surface part of said third surface portion of said semiconductor body spaced apart from said first surface portion of said semiconductor body by a second surface part of said third surface portion thereof and defining with said semiconductor body a third PN junction, said third semiconductor region being contiguous with said second semiconductor region;

a fourth semiconductor region of said first conductivity type, and having an impurity concentration greater than that of said semiconductor body, formed in said third semiconductor region and defining therewith a fourth PN junction;

an insulator layer formed on said first surface of said semiconductor body; and

a gate electrode formed on said insulator layer so as to overlie said second surface part of said third surface portion of said semiconductor body, that portion of said semiconductor body lying beneath said gate electrode serving as a channel region of said device, said gate electrode being applied with a gate voltage for inducing a conductive channel through said channel region;

said device being reverse-biased, so that a first depletion region extends from said third PN junction into said third semiconductor region and said semiconductor body and a second depletion region extends from said fourth PN junction into said third semiconductor region and said fourth semiconductor region;

said semiconductor body having a first ON resistance in a first current flow path therethrough between said first and second semiconductor regions, and said fourth semiconductor region providing a second ON resistance, less than said first ON resistance, in a second current flow path along the surface of said semiconductor body from said first semiconductor region through said channel and said third and fourth semiconductor regions to said second semiconductor region, so that said fourth semiconductor region serves to provide a reduced resistance current flow path in parallel with said first current flow path,

thereby effectively reducing the total ON resistance of the overall current flow path between said first and second semiconductor regions; and

wherein the impurity concentration said fourth semiconductor region is such that said fourth semiconductor is completely depleted by said second depletion region at a reverse bias less than that at which said first and second depletion regions come together within and punch through said third semiconductor region.

38. A high voltage MOS transistor comprising:

a semiconductor substrate of a first conductivity type having a surface,

a pair of laterally spaced source and drain pockets of semiconductor material of a second conductivity type within the substrate and adjoining the substrate surface,

an extended drain region of the second conductivity type extending laterally each way from said drain pocket to surface-adjoining positions,

a surface adjoining layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain pocket and the surface-adjoining positions,

said top layer of material and said substrate being subject to application of a reverse-bias voltage,

an insulating layer on the surface of the substrate and covering at least that portion between the source pocket and the nearest surface-adjointing position of the extended drain region, and

a gate electrode on the insulating layer and electrically isolated from the substrate region thereunder which forms a channel laterally between the source pocket and the nearest surface-adjointing position of the extended drain region, said gate electrode controlling by field-effect the flow of current thereunder through the channel.

39. A high voltage MOS transistor according to claim 38, wherein said extended drain region has an impurity concentration greater than $1 \times 10^{12} \text{ cm}^{-2}$.

40. A high voltage MOS transistor according to claim 38, further including an ohmic contact region of said first conductivity type formed in a surface adjoining portion of said semiconductor substrate, said ohmic contact region overlapping said top layer of material.

41. A high voltage MOS transistor comprising:

semiconductor material of a first conductivity type having a surface,

a pair of laterally spaced source and drain pockets of semiconductor material of a second conductivity type within the substrate and adjoining the surface of said semiconductor material,

an extended drain region of the second conductivity type extending laterally from said drain pocket to a surface-adjointing position,

a surface adjoinig top layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain pocket and said surface-adjointing position,

said top layer of material and said semiconductor material being subject to application of a reverse-bias voltage,

an insulating layer on the surface of said semiconductor material and covering at least that portion between the source pocket and the nearest surface-adjointing position of the extended drain region, and

a gate electrode on the insulating layer and electrically isolated from a semiconductor material region thereunder containing a channel that extends laterally between the source pocket and the nearest surface-adjointing position of the extended drain region, said gate electrode controlling by field-effect the flow of current thereunder through the channel.

42. A high voltage MOS transistor according to claim 41, wherein said extended drain region extends in a plurality of different directions from said drain pocket to respective plural surface adjoinig positions.

43. A high voltage MOS transistor according to claim 41, wherein said extended drain region surrounds said drain pocket and extends to a surrounding surface adjoinig position.

44. A high voltage MOS transistor according to claim 41, wherein said drain pocket comprises a first relatively deep pocket of a first impurity concentration and a second relatively shallow pocket formed in a surface portion of said first relatively deep pocket and having a second impurity concentration greater than said first impurity concentration and providing a drain contact region.

45. A high voltage MOS transistor according to claim 41, wherein said extended drain region has an impurity concentration greater than $1 \times 10^{12} \text{ cm}^{-2}$.

46. A high voltage MOS transistor according to claim 41, further including an ohmic contact region of said first conductivity type formed in a surface adjoining portion of said semiconductor material, said ohmic contact region overlapping said top layer of material.

47. A high voltage field effect transistor device comprising:

semiconductor material of a first conductivity type having a surface;

a source region of a second conductivity type formed in a first surface portion of said semiconductor material;

a drain region of said second conductivity type formed in a second surface portion of said semiconductor material spaced apart from said first surface portion by a third surface portion therebetween;

an extended drain region of said second conductivity type extending from said drain region beneath a first portion of said third surface portion of said semiconductor material, to adjoin a second portion of said third surface portion of said semiconductor material, spaced apart from said second surface portion of said semiconductor material, by said first portion of said third surface portion of said semiconductor material;

a surface region of said first conductivity type formed in said first portion of said third surface portion of said semiconductor material;

an insulating layer disposed on said surface of said semiconductor material, so as to overlie a third portion of said third surface portion of said semiconductor material between the second portion of said third surface portion of said semiconductor material and said first surface portion of said semiconductor material; and

a gate electrode disposed on that portion of said insulating layer overlying said third portion of said third surface portion of said semiconductor material, and wherein said surface region and said semiconductor material are subject to the application of a reverse bias voltage.

48. A high voltage field effect transistor device according to claim 47, wherein said extended drain region extends laterally in a plurality of different directions from said drain region to adjoin said second portion of said third surface portion of said semiconductor material and to adjoin a fifth surface portion of said semiconductor material.

49. A high voltage field effect transistor device according to claim 47, wherein said extended drain region surrounds said drain region and extends to a surrounding surface-adjoining portion of said semiconductor material.

50. A high voltage field effect transistor device according to claim 47, wherein said drain region comprises a first relatively deep region of a first impurity concentration and a second relatively shallow region formed in a surface portion of said first relatively deep region and having a second impurity concentration greater than said first impurity concentration and providing a drain contact region.

51. A high voltage field effect transistor device according to claim 47, wherein said extended drain region has an impurity concentration greater than $1 \times 10^{12} \text{ cm}^{-2}$.

52. A high voltage field effect transistor device according to claim 47, further including an ohmic contact region of said first conductivity type formed in a surface adjoining portion of said semiconductor material, said ohmic contact region overlapping said surface region.

53. An integrated MOS/JFET transistor device comprising an insulated gate field effect transistor and a double-sided junction field effect transistor integrated together in semiconductor substrate which contains a source region, and a drain region formed therein, and a dual channel path formed in said semiconductor material between said source and drain regions, said dual channel path comprising an insulated gate-controlled channel region having a first conductivity type in the presence of a channel-inducing gate voltage, said insulated gate controlled channel region being contiguous with a double-sided junction channel region of said first conductivity type, and wherein said source region adjoins said insulated gate-controlled channel region and said drain region adjoins said double-sided channel region.

54. An integrated MOS/JFET transistor device according to claim 53, wherein said insulated gate-controlled channel region comprises a surface portion of said semiconductor material adjoining said source region, and wherein said double-sided junction channel region comprises an extended drain region extending laterally from said drain region beneath a top gate region to said surface portion of said semiconductor material, an underlying portion of said semiconductor material extending beneath and adjoining said extended drain region and forming a bottom gate, said top gate region and said bottom gate forming respective PN junctions with said double-sided junction channel region.

55. An integrated MOS/JFET transistor device according to claim 53, wherein said extended drain region and said double-sided junction channel region surround said drain region and extend to a surrounding surface-adjoining position.

56. An integrated MOS/JFET transistor device according to claim 53, ~~wherein said extended drain region and said double,~~ wherein said drain region comprises a first relatively deep region of a first impurity concentration and a second relatively shallow region formed in a surface portion of said first relatively deep region and having a second impurity concentration greater than said first impurity concentration and providing a drain contact region.

57. An integrated MOS/JFET transistor device according to claim 53, ~~wherein said extended drain region and said double,~~ further including an ohmic contact region of said first conductivity type formed in a surface adjoining portion of said semiconductor material, said ohmic contact region overlapping said top gate.

58. An integrated MOS/JFET transistor device according to claim 53, wherein said extended drain region has an impurity concentration greater than $1 \times 10^{12} \text{ cm}^{-2}$.

59. A high voltage MOS transistor comprising:

semiconductor material of a first conductivity type having a surface;

source and drain regions of a second conductivity type adjoining spaced apart portions of the surface of said semiconductor material;

an extended drain region of said second conductivity type extending laterally from said drain region through said semiconductor material to a surface-adjoining portion of the surface of said semiconductor material;

a top gate semiconductor layer of said first conductivity type adjoining said drain region and adjoining said extended drain region along the surface of said semiconductor material to said surface-adjoining portion of the surface of said semiconductor material, said top gate semiconductor layer and said semiconductor material being subject to the application of a reverse-bias voltage;

an insulating layer on the surface of the semiconductor material and covering at least that portion of the surface of said semiconductor material between said source region and said surface-adjoining portion of said extended drain region; and

a gate electrode disposed on said insulating layer and being electrically isolated from that portion of the surface of said semiconductor material thereunder which forms a channel laterally between said source region and said surface-adjoining portion of said extended drain region, said gate electrode controlling, by field-effect, the flow of current thereunder through said channel.

60. A high voltage MOS transistor according to claim 59, wherein said extended drain region extends laterally each way from said drain region to surface-adjoining portions of the surface of said semiconductor material, and wherein said top gate semiconductor layer extends laterally in a plurality of different directions from said drain region and adjoins said extended drain region along the surface of said semiconductor material to said surface-adjoining portions of the surface of said semiconductor material.

61. A high voltage MOS transistor according to claim 59, wherein said extended drain region surrounds said drain region and extends to a surrounding surface adjoining position.

62. A high voltage MOS transistor according to claim 59, wherein said drain region comprises a first relatively deep region of a first impurity concentration and a second relatively shallow region formed in a surface portion of said first relatively deep region and having a second impurity concentration greater than said first impurity concentration and providing a drain contact region.

63. A high voltage MOS transistor according to claim 59, wherein said extended drain region has an impurity concentration greater than $1 \times 10^{12} \text{ cm}^{-2}$.

64. A high voltage MOS transistor according to claim 59, further including an ohmic contact region of said first conductivity type formed in a surface adjoining portion of said semiconductor material, said ohmic contact region overlapping said top gate layer.

65. A high voltage diode comprising:

semiconductor material of a first conductivity type having a surface,

a first, surface-adjoining region of a second conductivity type;

a second surface-adjoining region of said first conductivity type spaced apart from said first, surface-adjoining region;

a third region of said second conductivity type extending laterally from said first, surface-adjoining region; and

a fourth, surface-adjoining region of said first conductivity type overlying an intermediate portion of said third, laterally extending and surface-adjoining region.

66. A high voltage diode according to claim 65, wherein said third region surrounds said first, surface-adjoining region and extends to a surrounding surface adjoining position.

67. A high voltage diode according to claim 65, wherein said first region comprises a first relatively deep region of a first impurity concentration and a second relatively shallow region formed in a surface portion of said first relatively deep region and having a second impurity concentration greater than said first impurity concentration.

68. A high voltage diode according to claim 65, wherein said third region has an impurity concentration greater than $1 \times 10^{12} \text{ cm}^{-2}$.

69. A lateral bipolar transistor having a high voltage base-collector diode comprising:

semiconductor material of a first conductivity type having a surface and forming a base of said bipolar transistor,

a first, surface-adjointing collector region of a second conductivity type forming a base-collector junction with said semiconductor material;

a second surface-adjointing base region of said first conductivity type spaced apart from said first, surface-adjointing collector region;

a third, extended collector region of said second conductivity type extending laterally from said first, surface-adjointing collector region, so that said base-collector junction extends laterally from said first, surface adjointing collector region;

a fourth, surface-adjoining region of said first conductivity type overlying an intermediate portion of said third, laterally extending and surface-adjoining extended collector region; and

a fifth, surface-adjoining emitter region of said second conductivity type formed in said second surface-adjoining base region and defining therewith an emitter-base junction.

70. A lateral bipolar transistor according to claim 69, wherein said third region surrounds said first, surface-adjoining region and extends to a surrounding surface adjoining position.

71. A lateral bipolar transistor according to claim 69, wherein said first region comprises a first relatively deep region of a first impurity concentration and a second relatively shallow region formed in a surface portion of said first relatively deep region and having a second impurity concentration greater than said first impurity concentration.

72. A lateral bipolar transistor according to claim 69, wherein said third, extended collector region has an impurity concentration greater than $1 \times 10^{12} \text{ cm}^{-2}$.--

REMARKS

The specification has been amended to conform with the Amendment filed July 13, 1990 in parent application Serial No. 242,405.

Original claims 1-30 have been replaced by new claims 31-72. Of these newly presented claims, claims 31-37 correspond to those claims filed in the Amendments of July 13, 1990 and January 25, 1991, in parent application Serial No. 242,405, and incorporating the Amendments of the Examiner's Amendment dated February 22, 1991. New claims 38-72 embody further definitions of subject matter for which patent protection is sought.

With respect to newly added claims 38-72, to the extent that 37 C.F.R. 1.607(c) is applicable, please be advised that claim 38, although not identically copied, is considered to be generic to the invention defined in claim 1 of U.S. Patent No. 4,811,075 to Eklund. Claims 41, 47 and 59 are also considered to be generic to the invention defined in claim 1 of the patent to Eklund, 4,811,075.

U.S. Patent No. 4,823,173, of which application Serial No. 242,405, filed September 8, 1988 is a continuation-in-part, has a filing date of January 7, 1986, the present application being a continuation of application Serial No. 242,405, it is respectfully submitted that the effective filing date of the above-identified claims is the filing date of parent Patent 4,823,173, or January 7, 1986. This filing date antedates the filing date of April 24, 1987 of the above-identified Eklund patent, 4,811,075.

Early examination of the present application is earnestly solicited.

To the extent necessary, Applicants petition for an Extension of Time under 37 C.F.R. 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including Extension of Time fees, to Deposit Account No. 05-1323 (118/28508CO) and please credit any excess fees to such deposit account.

Respectfully submitted,

Charles E. Wands
Reg. No. 25,649
EVENSON, WANDS, EDWARDS,
LENAHAN & MCKEOWN

CEW:cn
Attachment
(407) 725-4760
(202) 828-8300

pat\28508.pa



US005264719A

United States Patent [19][11] **Patent Number:** **5,264,719****Beasom**[45] **Date of Patent:** **Nov. 23, 1993**[54] **HIGH VOLTAGE LATERAL SEMICONDUCTOR DEVICE**[75] **Inventor:** **James D. Beasom**, Melbourne Village, Fla.[73] **Assignee:** **Harris Corporation**, Melbourne, Fla.[21] **Appl. No.:** **705,509**[22] **Filed:** **May 24, 1991**

4,628,341 12/1986 Thomas 357/23.8
 4,811,075 3/1989 Eklund et al. 357/46
 4,994,889 2/1991 Takeuchi et al. 357/55
 4,994,904 2/1991 Nakagawa et al. 357/38

Primary Examiner—Rolf Hille*Assistant Examiner*—Roy Potter*Attorney, Agent, or Firm*—Evenson, Wands, Edwards, Lenahan & McKeown[57] **ABSTRACT**

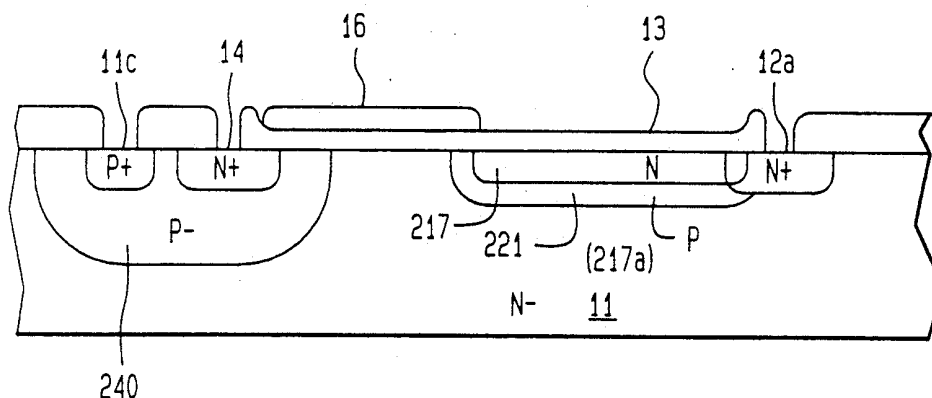
The present invention provides an improved lateral drift region for both bipolar and MOS devices where improved breakdown voltage and low ON resistance are desired. A top gate of the same conductivity type as the device region with which it is associated is provided along the surface of the substrate and overlying the lateral drift region. In an MOS device, the extremity of the lateral drift region curves up to the substrate surface beyond the extremity of the top gate to thereby provide contact between the JFET channel and the MOS channel.

Related U.S. Application Data

[63] Continuation of Ser. No. 242,405, Sep. 8, 1988, abandoned, which is a continuation-in-part of Ser. No. 831,384, Jan. 7, 1986, Pat. No. 4,823,173.

[51] **Int. Cl.⁵** **H01L 29/80**[52] **U.S. Cl.** **257/335; 257/336; 257/339**[58] **Field of Search** 357/38, 55, 23.8, 46[56] **References Cited****U.S. PATENT DOCUMENTS**

4,626,879 12/1986 Colak 357/23.8

42 Claims, 7 Drawing Sheets

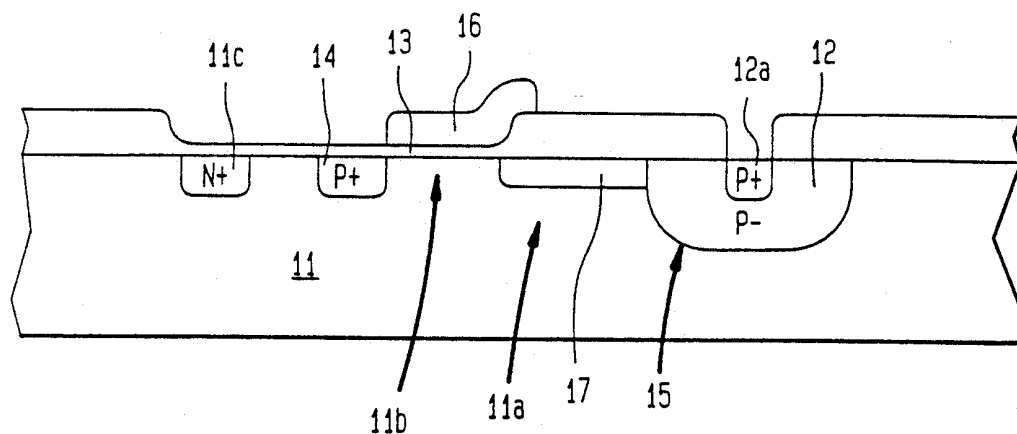


FIG. 1

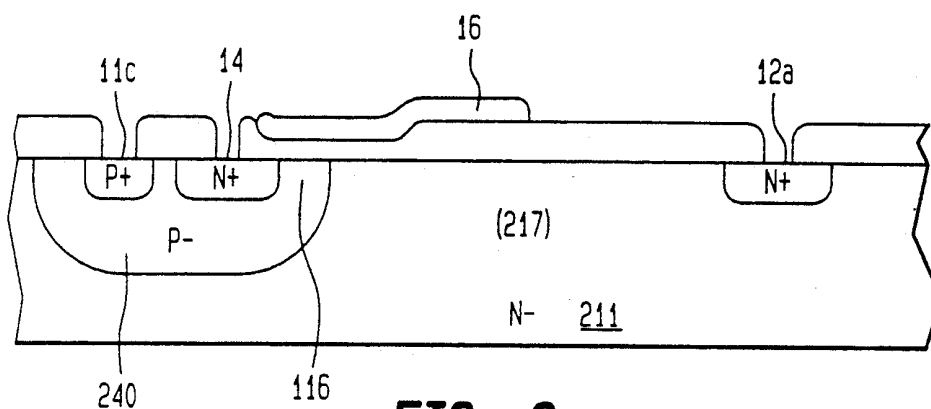


FIG. 2
(PRIOR ART)

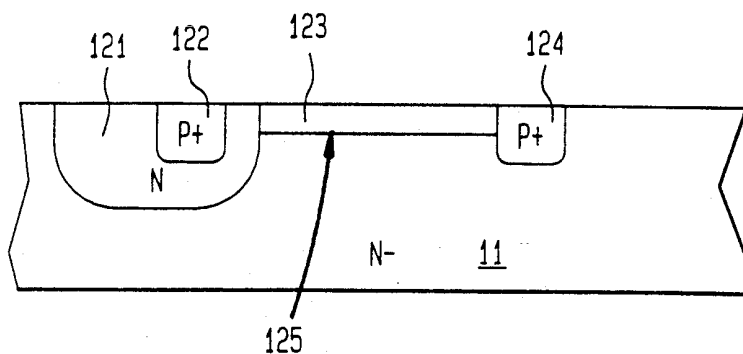


FIG. 3

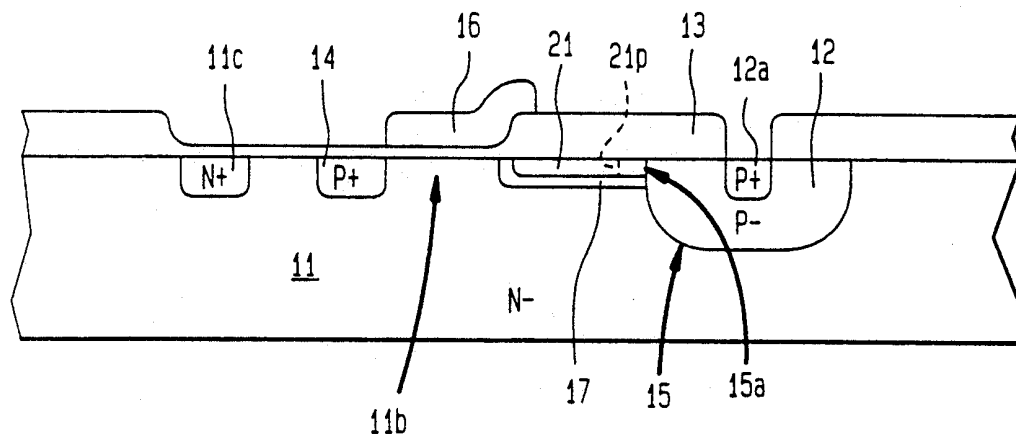


FIG. 4

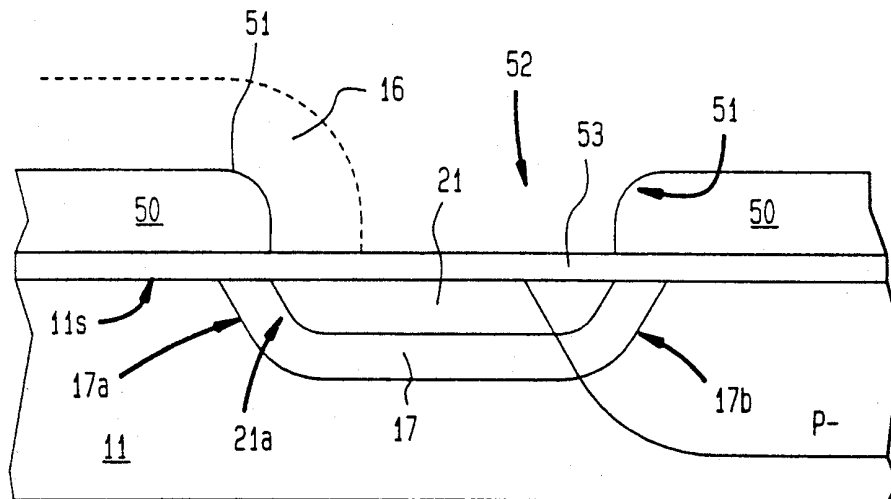


FIG. 5

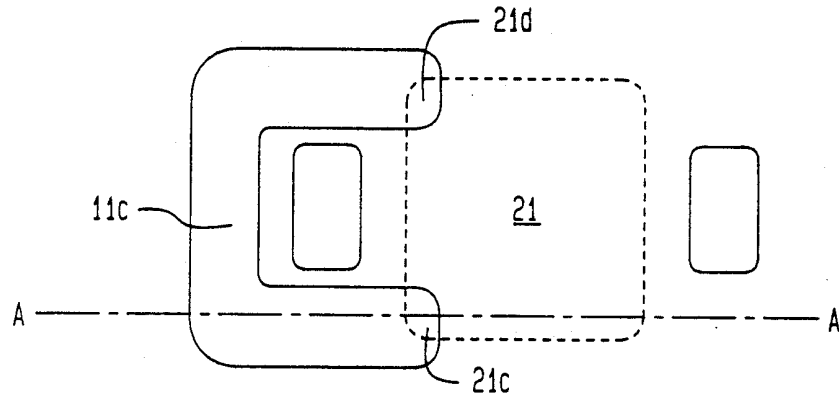


FIG. 6a

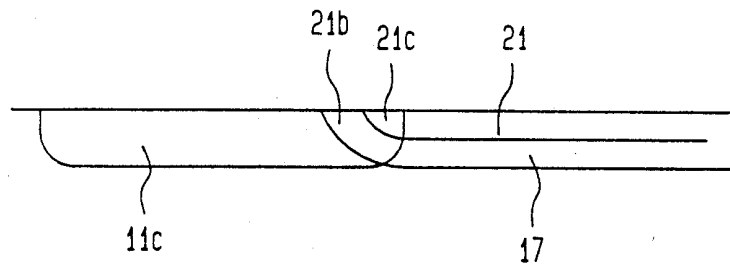


FIG. 6b

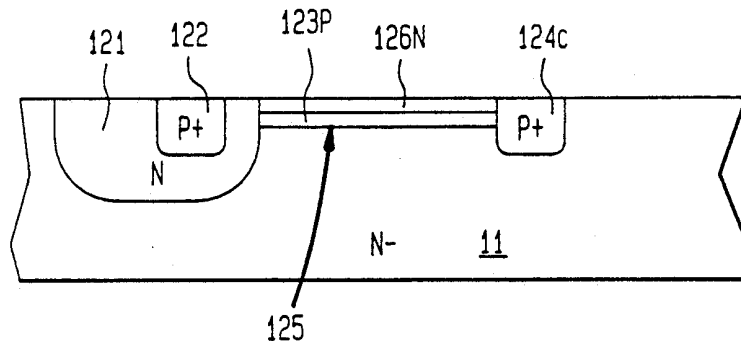


FIG. 7

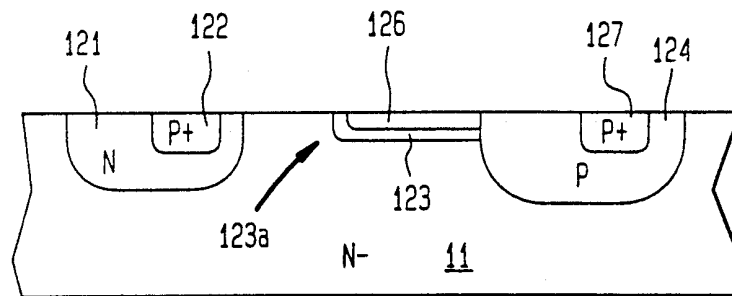


FIG. 8

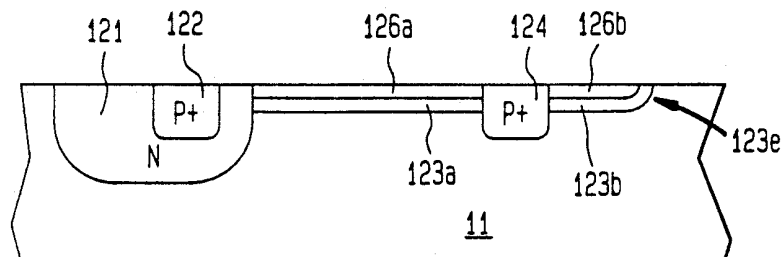


FIG. 9

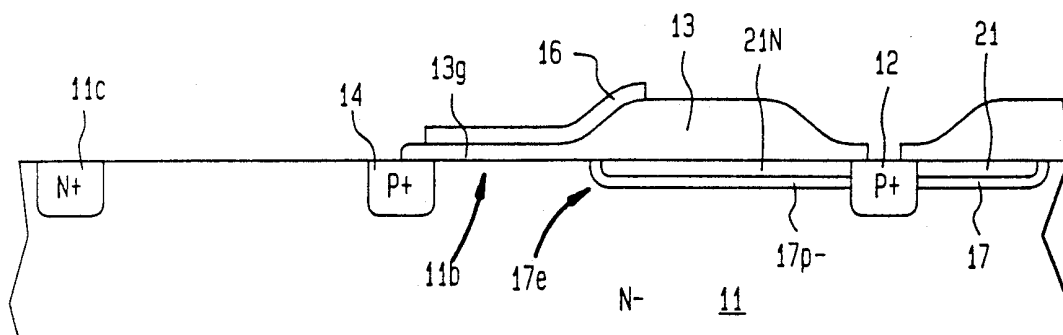


FIG. 10

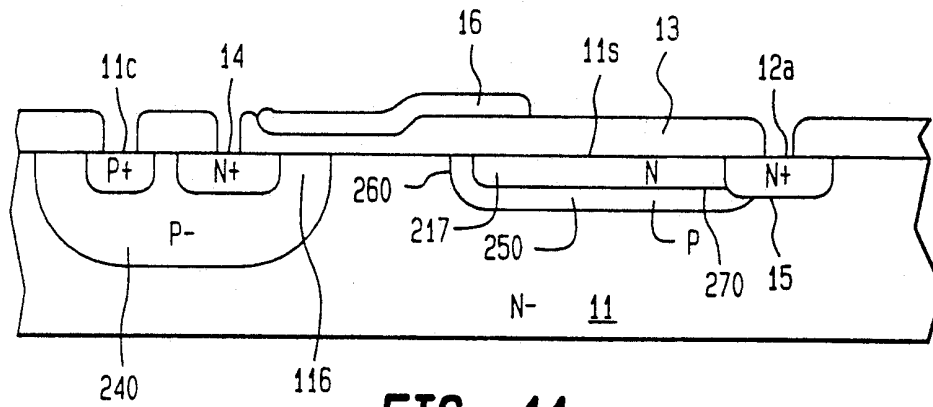


FIG. 11

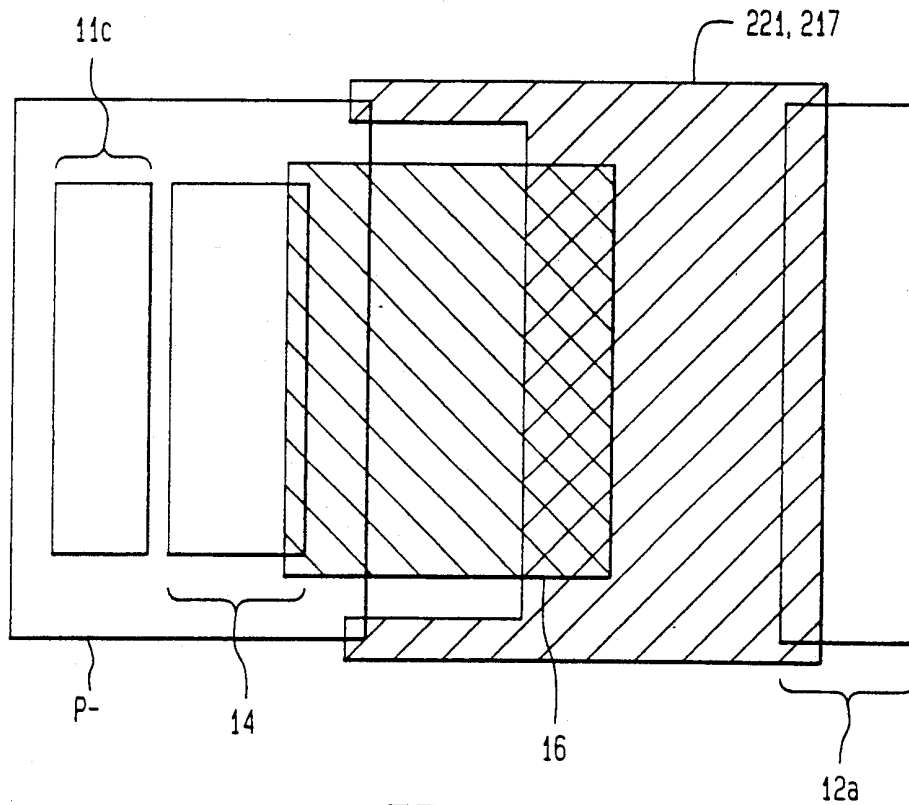


FIG. 12

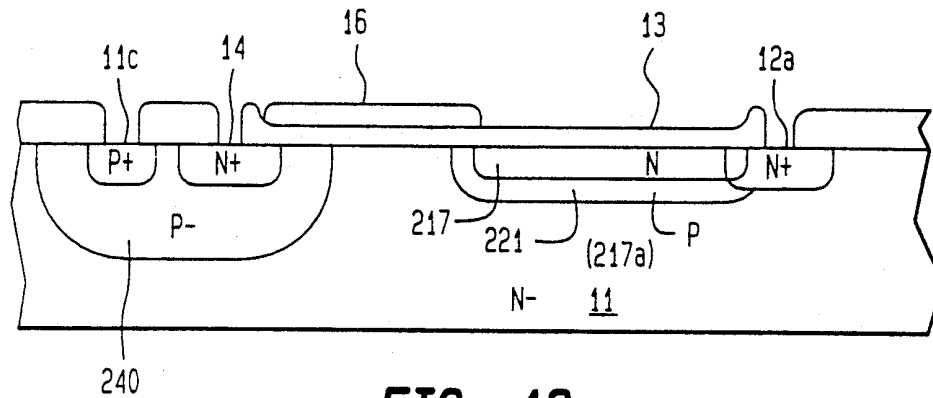


FIG. 13

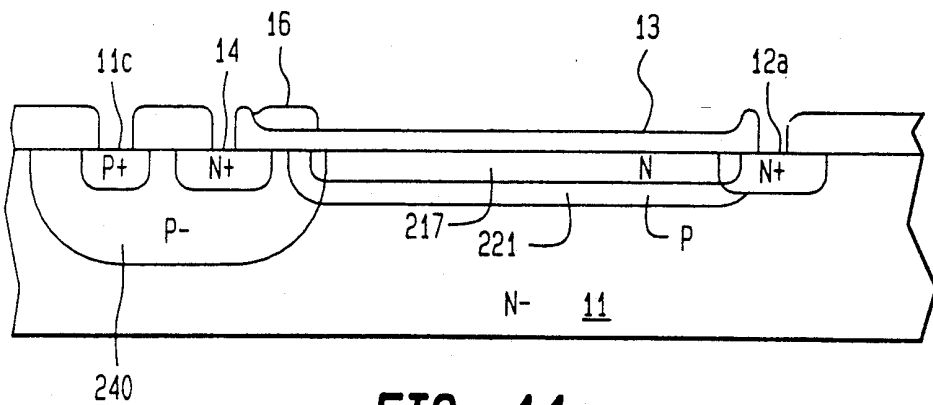


FIG. 14

HIGH VOLTAGE LATERAL SEMICONDUCTOR DEVICE

This is a continuation of application, Ser. No. 242,405, filed Sep. 8, 1988, now abandoned which, in turn, is a continuation-in-part of application, Ser. No. 831,384, filed Jan. 7, 1986, now U.S. Pat. No. 4,823,173, issued Apr. 18, 1989.

FIELD OF THE INVENTION

The present invention relates to lateral semiconductor devices and an improved method of making lateral semiconductor devices. More specifically, the invention relates to high voltage lateral devices with reduced ON resistance and a method of making such devices.

Previous high voltage lateral devices include both MOS devices and bipolar transistors. For example, FIG. 1 illustrates a known structure which can be used as a high voltage lateral MOS device. This device is known as a lateral drift region MOS device and is dependent upon the drain-to-body junction 15 as the basic high voltage junction of the device. The drift region 17 is a P region along the top surface of the N- substrate 11 and is located so as to lie adjacent the P- drain region 12. The drift region 17 is used to connect the high voltage drain 12 to the gate 16 and source 14. The two contacts, drain contact 12_a and body contact 11_c are shown for completeness. In the operation of this circuit, the gate 16 and source 14 never assume large voltages relative to the body 11. The drift region 17 serves as a JFET channel with the portion 11_a of body region 11 underlying the channel acting as a JFET gate. The JFET channel 17 is designed to totally deplete when the drain 12 is reverse biased to a voltage less than the voltage necessary to reach critical field in the channel-to-body depletion layer. This design preserves the effective high breakdown voltage of drain body junction 15. Also the source 14 and gate 16 (over the gate oxide 13) are safely shielded from the high drain body voltage by the pinched off JFET channel 17.

The resistance of the lateral drift region JFET channel 17 is in series with the resistance of the MOS channel 11_b, consequently the total channel resistance of the device is the sum of these two individual resistances. The JFET channel, which must be quite long to sustain high drain body voltages, is often the larger of the two resistance terms. Thus it is desirable to find ways to reduce the resistance of the drift region so that devices of a given size can be made with smaller channel resistance.

FIG. 2 illustrates a known structure which can be used as a high voltage lateral DMOS (LDMOS) device. In this device, an N⁺ drain contact 12A is formed in the N- substrate 211 and an N⁺ source 14 and P⁺ body contact 11_c are formed in a P- body region 240. The drift region 217 is an N- region along the top surface of the N- substrate 211 which connects the drain 12 to the gate 16 and source 14. In this high voltage device, the N- drift region 217 must be lightly doped to obtain high body 240 to drain breakdown.

The ON resistance of the LDMOS is approximately the sum of the channel resistance and the bulk resistance in the N- drift region 217. The lateral distance from the N⁺ drain 12 to the adjacent edge of the MOS channel 11_b underlying the gate on the P- body 240 must be large to allow space for the reverse bias depletion layer which spreads from the body-to-drain junction into the

lightly doped drain. This distance, along with the high N- resistivity contribute to the high drift region resistance, which is often much greater than the channel resistance. Thus, it is desirable to reduce the drift region resistance of the LDMOS device.

FIG. 3 shows a known structure which can be used as a lateral bipolar transistor. Another illustration of such a device is contained in FIG. 7 of U.S. Pat. No. 4,283,236 issued Aug. 11, 1981. Referring to FIG. 3, an N- substrate 11, has an N type emitter shield 121 formed therein and P⁺ emitter 122 and collector 124 formed as shown. Additionally, a P- drift region 123 is provided along the surface of the substrate between the collector 124 and the emitter shield 121. In the operation of this device, the total collector resistance is equal to the sum of the resistance across the drift region 125 plus the resistance of the P⁺ collector between the drift region and the collector contact. In order to provide devices of equal size having a lower collector resistance, it is desirable to find ways to reduce the resistance of the drift region.

In the operation of this device, the drift region extends the collector to the edge of the emitter shield, 121, so that the base width is just that small distance between the adjacent edges of the emitter, 121, and the drift region, therefore, providing improved frequency response.

At high base-collector voltages, the drift region, 123, depletes by JFET action with the N-base, 11, and N shield, 121, which is part of the base, acting as gate before critical field is reached just as for the MOS of FIG. 1. This preserves the high breakdown of the structure.

SUMMARY OF THE INVENTION

The present invention provides a structure having a reduced channel resistance and a process capable of efficiently obtaining the structure of the invention. The reduction in channel resistance is accomplished by providing a top gate which is located between the lateral drift region of the prior art and the surface of the channel region and which may be in contact with the high voltage device region. This top gate allows the total channel doping to be increased because the top gate to channel depletion layer holds some additional channel charge when reverse biased in addition to that held by the bottom gate to channel depletion layer of the prior art structure. The ionized channel impurity atoms associated with this additional channel charge causes the reduction in channel resistance.

With respect to providing an improved LDMOS structure having a lower drift region resistance, a second drift region which is separated from the original drift region by a region of opposing conductivity is formed. The second drift region provides a conductive path which is in parallel with the original drift region thereby achieving the desired reduction in resistance. Because of the formation of the second drift region, the first enclosed drift region can now have a much higher doping than the second drift region which it replaces, while achieving the same breakdown voltage.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cross section of a known MOS device having typical ON resistance.

FIG. 2 is a cross section of a known LDMOS device having typical ON resistance.

FIG. 3 is a cross section of a known bipolar transistor having typical collector resistance.

FIG. 4 is a cross section of an MOS device including the improved drift region and top gate of the invention.

FIG. 5 illustrates optimized process steps for obtaining the desired shape of the top gate and drift region of the invention.

FIGS. 6a and 6b are, respectively, a top view and a cutaway perspective view of the body contact extending through the top gate and drift region of the invention.

FIG. 7 is a cross section of a bipolar device made in accordance with one aspect of the invention.

FIG. 8 is a cross section of a bipolar device made in accordance with another aspect of the invention.

FIG. 9 is a cross section of a bipolar device made in accordance with a preferred aspect of the invention.

FIG. 10 is a cross section of an MOS device, including the lateral drift region and top gate of the invention, in a preferred embodiment.

FIG. 11 is a cross section of a LDMOS device made in accordance with a preferred embodiment of the invention.

FIG. 12 is a top view of the LDMOS device of FIG. 11.

FIG. 13 is a cross section of a LDMOS device made in accordance with another preferred embodiment of the invention.

FIG. 14 is a cross section of a LDMOS device made in accordance with still another preferred embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

The present invention is described herein with reference to the drawings for both MOS and bipolar applications. FIG. 4 shows an MOS device where P⁺ drain contact 12_a is formed in P⁻ type drain 12, P⁺ source 14 is formed in the N⁻ body 11 and N⁺ body contact 11_c is provided in the N⁺ body 11. The MOS channel region 11_b is in the N⁻ body 11 below the MOS gate 16. The N type top gate 21 is provided along the surface 11_s of the body 11 above the P type drift region 17 which acts as a JFET channel. The lateral edge or peripheral edge of both the top gate 21 and drift region 17 extend to the drain-to-body junction 15 and preferably terminate at the junction 15. It is noted that situations may exist where the doping level in the top gate may be sufficiently high so as to render it desirable to provide a shorter top gate having a lateral extension which stops short of contacting the junction 15. In this case care should be taken to insure that any nondepleted portion of the top gate does not result in a breakdown of the top gate-to-drift region junction 17A. Proper doping of the top gate 21 will generally be a sufficient preventative step. Dashed line 21_p designates the peripheral edge of top gate 21 in an embodiment where the top gate does not extend all the way to the junction 15.

The structure of FIG. 4 provides reduced ON resistance in the JFET channel 17 relative to the prior art lateral drift MOS device as shown in FIG. 1. The reduction in ON resistance is accomplished by providing a structure which can accommodate increased drift region doping without suffering from reduced body-to-drain breakdown. This is possible because of the provision of the top gate 21. The top gate-to-channel depletion layer which holds some channel charge when reverse biased, is in addition to the channel charge held by

the bottom gate to channel depletion layer of the prior art. This additional channel charge, in the form of ionized channel impurity atoms, causes the reduction in channel resistance. It is possible to provide more than twice the doping level previously acceptable due to the additional ability to hold channel charge. Thus, for a drift region 17 having a doping of 1×10^{12} boron atoms per square centimeter in a bottom gate arrangement, the present invention will permit 2×10^{12} boron atoms per square centimeter. Thus, the ON resistance will be only half the ON resistance of the prior arrangement.

In order to optimize performance of the structure of the invention, the top gate 21 must be designed differently than an ordinary JFET gate. Top gate 21 should become totally depleted at a body-to-drain voltage of less than the breakdown voltage of the top gate-to-drain junction 15. Since top gate 21 is connected to body 11 (as shown in FIGS. 6A, 6B to be described below), the voltage at the top gate-to-drain junction 15_a will equal the voltage of the body-to-drain junction 15 voltage and the top gate-to-drain breakdown voltage should be greater than the voltage at which top gate 21 becomes totally depleted. Additionally, the top gate 21 must totally deplete before the body 11 to channel 17 depletion layer reaches the top gate 21 to channel 17 depletion layer to thereby assure that a large top gate 21 to drain 12 voltage is not developed by punch-through action from the body 11. An ordinary JFET gate never totally depletes regardless of operating conditions.

In addition to the above described characteristics of the device of the invention, it is also necessary to insure that the channel of the JFET drift region 17 contacts the inversion layer MOS surface channel. This can be accomplished as shown in FIG. 5 where an implant mask 50 having a tapered edge 51 is provided over the body 11. An implant aperture 52 is provided in mask 50 at the location where the P drift region 17 and N top gate 21 are to be formed. The aperture 52 is shown as exposing the protective oxide 53. Ion implantation is not substantially affected by the oxide 53 due to the oxide thickness of only about 0.1–0.2 micrometers, yet the oxide provides surface passivation for the underlying body 11.

The drift region 17 is ion implanted and, because of the graduated thickness of the implant mask 50 (along the edge 51), the depth of the implanted drift region 17 is graduated or tapered. In the illustration, a fairly good rounding of the drift region 17 occurs at the peripheral edges or extremities 17_a, 17_b of the region 17. The curved extremity 17_a is of interest because at this location the channel of the JFET drift region 17 contacts the surface 11_s of body 11 beyond the end 21_a of top gate 21 and is desirably beneath the gate 16 of the MOS device. The top gate 21 may be ion-implanted using the implant mask 50 but at an energy level which results in a shallower implantation. This tapered profile, particularly if curved, provides improved performance.

In a variation of this method, a diffusion process can be used to bring the JFET channel into contact with the surface of body 11, and hence insure that the JFET channel 17 will contact the inversion layer MOS surface channel (lateral drift region 17 and top gate 21 are diffused after initial introduction by ion implant). The doping levels and diffusion times are chosen such that the extremity 17_a of JFET channel 17 diffuses beyond the end 21_a of the top gate 21 and so that the end 17_a reaches the surface 11_s of body 11. In practice, this approach can be facilitated by choosing a top gate dop-

ant which has a lower diffusion coefficient than that of the drift region dopant.

The formation of the drift region 17 and top gate 21 may be conveniently carried out by forming a mask over the gate oxide which is present in a lateral MOS application. The MOS gate may be utilized as one delineating edge of the implant for the drift region and top gate and a thick oxide portion surrounding a thinner oxide portion may form the remainder of the implant mask. The thinner oxide portion shall be located such that it extends from beneath the MOS gate to the drain and preferably overlaps the drain. The implant mask 50 illustrated in FIG. 5 is shown as having thin oxide portion 53 being surrounded by the implant mask 50. If the MOS gate 16 shown in dashed lines were used as a portion of the mask 50, the edge of the drift region and top gate would be self-aligned with the MOS gate as shown in dashed lines. Then, when diffused, the drift region will extend laterally to a point beneath the MOS gate, while the top gate 21 may be formed such that there is little or no lateral overlap with the MOS gate. The extent of lateral diffusion of the top gate is dependent upon the dopant material and processing temperatures following top gate implant. It is noted that there is a separation between the drift region and the source. This separation zone is the location where the MOS channel is located.

The top gate 21 will perform as previously described if it is tied to the body 11. Thus, the top gate 21 and the body which operates as the bottom gate of the JFET channel will be at equal potential. According to the invention, this may be accomplished in a particularly effective manner if the drift region 17 is widened to overlap with the body contact region 11_c. This is shown in FIG. 6a which shows the overlapping of the top gate 21 and the body contact 11_c at the overlap regions 21_c, 21_d. In order for this arrangement to be effective, it is necessary that the body contact 11_c have a higher dopant concentration than the JFET channel (or drift region) 17, as shown in FIG. 6b to insure that the body contact 11_c forms a continuous region horizontally and/or vertically through the JFET channel and to the body region 11 from the top gate, 21.

FIG. 6b shows a cross section of the structure of FIG. 6a taken along dashed line A—A. The body 11 is provided with body contact 11_c which is located such that the top gate 21 and drift region 17 can be conveniently extended to overlap the body contact 11_c. The depth of body contact 11_c may be made greater than the depth of region 17 such that a portion of the body contact 11_c extends below region 17 and provides contact with the body 11. This arrangement provides a contact portion 21_c where the top gate 21 is in contact with body contact 11_c. Thus, as long as the body contact doping concentration in region 21_b is sufficiently high to overcome the opposite doping in region 17, then a good connection of uniform conductivity type will be provided between the top gate 21 and the body 11, via contact region 11_c. It is also noted that the body contact 11_c extends laterally beyond the end of both of the top gate 21 and the drift region 17. The lateral extension of the contact 11_c will also provide a structure which results in a good connection of uniform conductivity type from the top gate 21 to the body 11, again, provided that the doping of body contact 11_c converts region 21_b.

Another area where the present invention finds application is in lateral bipolar transistors which employ a lateral drift region. The known structure of FIG. 3 may

be improved by providing an N type top gate 126 as shown in FIG. 7. In this arrangement the N type gate 126 extends from the collector 124 to the emitter shield 121 along the surface of body 11. The operation of this device is enhanced by the same phenomenon as the lateral drift region of the previously described MOS device. As the base 11 becomes positive relative to the collector 124, the top gate-to-drift region depletion layer facilitates pinch-off of the drift region 123. However, as the base 11 becomes more negative, the top gate 126 contributes additional surface exposure to the drift region 123 and further enhances carrier transportation.

FIG. 8 shows an improvement over the arrangement shown in FIG. 7. In FIG. 8 the drift region 123 does not extend all the way over to the emitter shield 121. The curved end 123_a of the drift region 123 contacts the top surface of body 11. It is noted that in this arrangement, the emitter shield 121 may be omitted.

An additional improvement shown in FIG. 8 is the use of a deep diffusion to form the collector 124 resulting in a significantly increased breakdown voltage. The deep diffusion step may be the same step used for forming the emitter, in which case the collector 124 shown in FIG. 7 would be deeper, or a separate collector implant and diffusion step may be employed and the collector contact 127 may then be formed simultaneously with the formation of the emitter 122. This improvement in junction breakdown voltage is equally obtainable, for example, at the body to drain junction in the MOS devices described previously.

A further extension of the invention which may be used to increase base-to-collector breakdown voltage for a PNP device is shown in FIG. 9. In addition to the provision of the N type top gate 126_a over the P- drift region 123_a, the top gate 126_a and drift region 123_a are enlarged to surround the collector 124 and a curved edge 123_b is provided at the periphery of the enlarged portion 123_b of the drift region 123_a. This enlarged portion is designated by reference numerals 123_b for the drift region and 126_b for the top gate. The collector 124 to base 11 breakdown voltage is increased relative to alternative arrangements because of mitigation of the breakdown reduction due to the junction curvature. The top gate 126_a extends to the emitter shield 121 as does the drift region 123_a. The P+ emitter 122 is formed in the N+ type emitter shield 121.

FIG. 10 illustrates an extension of the invention with respect to a P channel MOS device similar to the improvement described with respect to the bipolar device shown in FIG. 9. For the MOS device, the drain 12 is surrounded by the P- drift region 17 and N type top gate 21. Around the entire periphery of the drift region 17 there is a curved portion 17_e which rounds up to the surface of the N- substrate 11 to insure that the JFET channel in the drift region 17 contacts the MOS channel 11_b under the MOS gate 16. The drift region 17 extends outward from the entire perimeter of the drain 12. This arrangement mitigates the breakdown reduction due to junction curvature. The P+ source 14 and N+ body contact 11_c are shown as is the dielectric 13 which serves as the gate oxide 13_g beneath the MOS gate 16.

In both the arrangements shown in FIG. 9 and FIG. 10, the planar diode breakdown improvement created by the drift region acting as a surface layer of the same conductivity type as the collector in FIG. 9 and drain in FIG. 10 and extending out from the perimeter of the collector and drain can be implemented by a single series of process steps. According to the invention, a

common set of process steps produces both a suitable breakdown improvement layer and an improved drift region. The breakdown improvement layer is a two layer component.

A further extension of the invention is illustrated in FIG. 11 which shows an LDMOS device where N⁺ drain contact 12_a is formed in an N⁻ type substrate and an N⁺ source 14 and P⁺ body contact 11_a are formed in a P⁻ type body region 240. The DMOS channel region 11_b is in the P⁻ body 240 below the DMOS gate 16. The N type first drift region 217 is provided along the surface 11_c of the substrate 11 above a P⁻ type separation region 250. A second drift region 217_a exists in the substrate 11 underneath the P⁻ type separation region. The lateral edge of both the first drift region 217 and the separation region 250 extend from the gate 16 to the N⁺ drain contact 12_a.

The structure in FIG. 11 provides reduced ON resistance by way of the second (surface) drift region 217_a relative to the (deeper) prior art lateral first drift region 217_a device, refer to above in FIG. 2. To illustrate this, consider an example in which the N⁻ region 11 has a doping of 1×10^{14} ions cm⁻³. The top gate layer 217 has an integrated doping of about 1×10^{12} ions cm⁻² and is preferably not more than two microns thick while maintaining full breakdown. The thickness of the N and P layers 217, 250 together is preferably less than ten microns and can be less than one micron. The same integrated doping in the N⁻ body 11 requires a thickness of 100 microns. Thus, the N and P layers 217, 250 respectively consume only a small fraction of the N⁻ thickness required to provide doping equal to that portion of the N layer of the prior art device.

The lateral spacing between the drain contact 12_a and the channel 11_b in the device described above would be approximately 30 microns. In such a device, even if a full 100 micron thick N⁻ body 11 were provided, it would have a higher resistance than the N⁻ first drift region 217 provided according to the invention. This is because the average path length of current flowing from the drain contact 12A down through the thick N⁻ body 11 and back up to the surface edge of the channel at the drain-to-body junction would be greater than the direct path through the N⁻ first drift region.

Maximum breakdown is achieved in the invention by providing doping densities of the N and P layers 217, 250 such that they become totally depleted before breakdown is reached at any point along the junctions which they form with adjoining regions and before breakdown is reached at the junction between them. To insure that this occurs, the N region 217 should have an integrated doping not exceeding approximately 1×10^{12} ions cm⁻² and the P region 250 should have a higher integrated doping not exceeding about 1.5 to 2×10^{12} ions cm⁻².

To insure proper depletion of the P and N regions 250, 217, they must have the proper voltages applied. The N layer bias is achieved by connecting the N first drift region 217 to the higher concentration N⁺ drain contact 12_a by overlapping the N first drift region 217 and drain contact 12_a. The P region 250 bias is achieved by overlapping the P region 250 with the P⁻ body 240 at least at one end of the channel, thereby applying the body voltage to the P layer 250. This is illustrated in FIG. 12.

With this structure and choice of doping levels, the desired results are achieved. When a reverse bias voltage is applied to the drain-to-body junction 15, the same

reverse bias appears on both the PN⁻ junction 260 and the PN junction 270. Depletion layers spread up into the N first drift region 217 and down into the N⁻ body 11 from the P layer 250. In a preferred embodiment, the P and N first drift region dopings are chosen such that the N layer 217 becomes totally depleted at a lower voltage than that at which the P layer 250 becomes totally depleted. This insures that no residual undepleted portion of the N layer 217 is present which could reduce breakdown voltage.

As a result of the invention, the improved DMOS device provides a reduced resistance current path in the drain which does not depend on the N⁻ doping. This allows the N⁻ doping to be reduced to achieve a desired breakdown voltage with good manufacturing margin, while maintaining desirable low drift region resistance. In a multi-device process which includes LDMOS devices, the N⁻ region can be adjusted to achieve the desired characteristics of one or more of the other device types, while the N first drift region 217 sets the drift region 217 resistance of the LDMOS.

Another embodiment of the DMOS invention is illustrated in FIG. 13, where the N and P regions 217, 221 are self-aligned to the gate 16 by using the gate 16 as a mask. An advantage of this structure is that N and P regions can be defined by the uncovered thin oxide area which extends from gate edge to overlap the drain contact. This embodiment requires no explicit mask step to delineate the location where the N and P regions are formed.

Still another embodiment, as illustrated in FIG. 14, provides no gap between the P⁻ body 240 and the P region 221 adjacent to the channel edge. The absence of the gap prevents current from flowing in the N⁻ body 11; so the entire drift region current path is in the N first drift region 217. Elimination of the gap also allows the device structure to be made smaller. As with the other structure, the N and P regions may be self-aligned to the gate edge, as illustrated in FIG. 14, or not self-aligned. They may also be covered by thick or thin oxide as a design option.

A preferred feature of the present invention provides that the body or substrate regions 11 shown in the FIGS. 3, 4, 6, 7, 8, 9, 11, 13 and 14 are designed to be dielectrically or self-isolated regions. In contrast with the typical RESERF type of devices in which the bottom isolation junction plays a central role in the action of the device, the present invention contemplates that the isolation junction does not contribute to the depletion of the drift or top gate regions which are taught to be totally depleted. Prior art RESERF devices such as that described in U.S. Pat. No. 4,300,150 to Colak always require the substrate to be part of such depletion whereby the substrate must assume the most negative voltage in the device because of its role as one side of the isolation junction. As a result of this bias on the substrate or body region, the prior art RESERF type devices are susceptible to punch through from the device region through the epitaxial layer to the substrate. As a result of the present invention not having the substrate as part of the depletion mechanism, the invention can more effectively provide high voltage protection while not increasing the resistance of the channel path. Although the figures illustrate a nonisolating structure or self-isolated structure, it is understood that the invention applies equally well to dielectrically or junction isolated substrates.

While the present invention has been described with respect to several preferred manners of implementing the invention, it is to be understood that the claims appended hereto are intended to cover the invention in its broadest sense and are not to be limited to the specific implementations disclosed.

What is claimed is:

1. A semiconductor device comprising:

- a semiconductor body of a first conductivity type having a first surface;
- a first semiconductor region of a second conductivity type formed in a first portion of said first surface of said semiconductor body, and defining a first PN junction with said semiconductor body;
- a second semiconductor region of said first conductivity type formed in a surface portion of said first semiconductor region and defining therewith a second PN junction, said second PN junction being spaced apart from said first PN junction by material of said first semiconductor region therebetween;
- a third semiconductor region of said first conductivity type formed in a second surface portion of said semiconductor body, spaced apart from said first surface portion by a third surface portion thereof;
- a fourth semiconductor region of said second conductivity type formed in a first surface part of said third surface portion of said semiconductor body spaced apart from said first surface portion of said semiconductor body by a second surface part of said third surface portion thereof and defining with said semiconductor body a third PN junction, said fourth semiconductor region being connected to said first semiconductor region and being contiguous with said third semiconductor region;
- a fifth semiconductor region of said first conductivity type, and having an impurity concentration greater than that of said semiconductor body, formed in said fourth semiconductor region and defining therewith a fourth PN junction, said fifth semiconductor region being contiguous with said third semiconductor region;
- an insulator layer formed on said first surface of said semiconductor body; and
- a gate electrode formed on said insulator layer so as to overlie said second surface part of said third surface portion of said semiconductor body and material of said first and fourth semiconductor regions, that portion of said first semiconductor region lying beneath said gate electrode serving as a channel region of said device, said gate electrode having a gate voltage applied to induce a conductive channel through said first semiconductor region therebeneath; and wherein
- when said device is reverse-biased, a first depletion region extends from said fourth PN junction into said fourth semiconductor region and said semiconductor body, and a second depletion region extends from said fifth PN junction into said fifth semiconductor region and said fourth semiconductor region;
- said semiconductor body having a first ON resistance in a first current flow path therethrough between said second and third semiconductor regions, and said fifth semiconductor region providing a second ON resistance in a second current flow path along the surface of said semiconductor body from said second semiconductor region through said channel

and said fourth and fifth semiconductor regions to said third semiconductor region, so that said fifth semiconductor region serves to provide a current flow path in parallel with said first current flow path, thereby effectively reducing the total ON resistance of the overall current flow path between said second and third semiconductor regions.

2. A semiconductor device according to claim 1, wherein a peripheral edge of said gate electrode is aligned with a peripheral edge of said fifth semiconductor region.

3. A semiconductor device according to claim 1, wherein said fourth semiconductor region overlaps said first semiconductor region.

4. A semiconductor device according to claim 1, wherein the impurity concentration said fifth semiconductor region is such that said fifth semiconductor region is completely depleted by said second depletion region at a reverse bias less than that at which said first and second depletion regions come together within and punch through said fourth semiconductor region.

5. A semiconductor device comprising:

- a semiconductor body of a first conductivity type having a first surface;
- a first semiconductor region of a second conductivity type formed in a first portion of said first surface of said semiconductor body, and defining a first PN junction with said semiconductor body;
- a second semiconductor region of said first conductivity type formed in a surface portion of said first semiconductor region and defining therewith a second PN junction, said second PN junction being spaced apart from said first PN junction by material of said first semiconductor region therebetween;
- a third semiconductor region of said first conductivity type formed in a second surface portion of said semiconductor body, spaced apart from said first surface portion by a third surface portion thereof;
- a fourth semiconductor region of said second conductivity type formed in said third surface portion of said semiconductor body and defining with said semiconductor body a third PN junction, said fourth semiconductor region being connected to said first semiconductor region and being contiguous with said first and third semiconductor regions;
- a fifth semiconductor region of said first conductivity type, and having an impurity concentration greater than that of said semiconductor body, formed in said fourth semiconductor region and defining therewith a fourth PN junction, said fifth semiconductor region being contiguous with said first and third semiconductor regions;
- an insulator layer formed on said first surface of said semiconductor body; and
- a gate electrode formed on said insulator layer so as to overlie material of said first and fourth semiconductor regions, that portion of said first semiconductor region lying beneath said gate electrode serving as a channel region of said device, said gate electrode having a gate voltage applied to induce a conductive channel through said first semiconductor region therebeneath; and wherein
- when said device is reverse-biased, a first depletion region extends from said fourth PN junction into said fourth semiconductor region and said semiconductor body, and a second depletion region extends from said fifth PN junction into said fifth semiconductor

5,264,719

11

ductor region and said fourth semiconductor region.

6. A semiconductor device according to claim 5, wherein the impurity concentration said fifth semiconductor region is such that said fifth semiconductor region is completely depleted by said second depletion region at a reverse bias less than that at which said first and second depletion regions come together within and punch through said fourth semiconductor region.

7. A semiconductor device comprising:

- a semiconductor body of a first conductivity type having a first surface;
- a first semiconductor region of a second conductivity type formed in a first portion of said first surface of said semiconductor body, and defining a first PN junction with said semiconductor body;
- a second semiconductor region of said second conductivity type formed in a second surface portion of said semiconductor body, spaced apart from said first surface portion by a third surface portion thereof and defining a second PN junction with said semiconductor body;
- a third semiconductor region of said second conductivity type formed in a first surface part of said third surface portion of said semiconductor body spaced apart from said first surface portion of said semiconductor body by a second surface part of said third surface portion thereof and defining with said semiconductor body a third PN junction, said third semiconductor region being contiguous with said second semiconductor region;
- a fourth semiconductor region of said first conductivity type, and having an impurity concentration greater than that of said semiconductor body, formed in said third semiconductor region and defining therewith a fourth PN junction;
- an insulating layer formed on said first surface of said semiconductor body; and
- a gate electrode formed on said insulator layer so as to overlie said second surface part of said third surface portion of said semiconductor body, that portion of said semiconductor body lying beneath said gate electrode serving as a channel region of said device, said gate electrode being applied with a gate voltage for inducing a conductive channel through said channel region;

said device being reverse-biased, so that a first depletion region extends from said third PN junction into said third semiconductor region and said semiconductor body and a second depletion region extends from said fourth PN junction into said third semiconductor region and said fourth semiconductor region;

said semiconductor body having a first ON resistance in a first current flow path therethrough between said first and second semiconductor regions, and said fourth semiconductor region providing a second ON resistance, less than said first ON resistance, in a second current flow path along the surface of said semiconductor body from said first semiconductor region through said channel and said third and fourth semiconductor regions to said second semiconductor region, so that said fourth semiconductor region serves to provide a reduced resistance current flow path in parallel with said first current flow path, thereby effectively reducing the total ON resistance of the overall current

12

flow path between said first and second semiconductor regions; and

wherein the impurity concentration said fourth semiconductor region is such that said fourth semiconductor is completely depleted by said second depletion region at a reverse bias less than that at which said first and second depletion regions come together within and punch through said third semiconductor region.

8. A high voltage MOS transistor comprising:

- a semiconductor substrate of a first conductivity type having a surface,
- a pair of laterally spaced source and drain pockets of semiconductor material of a second conductivity type within the substrate and adjoining the substrate surface,
- an extended drain region of the second conductivity type extending laterally each way from said drain pocket to surface-adjoining positions,
- a surface adjoining, top layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain pocket and the surface-adjoining positions,
- said top layer of material and said substrate being subject to application of a reverse-bias voltage,
- an insulating layer on the surface of the substrate and covering at least that portion between the source pocket and the nearest surface-adjoining position of the extended drain region, and
- a gate electrode on the insulating layer and electrically isolated from the substrate region thereunder which forms a channel laterally between the source pocket and the nearest surface-adjoining position of the extended drain region, said gate electrode controlling by field-effect the flow of current thereunder through the channel.

9. A high voltage MOS transistor according to claim 8, wherein said extended drain region has an impurity concentration greater than $1 \times 10^{12} \text{ cm}^{-2}$.

10. A high voltage MOS transistor according to claim 8, further including an ohmic contact region of said first conductivity type formed in a surface adjoining portion of said semiconductor substrate, said ohmic contact region overlapping said top layer of material.

11. A high voltage MOS transistor comprising:

- semiconductor material of a first conductivity type having a surface,
- a pair of laterally spaced source and drain pockets of semiconductor material of a second conductivity type within the substrate and adjoining the surface of said semiconductor material,
- an extended drain region of the second conductivity type extending laterally from said drain pocket to a surface-adjoining position,
- a surface adjoining top layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain pocket and said surface-adjoining position,
- said top layer of material and said semiconductor material being subject to application of a reverse-bias voltage,
- an insulating layer on the surface of said semiconductor material and covering at least that portion between the source pocket and the nearest surface-adjoining position of the extended drain region, and
- a gate electrode on the insulating layer and electrically isolated from a semiconductor material re-

gion thereunder containing a channel that extends laterally between the source pocket and the nearest surface-adjointing position of the extended drain region, said gate electrode controlling by field-effect the flow of current thereunder through the channel.

12. A high voltage MOS transistor according to claim 11, wherein said extended drain region extends in a plurality of different directions from said drain pocket to respective plural surface adjoining positions.

13. A high voltage MOS transistor according to claim 11, wherein said extended drain region surrounds said drain pocket and extends to a surrounding surface adjoining position.

14. A high voltage MOS transistor according to claim 11, wherein said drain pocket comprises a first relatively deep pocket of a first impurity concentration and a second relatively shallow pocket formed in a surface portion of said first relatively deep pocket and having a second impurity concentration greater than said first impurity concentration and providing a drain contact region.

15. A high voltage MOS transistor according to claim 11, wherein said extended drain region has an impurity concentration greater than $1 \times 10^{12} \text{ cm}^{-2}$.

16. A high voltage MOS transistor according to claim 11, further including an ohmic contact region of said first conductivity type formed in a surface adjoining portion of said semiconductor material, said ohmic contact region overlapping said top layer of material.

17. A high voltage field effect transistor device comprising:

semiconductor material of a first conductivity type having a surface;

a source region of a second conductivity type formed in a first surface portion of said semiconductor material;

a drain region of said second conductivity type formed in a second surface portion of said semiconductor material spaced apart from said first surface portion by a third surface portion therebetween;

an extended drain region of said second conductivity type extending from said drain region beneath a first portion of said third surface portion of said semiconductor material, to adjoin a second portion of said third surface portion of said semiconductor material, spaced apart from said said second surface portion of said semiconductor material, by said first portion of said third surface portion of said semiconductor material;

a surface region of said first conductivity type formed in said first portion of said third surface portion of said semiconductor material;

an insulating layer disposed on said surface of said semiconductor material, so as to overlie a third portion of said third surface portion of said semiconductor material between the second portion of said third surface portion of said semiconductor material and said first surface portion of said semiconductor material; and

a gate electrode disposed on that portion of said insulating layer overlying said third portion of said third surface portion of said semiconductor material, and wherein said surface region and said semiconductor material are subject to the application of a reverse bias voltage.

18. A high voltage field effect transistor device according to claim 17, wherein said extended drain region

extends laterally in a plurality of different directions from said drain region to adjoin said second portion of said third surface portion of said semiconductor material and to adjoin a fifth surface portion of said semiconductor material.

19. A high voltage field effect transistor device according to claim 17, wherein said extended drain region surrounds said drain region and extends to a surrounding surface-adjointing portion of said semiconductor material.

20. A high voltage field effect transistor device according to claim 17, wherein said drain region comprises a first relatively deep region of a first impurity concentration and a second relatively shallow region formed in a surface portion of said first relatively deep region and having a second impurity concentration greater than said first impurity concentration and providing a drain contact region.

21. A high voltage field effect transistor device according to claim 17, wherein said extended drain region has an impurity concentration greater than $1 \times 10^{12} \text{ cm}^{-2}$.

22. A high voltage field effect transistor device according to claim 17, further including an ohmic contact region of said first conductivity type formed in a surface adjoining portion of said semiconductor material, said ohmic contact region overlapping said surface region.

23. An integrated MOS/JFET transistor device comprising an insulated gate field effect transistor and a double-sided junction field effect transistor integrated together in semiconductor substrate which contains a source region, and a drain region, and a dual channel path formed in said semiconductor material between said source and drain regions, said dual channel path comprising an insulated gate-controlled channel region having a first conductivity type in the presence of a channel-inducing gate voltage, said insulated gate-controlled channel region being contiguous with a double-sided junction channel region of said first conductivity type, and wherein said source region adjoins said insulated gate-controlled channel region and said drain region adjoins said double-sided channel region.

24. An integrated MOS/JFET transistor device according to claim 23, wherein said insulated gate-controlled channel region comprises a surface portion of said semiconductor material adjoining said source region, and wherein said double-sided junction channel region comprises an extended drain region extending laterally from said drain region beneath a top gate region to said surface portion of said semiconductor material, an underlying portion of said semiconductor material extending beneath and adjoining said extended drain region and forming a bottom gate, said top gate region and said bottom gate forming respective PN junctions with said double-sided junction channel region.

25. An integrated MOS/JFET transistor device according to claim 23, wherein said extended drain region and said double-sided junction channel region surround said drain region and extend to a surrounding surface-adjointing position.

26. An integrated MOS/JFET transistor device according to claim 23, wherein said extended drain region and said double, wherein said drain region comprises a first relatively deep region of a first impurity concentration and a second relatively shallow region formed in a surface portion of said first relatively deep region and having a second impurity concentration greater than

5,264,719

15

said first impurity concentration and providing a drain contact region.

27. An integrated MOS/JFET transistor device according to claim 23, wherein said extended drain region and said double, further including an ohmic contact region of said first conductivity type formed in a surface adjoining portion of said semiconductor material, said ohmic contact region overlapping said top gate.

28. An integrated MOS/JFET transistor device according to claim 23, wherein said extended drain region has an impurity concentration greater than $1 \times 10^{12} \text{ cm}^{-2}$.

29. A high voltage MOS transistor comprising: semiconductor material of a first conductivity type having a surface;

source and drain regions of a second conductivity type adjoining spaced apart portions of the surface of said semiconductor material;

an extended drain region of said second conductivity type extending laterally from said drain region through said semiconductor material to a surface-adjoining portion of the surface of said semiconductor material;

a top gate semiconductor layer of said first conductivity type adjoining said drain region and adjoining said extended drain region along the surface of said semiconductor material to said surface-adjoining portion of the surface of said semiconductor material, said top gate semiconductor layer and said semiconductor material being subject to the application of a reverse-bias voltage;

an insulating layer on the surface of the semiconductor material and covering at least that portion of the surface of said semiconductor material between said source region and said surface-adjoining portion of said extended drain region; and

a gate electrode disposed on said insulating layer and being electrically isolated from that portion of the surface of said semiconductor material thereunder which forms a channel laterally between said source region and said surface-adjoining portion of said extended drain region, said gate electrode controlling, by field-effect, the flow of current thereunder through said channel.

30. A high voltage MOS transistor according to claim 29, wherein said extended drain region extends laterally each way from said drain region to surface-adjoining portions of the surface of said semiconductor material, and wherein said top gate semiconductor layer extends laterally in a plurality of different directions from said drain region and adjoins said extended drain region along the surface of said semiconductor material to said surface-adjoining portions of the surface of said semiconductor material.

31. A high voltage MOS transistor according to claim 29, wherein said extended drain region surrounds said drain region and extends to a surrounding surface adjoining position.

32. A high voltage MOS transistor according to claim 29, wherein said drain region comprises a first relatively deep region of a first impurity concentration and a second relatively shallow region formed in a surface portion of said first relatively deep region and having a second impurity concentration greater than said first impurity concentration and providing a drain contact region.

33. A high voltage MOS transistor according to claim 29, wherein said extended drain region has an impurity concentration greater than $1 \times 10^{12} \text{ cm}^{-2}$.

34. A high voltage MOS transistor according to claim 29, further including an ohmic contact region of said

16

first conductivity type formed in a surface adjoining portion of said semiconductor material, said ohmic contact region overlapping said top gate layer.

35. A high voltage diode comprising:

semiconductor material of a first conductivity type having a surface,

a first, surface-adjoining region of a second conductivity type;

a second surface-adjoining region of said first conductivity type spaced apart from said first, surface-adjoining region;

a third region of said second conductivity type extending laterally from said first, surface-adjoining region; and

a fourth, surface-adjoining region of said first conductivity type overlying an intermediate portion of said third, laterally extending and surface-adjoining region.

36. A high voltage diode according to claim 35, wherein said third region surrounds said first, surface-adjoining region and extends to a surrounding surface adjoining position.

37. A high voltage diode according to claim 35, wherein said first region comprises a first relatively deep region of a first impurity concentration and a second relatively shallow region formed in a surface portion of said first relatively deep region and having a second impurity concentration greater than said first impurity concentration.

38. A high voltage diode according to claim 35, wherein said third region has an impurity concentration greater than $1 \times 10^{12} \text{ cm}^{-2}$.

39. A lateral bipolar transistor having a high voltage base-collector diode comprising:

semiconductor material of a first conductivity type having a surface and forming a base of said bipolar transistor,

a first, surface-adjoining collector region of a second conductivity type forming a base-collector junction with said semiconductor material;

a second surface-adjoining base region of said first conductivity type spaced apart from said first, surface-adjoining collector region;

a third, extended collector region of said second conductivity type extending laterally from said first, surface-adjoining collector region, so that said base-collector junction extends laterally from said first, surface adjoining collector region;

a fourth, surface-adjoining region of said first conductivity type overlying an intermediate portion of said third, laterally extending and surface-adjoining extended collector region; and

a fifth, surface-adjoining emitter region of said second conductivity type formed in said second surface-adjoining base region and defining therewith an emitter-base junction.

40. A lateral bipolar transistor according to claim 39, wherein said third region surrounds said first, surface-adjoining region and extends to a surrounding surface adjoining position.

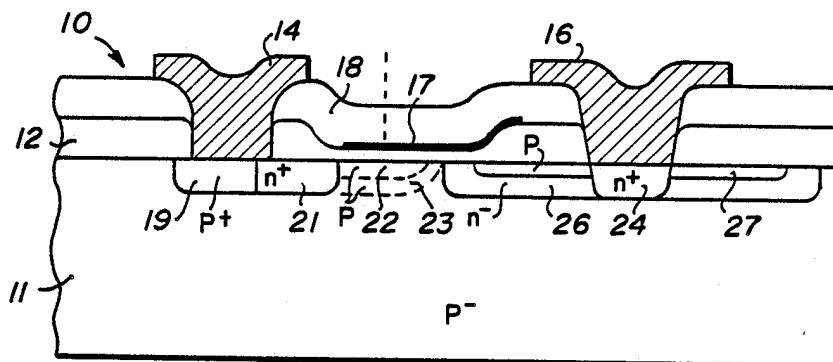
41. A lateral bipolar transistor according to claim 39, wherein said first region comprises a first relatively deep region of a first impurity concentration and a second relatively shallow region formed in a surface portion of said first relatively deep region and having a second impurity concentration greater than said first impurity concentration.

42. A lateral bipolar transistor according to claim 39, wherein said third, extended collector region has an impurity concentration greater than $1 \times 10^{12} \text{ cm}^{-2}$.

* * * * *

United States Patent [19]**Eklund**[11] **Patent Number:** **4,811,075**[45] **Date of Patent:** **Mar. 7, 1989**[54] **HIGH VOLTAGE MOS TRANSISTORS**[75] **Inventor:** **Klas H. Eklund**, Los Gatos, Calif.[73] **Assignee:** **Power Integrations, Inc.**, Mountain View, Calif.[21] **Appl. No.:** **41,994**[22] **Filed:** **Apr. 24, 1987**[51] **Int. Cl.⁴** **H01L 27/02; H01L 29/78; H01L 29/80**[52] **U.S. Cl.** **357/46; 357/22; 357/23.4; 357/23.8**[58] **Field of Search** **357/23.8, 23.4, 46, 357/22**[56] **References Cited****U.S. PATENT DOCUMENTS**4,626,879 12/1986 Colak 357/23.8
4,628,341 12/1986 Thomas 357/23.8**OTHER PUBLICATIONS**Sze, *Physics of Semiconductor Devices* Wiley & Sons
N.Y. c. 1981 pp. 431-438, 486-491.*Primary Examiner*—Andrew J. James*Assistant Examiner*—Jerome Jackson*Attorney, Agent, or Firm*—Thomas E. Schatzel[57] **ABSTRACT**

An insulated-gate, field-effect transistor and a double-sided, junction-gate field-effect transistor are connected in series on the same chip to form a high-voltage MOS transistor. An extended drain region is formed on top of a substrate of opposite conductivity-type material. A top layer of material having a conductivity-type opposite that of the extended drain and similar to that of the substrate is provided by ion-implantation through the same mask window as the extended drain region. This top layer covers only an intermediate portion of the extended drain which has ends contacting a silicon dioxide layer thereabove. The top layer is either connected to the substrate or left floating. Current flow through the extended drain region can be controlled by the substrate and the top layer, which act as gates providing field-effects for pinching off the extended drain region therebetween. A complementary pair of such high-voltage MOS transistors having opposite conductivity-type are provided on the same chip.

7 Claims, 2 Drawing Sheets

U.S. Patent

Mar. 7, 1989

Sheet 1 of 2

4,811,075

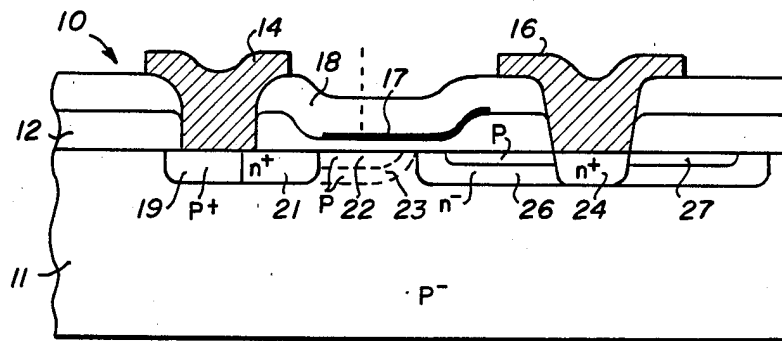


Fig. 1

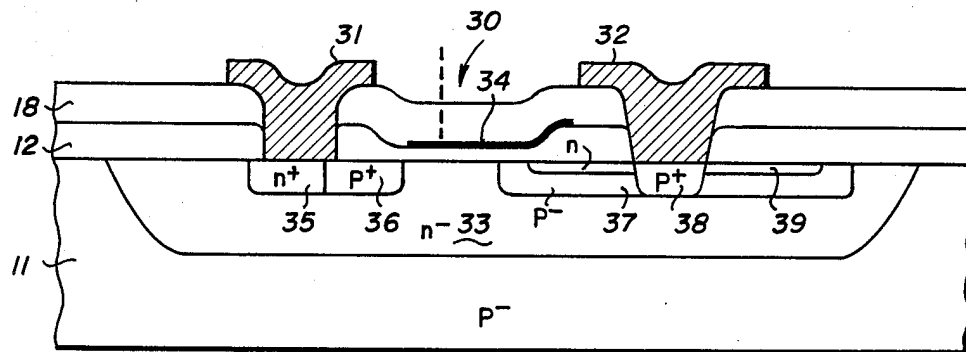


Fig. 2

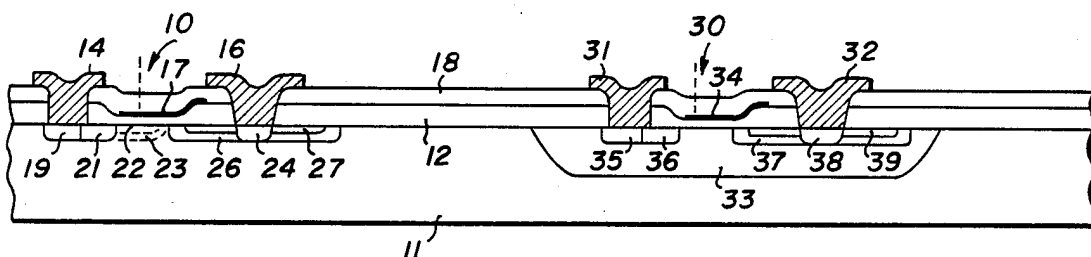


Fig. 3

U.S. Patent

Mar. 7, 1989

Sheet 2 of 2

4,811,075

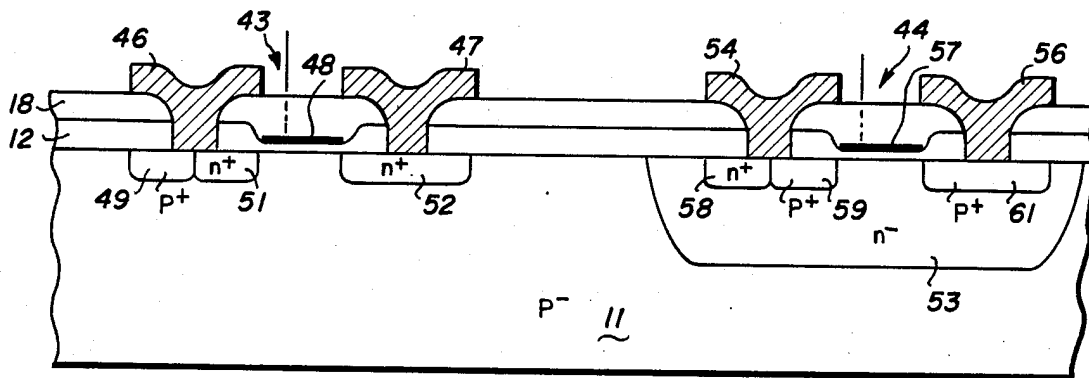


Fig. 4

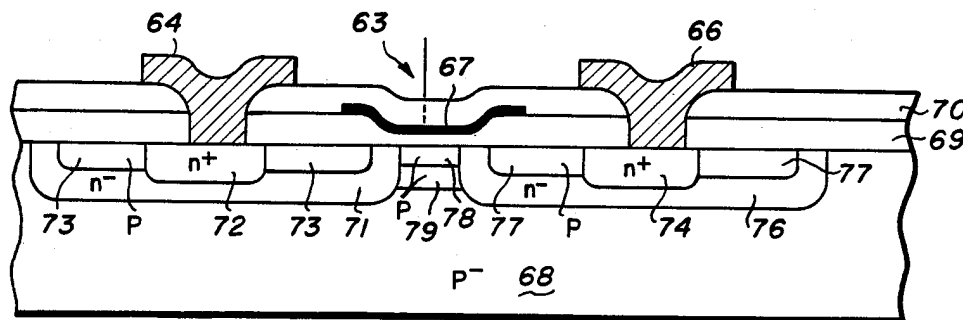


Fig. 5

4,811,075

1

HIGH VOLTAGE MOS TRANSISTORS

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates generally to high voltage metal-oxide semiconductor (MOS) transistors of the field-effect type. More specifically, the transistors can be made as either discrete or integrated devices of either n-channel or p-channel conductivity. The integrated devices can easily be combined with low voltage control logic on the same chip. Further devices of opposite conductivity can be combined in a complementary manner on the same chip.

2. Description of the Prior Art

Self isolation technology is used for making high voltage MOS devices, particularly integrated high voltage devices in combination with low voltage control logic on the same chip. The voltage is sustained by an offset gate, as a lightly doped extended drain region is used. Such devices can be considered as an IGFET or MOSFET in series with a single sided JFET. Two of such high voltage devices having opposite conductivity types can be used as a complementary pair on the same chip, with the device having an extended p-type drain being imbedded in an n-well in a p-substrate.

The voltage capability of such high voltage devices is determined by the doping of the substrate, the length of the extended drain region and the net number of charges therein. For optimum performance, the net number of charges should be around $1 \times 10^{12}/\text{cm}^2$. Such devices have been used for making display drivers in the one hundred to two hundred volt range, but the current capabilities of the devices are poor. The main advantage is that low voltage control logic easily can be combined on the same chip. For these devices, a general figure of merit can be determined by the product of $R_{on} \times A$ (where R_{on} is the on-resistance in the linear region and A is the area taken up by the device). For an n-channel device in the voltage range of two hundred fifty to three hundred volts, $R_{on} \times A$ is typically $10\text{--}15 \Omega \text{mm}^2$. A discrete vertical D-MOS device in the same voltage range has a figure of merit of $3 \Omega \text{mm}^2$, but is much more difficult to combine with low voltage control logic on the same chip. Thus, the application of these high voltage devices is restricted to current level below 100 mA, such as display drivers. Even such drivers are more costly due to poor area efficiency of the high voltage devices.

SUMMARY OF THE PRESENT INVENTION

An object of the present invention is to provide a more efficient high voltage MOS transistor.

Another object of the invention is to provide a high voltage MOS transistor that is compatible with five volt logic.

A further object of the invention is to provide a three hundred volt n-channel device with a figure of merit, $R_{on} \times A$, of about $2.0 \Omega \text{mm}^2$,

Briefly, the present invention includes an insulated gate, field-effect transistor (IGFET or MOSFET) and a double-sided junction gate field-effect transistor (JFET) connected in series on the same chip to form a high voltage MOS transistor. In a preferred embodiment of the invention, a complementary pair of such high voltage MOS transistors having opposite conductivity type are provided on the same chip.

2

Advantages of the invention include more efficient high voltage MOS transistors, compatibility with five volt logic, and for an n-channel device, voltage capability of three hundred volts with a figure of merit, $R_{on} \times A$, of about $2.0 \Omega \text{mm}^2$.

These and other objects and advantages of the present invention will no doubt become obvious to those of ordinary skill in the art after having read the following detailed description of the preferred embodiments which are illustrated in the various drawing figures.

IN THE DRAWINGS

FIG. 1 is a diagrammatic view of a high voltage MOS transistor of the n-channel type embodying the present invention.

FIG. 2 is a diagrammatic view of a high voltage MOS transistor of the p-channel type embodying the present invention.

FIG. 3 is a diagrammatic view of the transistors shown in FIGS. 1 and 2 forming a complementary pair on the same chip.

FIG. 4 is a diagrammatic view of low voltage, C-MOS implemented devices that can be combined on the same chip with the complementary pair of high voltage MOS transistors shown in FIG. 3.

FIG. 5 is a diagrammatic view of a symmetric high-voltage n-channel device wherein the source region and the drain region are similar.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Looking now at FIG. 1, an n-channel type, high voltage MOS transistor, indicated generally by reference numeral 10, is formed on a p-substrate 11 covered by a silicon dioxide layer 12. A metal source contact 14 and a metal drain contact 16 extend through the silicon dioxide layer to the substrate. A polysilicon gate 17 is positioned between the source contact and the drain contact at a location where the silicon dioxide layer is very thin so that the gate is slightly offset and insulated from the substrate. The polysilicon gate is the gate electrode, and an insulation layer 18 covers the gate and the silicon dioxide layer.

Beneath the source contact 14, a pocket 19 of p+ material and a pocket 21 of n+ material are diffused into the p-substrate 11. The pocket 21 extends from beneath the source contact to the gate 17. Beneath the gate is a threshold voltage implant 22 of p-type material for adjusting the threshold voltage and a punch through implant 23 of p-type material for avoiding punch through voltage breakdown. Beneath the drain contact 16, a pocket 24 of n+ material is diffused into the substrate. An extended drain region 26 of n-material is formed by diffusion or ion implantation on top of the p-substrate, and extends from beneath gate 17 to the pocket 24 and a similar distance to the opposite side of the pocket. A top layer 27 of p-material is provided by ion-implantation through the same mask window as the extended drain region to cover an intermediate portion thereof, while the end portions of the drain region are uncovered to contact the silicon dioxide layer 12. The top layer is either connected to the substrate or left floating.

The gate 17 controls by field-effect the current flow thereunder laterally through the p-type material to the n-type material in the extended drain region 26. Further flow through the extended drain region can be controlled by the substrate 11 and the top layer 27, which

4,811,075

3

act as gates providing field-effects for pinching off the extended drain region therebetween. Thus, the transistor 10 can be considered as an insulated gate, field-effect transistor (IGFET or MOSFET) connected in series with a double-sided, junction-gate field-effect transistor (JFET). While the insulated gate, field-effect transistor shown is a conventional MOS type, it should be understood that it could also be a lateral D-MOS or a depletion MOS type.

By adding the top layer 27 over the extended drain region 26 and connecting this top layer to the substrate 11, the net number of charges in the extended drain region can be increased from $1 \times 10^{12}/\text{cm}^2$ to around $2 \times 10^{12}/\text{cm}^2$, or approximately double. This drastically reduces the on-resistance of the transistor 10. The pinch off voltage of the extended drain region can be reduced from typically around forty volts to below ten volts. Thus, a conventional short channel, thin gate oxide MOS transistors can be used as the series transistor instead of a D-MOS device. This results in the following benefits. First, the threshold voltage of a conventional MOS transistor is typically much lower than for a D-MOS device (0.7 volts compared to two four volts for the D-MOS device) and thus, is directly compatible with five volt logic. The D-MOS device usually requires an additional power supply of ten to fifteen volts for driving the gate. Second, the conventional MOS transistor has less on resistance and thus, further reduces the total on resistance.

As the p-type top layer 27 can be made very shallow with a depth of one micron or less, the doping density in that layer will be in the range of 5×10^{16} – $1 \times 10^{17}/\text{cm}^3$. At doping levels above $10^{16}/\text{cm}^3$, the mobility starts to degrade and a decrease in mobility will increase the critical electrical field for breakdown, thus giving a higher breakdown voltage for fixed geometry. The number of charges in the top layer is around $1 \times 10^{12}/\text{cm}^2$ and to first order approximation independent of depth.

The combined benefits of the above features result in a voltage capability of three hundred volts with a figure of merit, $R_{on} \times A$, of about $2.0 \Omega \text{ mm}^2$ for the transistor 10. Currently used integrated MOS transistors have a figure of merit of about 10 – $15 \Omega \text{ mm}^2$, while the best discrete vertical D-MOS devices on the market in a similar voltage range have a figure of merit of 3 – $4 \Omega \text{ mm}^2$.

With reference to FIG. 2, a p-channel type, high voltage MOS transistor is indicated generally by reference numeral 30. Since the layers of substrate, silicon dioxide, and insulation for this transistor are similar to those previously described for transistor 10, they will be given like reference numerals. A p-substrate 11 is covered by a silicon dioxide layer 12 and an insulation layer 18. A metal source contact 31 and a metal drain contact 32 extend through the insulation layer and the silicon dioxide layer to an n-well 33 that is embedded in the substrate. A polysilicon gate 34, which is an electrode, is positioned between the source contact and the drain contact at a location where the silicon dioxide layer is very thin so that the gate is slightly offset and insulated from the n-well. The gate and the silicon dioxide layer are covered by the insulation layer 18.

A pocket 35 of n+ type material and a pocket 36 of p+ type material are provided in the n-well 33 beneath the metal source contact 31. The pocket 36 extends to the gate 34. An extended drain region 37 of p-type material is formed in the n-well and extends from be-

4

neath the gate to a pocket 38 located beneath the drain contact 32, and the extended drain region continues a similar distance on the opposite side of the drain contact. A top layer 39 of n-material is provided by ion-implantation through the same window of the mask as the extended drain region to cover an intermediate portion thereof. The end portions of the extended drain region are uncovered so as to contact the silicon dioxide layer 12. The top layer is either connected to the n-well or left floating.

The gate 34 controls by field-effect the current flow thereunder laterally through the n-type material to the p-type material in the extended drain region 37. Further flow through the extended drain region can be controlled by the n-well 33 and the top layer 39, which act as gates providing field-effects for pinching off the extended drain region therebetween. Thus, the transistor 30 can be considered as an insulated-gate field-effect transistor (IGFET or MOSFET) connected in series with a double-sided, junction-gate field-effect transistor (JFET). The n-well under the extended drain region has to be depleted before breakdown occurs between the p+ drain contact pocket 38 and the n-well.

Looking now at FIG. 3, an n-channel transistor 10, similar to that shown in FIG. 1, and a p-channel transistor 30, similar to that shown in FIG. 2, are shown as a complementary pair on the same substrate 11 and isolated from each other. Since the details of each transistor has been previously described with reference to FIGS. 1 and 2, no further description is considered necessary.

As shown in FIG. 4, low voltage, C-MOS implemented devices 43 and 44 can be combined on the same p-substrate 11 as the high voltage devices 10 and 30, shown in FIG. 3. These low voltage devices enable low voltage logic and analog function to control the high voltage devices. The device 43 is an n-channel type having a source contact 46, a drain contact 47 and a polysilicon gate 48. A p+ pocket 49 and an n+ pocket 51 are provided in the p- substrate beneath the source contact. The n+ pocket extends to beneath the gate. An n+ pocket 52 is provided beneath the drain contact. The gate 48 is insulated from the substrate by the silicon dioxide layer 12, but the gate controls the current flow through the substrate between pockets 51 and 52. The gate is covered by the insulation layer 18. An n-well 53 is provided in the substrate to accommodate the low voltage, p-channel device 44. This device includes a source contact 54, a drain contact 56 and a polysilicon gate 57. An n+ pocket 58 and a p+ pocket 59 are provided in the n-well beneath the source contact and a p+ pocket 61 is provided in the n-well beneath the drain contact. The gate 57 is insulated from the n-well and extends thereabove between pockets 59 and 61.

It should be noted that the term "substrate" refers to the physical material on which a microcircuit is fabricated. If a transistor is fabricated on a well of n or p type material within a primary substrate of opposite type material, the well material can be considered a secondary substrate. Similarly, if a transistor is fabricated on an epitaxial layer or spi-island that merely supports and insulates the transistor, the epitaxial layer or epi-island can be considered a secondary substrate. An epi-island is a portion of an epitaxial layer of one conductivity type that is isolated from the remaining portion of the epitaxial layer by diffusion pockets of an opposite conductivity type. When complimentary transistors are formed on the same chip, the well in which one compli-

4,811,075

5

mentary transistor is embedded is formed by the same diffusion as the extended drain region for the other transistor.

FIG. 5 shows a symmetrical n-channel device 63 having a source contact 64 and a drain contact 66. A polysilicon gate 67 is insulated from a substrate 68 by a silicon dioxide layer 69 and the gate is covered by an insulation layer 20. An n-type extended source region 71 is provided beneath the source contact and an n+ type pocket 72. A top layer 73 of p-type material is positioned over an intermediate portion of the extended source region, while the end portions of the extended source region contact the silicon dioxide layer thereabove. Beneath the drain contact is an n+ type pocket 74 and an n-type extended drain region 76. A top layer 73 of p-type material is positioned over an intermediate portion of the extended drain region and end portions of the extended drain region contact the silicon dioxide layer. An implant 78 of the p-type material is provided under the gate 67 between the extended source region and the extended drain region for sustaining the threshold voltage. A similar implant 79 for sustaining the punch-through voltage is provided beneath the implant 78. Since the symmetrical channel device has both an extended source and an extended drain, the source can sustain the same high potential as the drain. A symmetric p-channel device could be made in a similar way using opposite conductivity type materials.

From the foregoing description, it will be seen that an efficient, high voltage MOS transistor has been provided. This transistor is compatible with five volt logic which easily can be integrated on the same chip. The transistor has a voltage capability of three hundred volts for an n-channel device, and has a figure of merit, $R_{on} \times A$, of about $2.0 \Omega \text{mm}^2$. The transistor is formed by an insulated-gate field-effect transistor and a double-sided junction-gate field-effect transistor connected in series on the same chip. These transistors can be made as either discrete devices or integrated devices of either n-channel or p-channel conductivity. The integrated devices can be easily combined with low voltage control logic on the same chip. Further devices of opposite conductivity can be combined in a complementary manner on the same chip.

Although the present invention has been described in terms of the presently preferred embodiment, it is to be understood that such disclosure is not to be interpreted as limiting. Various alterations and modifications will no doubt become apparent to those of ordinary skill in the art after having read the above disclosure. Accordingly, it is intended that the appended claims be interpreted as covering all alterations and modifications as fall within the true spirit and scope of the invention.

I claim:

1. A high voltage MOS transistor comprising:
 - a semiconductor substrate of a first conductivity type having a surface
 - a pair of laterally spaced pockets of semiconductor material of a second conductivity type within the substrate and adjoining the substrate surface,
 - a source contact connected to one pocket,
 - a drain contact connected to the other pocket,
 - an extended drain region of the second conductivity type extending laterally each way from the drain contact pocket to surface-adjoining positions,
 - a surface adjoining layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain contact pocket and the surface-adjoining positions,

6

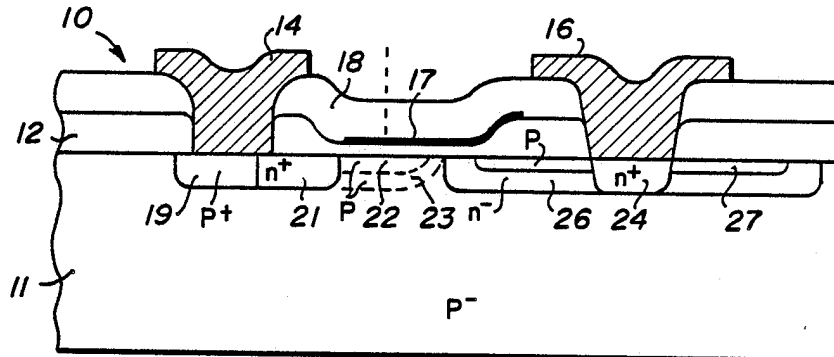
said top layer of material and said substrate being subject to application of a reverse-bias voltage, an insulating layer on the surface of the substrate and covering at least that portion between the source contact pocket and the nearest surface-adjoining position of the extended drain region, and a gate electrode on the insulating layer and electrically isolated from the substrate region thereunder which forms a channel laterally between the source contact pocket and the nearest surface-adjoining position of the extended drain region, said gate electrode controlling by field-effect the flow of current thereunder through the channel.

2. The high-voltage MOS transistor of claim 1 wherein, said top layer has a depth of one micron or less.
3. The high-voltage MOS transistor of claim 1 wherein, said top layer has a doping density higher than $5 \times 10^{16}/\text{cm}^3$ so that the mobility starts to degrade.
4. The high voltage MOS transistor of claim 1 having one channel conductivity type in combination with a complementary high voltage MOS transistor of an opposite channel conductivity type combined on the same chip and isolated from each other.
5. The high voltage MOS transistor of claim 1 combined on the same chip with a low voltage CMOS implemented device.
6. The combination of claim 5 further including, a complementary high voltage MOS transistor, and a complementary low voltage CMOS implemented device on the same chip and isolated from each other.
7. A high voltage MOS transistor comprising:
 - a semiconductor substrate of a first conductivity type having a surface,
 - a pair of laterally spaced pockets of semiconductor material of a second conductivity type within the substrate and adjoining the substrate surface,
 - a source contact connected to one pocket,
 - an extended source region of the second conductivity type extending laterally each way from the source contact pocket to surface-adjoining positions,
 - a surface adjoining layer of material of the first conductivity type on top of an intermediate portion of the extended source region between the surface-adjoining positions,
 - said top layer and said substrate being subject to application of a reverse-bias voltage,
 - a drain contact connected to the other pocket,
 - an extended drain region of the second conductivity type extending laterally each way from the drain contact pocket to surface-adjoining positions,
 - a surface adjoining layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain contact pocket and the surface-adjoining positions,
 - said top layer of material and said substrate being subject to application of a reverse-bias voltage,
 - an insulating layer on the surface of the substrate and covering at least that portion between the nearest surface-adjoining positions of the extended source region and the extended drain region, and
 - a gate electrode on the insulating layer and electrically isolated from the substrate region thereunder which forms a channel laterally between the nearest surface-adjoining positions of the extended source region and the extended drain region, said gate electrode controlling by field-effect the current flow thereunder through the channel.

* * * * *

United States Patent [19]**Eklund**[11] **Patent Number:** **4,811,075**[45] **Date of Patent:** **Mar. 7, 1989**[54] **HIGH VOLTAGE MOS TRANSISTORS**[75] **Inventor:** **Klas H. Eklund**, Los Gatos, Calif.[73] **Assignee:** **Power Integrations, Inc.**, Mountain View, Calif.[21] **Appl. No.:** **41,994**[22] **Filed:** **Apr. 24, 1987**[51] **Int. Cl.⁴** **H01L 27/02; H01L 29/78; H01L 29/80**[52] **U.S. Cl.** **357/46; 357/22; 357/23.4; 357/23.8**[58] **Field of Search** **357/23.8, 23.4, 46, 357/22**[56] **References Cited****U.S. PATENT DOCUMENTS**4,626,879 12/1986 Colak 357/23.8
4,628,341 12/1986 Thomas 357/23.8**OTHER PUBLICATIONS**Sze, *Physics of Semiconductor Devices* Wiley & Sons
N.Y. c. 1981 pp. 431-438, 486-491.*Primary Examiner*—Andrew J. James*Assistant Examiner*—Jerome Jackson*Attorney, Agent, or Firm*—Thomas E. Schatzel[57] **ABSTRACT**

An insulated-gate, field-effect transistor and a double-sided, junction-gate field-effect transistor are connected in series on the same chip to form a high-voltage MOS transistor. An extended drain region is formed on top of a substrate of opposite conductivity-type material. A top layer of material having a conductivity-type opposite that of the extended drain and similar to that of the substrate is provided by ion-implantation through the same mask window as the extended drain region. This top layer covers only an intermediate portion of the extended drain which has ends contacting a silicon dioxide layer thereabove. The top layer is either connected to the substrate or left floating. Current flow through the extended drain region can be controlled by the substrate and the top layer, which act as gates providing field-effects for pinching off the extended drain region therebetween. A complementary pair of such high-voltage MOS transistors having opposite conductivity-type are provided on the same chip.

7 Claims, 2 Drawing Sheets

U.S. Patent

Mar. 7, 1989

Sheet 1 of 2

4,811,075

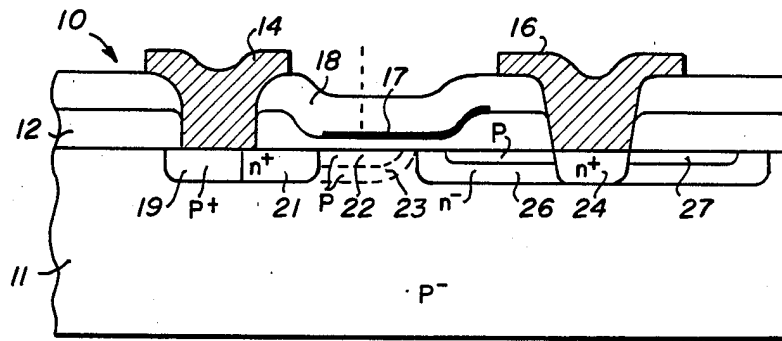


Fig. 1

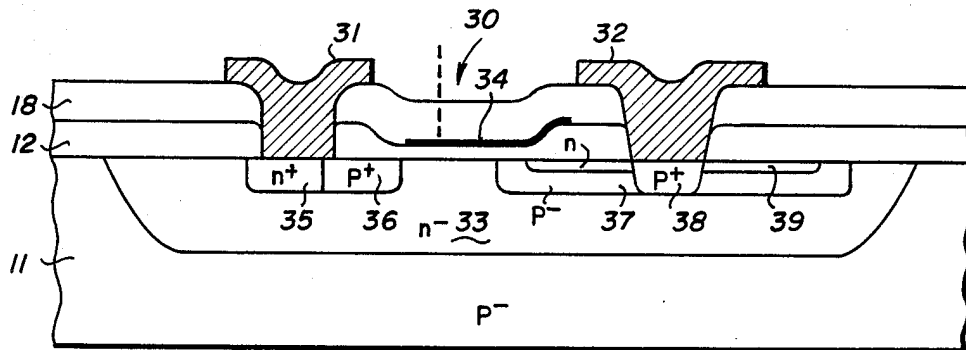


Fig. 2

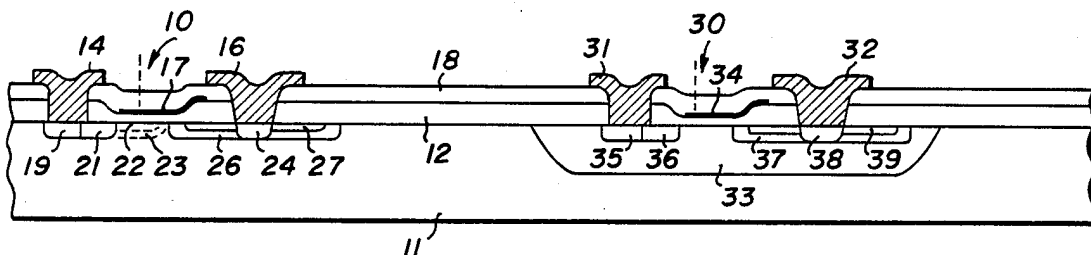


Fig. 3

U.S. Patent

Mar. 7, 1989

Sheet 2 of 2

4,811,075

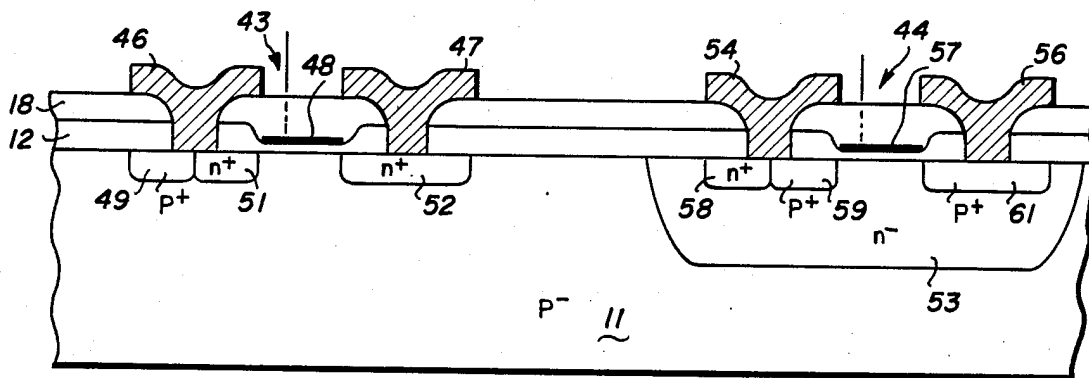


Fig.4

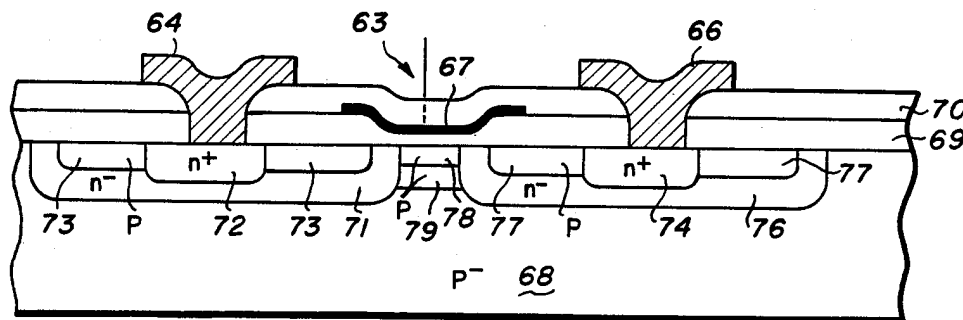


Fig.5

4,811,075

1

HIGH VOLTAGE MOS TRANSISTORS

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates generally to high voltage metal-oxide semiconductor (MOS) transistors of the field-effect type. More specifically, the transistors can be made as either discrete or integrated devices of either n-channel or p-channel conductivity. The integrated devices can easily be combined with low voltage control logic on the same chip. Further devices of opposite conductivity can be combined in a complementary manner on the same chip.

2. Description of the Prior Art

Self isolation technology is used for making high voltage MOS devices, particularly integrated high voltage devices in combination with low voltage control logic on the same chip. The voltage is sustained by an offset gate, as a lightly doped extended drain region is used. Such devices can be considered as an IGFET or MOSFET in series with a single sided JFET. Two of such high voltage devices having opposite conductivity types can be used as a complementary pair on the same chip, with the device having an extended p-type drain being imbedded in an n-well in a p-substrate.

The voltage capability of such high voltage devices is determined by the doping of the substrate, the length of the extended drain region and the net number of charges therein. For optimum performance, the net number of charges should be around $1 \times 10^{12}/\text{cm}^2$. Such devices have been used for making display drivers in the one hundred to two hundred volt range, but the current capabilities of the devices are poor. The main advantage is that low voltage control logic easily can be combined on the same chip. For these devices, a general figure of merit can be determined by the product of $R_{on} \times A$ (where R_{on} is the on-resistance in the linear region and A is the area taken up by the device). For an n-channel device in the voltage range of two hundred fifty to three hundred volts, $R_{on} \times A$ is typically $10\text{--}15 \Omega \text{mm}^2$. A discrete vertical D-MOS device in the same voltage range has a figure of merit of $3 \Omega \text{mm}^2$, but is much more difficult to combine with low voltage control logic on the same chip. Thus, the application of these high voltage devices is restricted to current level below 100 mA, such as display drivers. Even such drivers are more costly due to poor area efficiency of the high voltage devices.

SUMMARY OF THE PRESENT INVENTION

An object of the present invention is to provide a more efficient high voltage MOS transistor.

Another object of the invention is to provide a high voltage MOS transistor that is compatible with five volt logic.

A further object of the invention is to provide a three hundred volt n-channel device with a figure of merit, $R_{on} \times A$, of about $2.0 \Omega \text{mm}^2$.

Briefly, the present invention includes an insulated gate, field-effect transistor (IGFET or MOSFET) and a double-sided junction gate field-effect transistor (JFET) connected in series on the same chip to form a high voltage MOS transistor. In a preferred embodiment of the invention, a complementary pair of such high voltage MOS transistors having opposite conductivity type are provided on the same chip.

2

Advantages of the invention include more efficient high voltage MOS transistors, compatibility with five volt logic, and for an n-channel device, voltage capability of three hundred volts with a figure of merit, $R_{on} \times A$, of about $2.0 \Omega \text{mm}^2$.

These and other objects and advantages of the present invention will no doubt become obvious to those of ordinary skill in the art after having read the following detailed description of the preferred embodiments which are illustrated in the various drawing figures.

IN THE DRAWINGS

FIG. 1 is a diagrammatic view of a high voltage MOS transistor of the n-channel type embodying the present invention.

FIG. 2 is a diagrammatic view of a high voltage MOS transistor of the p-channel type embodying the present invention.

FIG. 3 is a diagrammatic view of the transistors shown in FIGS. 1 and 2 forming a complementary pair on the same chip.

FIG. 4 is a diagrammatic view of low voltage, C-MOS implemented devices that can be combined on the same chip with the complementary pair of high voltage MOS transistors shown in FIG. 3.

FIG. 5 is a diagrammatic view of a symmetric high-voltage n-channel device wherein the source region and the drain region are similar.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Looking now at FIG. 1, an n-channel type, high voltage MOS transistor, indicated generally by reference numeral 10, is formed on a p-substrate 11 covered by a silicon dioxide layer 12. A metal source contact 14 and a metal drain contact 16 extend through the silicon dioxide layer to the substrate. A polysilicon gate 17 is positioned between the source contact and the drain contact at a location where the silicon dioxide layer is very thin so that the gate is slightly offset and insulated from the substrate. The polysilicon gate is the gate electrode, and an insulation layer 18 covers the gate and the silicon dioxide layer.

Beneath the source contact 14, a pocket 19 of p+ material and a pocket 21 of n+ material are diffused into the p-substrate 11. The pocket 21 extends from beneath the source contact to the gate 17. Beneath the gate is a threshold voltage implant 22 of p-type material for adjusting the threshold voltage and a punch through implant 23 of p-type material for avoiding punch through voltage breakdown. Beneath the drain contact 16, a pocket 24 of n+ material is diffused into the substrate. An extended drain region 26 of n-material is formed by diffusion or ion implantation on top of the p-substrate, and extends from beneath gate 17 to the pocket 24 and a similar distance to the opposite side of the pocket. A top layer 27 of p-material is provided by ion-implantation through the same mask window as the extended drain region to cover an intermediate portion thereof, while the end portions of the drain region are uncovered to contact the silicon dioxide layer 12. The top layer is either connected to the substrate or left floating.

The gate 17 controls by field-effect the current flow thereunder laterally through the p-type material to the n-type material in the extended drain region 26. Further flow through the extended drain region can be controlled by the substrate 11 and the top layer 27, which

4,811,075

3

act as gates providing field-effects for pinching off the extended drain region therebetween. Thus, the transistor 10 can be considered as an insulated gate, field-effect transistor (IGFET or MOSFET) connected in series with a double-sided, junction-gate field-effect transistor (JFET). While the insulated gate, field-effect transistor shown is a conventional MOS type, it should be understood that it could also be a lateral D-MOS or a depletion MOS type.

By adding the top layer 27 over the extended drain region 26 and connecting this top layer to the substrate 11, the net number of charges in the extended drain region can be increased from $1 \times 10^{12}/\text{cm}^2$ to around $2 \times 10^{12}/\text{cm}^2$, or approximately double. This drastically reduces the on-resistance of the transistor 10. The pinch off voltage of the extended drain region can be reduced from typically around forty volts to below ten volts. Thus, a conventional short channel, thin gate oxide MOS transistors can be used as the series transistor instead of a D-MOS device. This results in the following benefits. First, the threshold voltage of a conventional MOS transistor is typically much lower than for a D-MOS device (0.7 volts compared to two four volts for the D-MOS device) and thus, is directly compatible with five volt logic. The D-MOS device usually requires an additional power supply of ten to fifteen volts for driving the gate. Second, the conventional MOS transistor has less on resistance and thus, further reduces the total on resistance.

As the p-type top layer 27 can be made very shallow with a depth of one micron or less, the doping density in that layer will be in the range of 5×10^{16} – $1 \times 10^{17}/\text{cm}^3$. At doping levels above $10^{16}/\text{cm}^3$, the mobility starts to degrade and a decrease in mobility will increase the critical electrical field for breakdown, thus giving a higher breakdown voltage for fixed geometry. The number of charges in the top layer is around $1 \times 10^{12}/\text{cm}^2$ and to first order approximation independent of depth.

The combined benefits of the above features result in a voltage capability of three hundred volts with a figure of merit, $R_{on} \times A$, of about $2.0 \Omega \text{ mm}^2$ for the transistor 10. Currently used integrated MOS transistors have a figure of merit of about 10 – $15 \Omega \text{ mm}^2$, while the best discrete vertical D-MOS devices on the market in a similar voltage range have a figure of merit of 3 – $4 \Omega \text{ mm}^2$.

With reference to FIG. 2, a p-channel type, high voltage MOS transistor is indicated generally by reference numeral 30. Since the layers of substrate, silicon dioxide, and insulation for this transistor are similar to those previously described for transistor 10, they will be given like reference numerals. A p-substrate 11 is covered by a silicon dioxide layer 12 and an insulation layer 18. A metal source contact 31 and a metal drain contact 32 extend through the insulation layer and the silicon dioxide layer to an n-well 33 that is embedded in the substrate. A polysilicon gate 34, which is an electrode, is positioned between the source contact and the drain contact at a location where the silicon dioxide layer is very thin so that the gate is slightly offset and insulated from the n-well. The gate and the silicon dioxide layer are covered by the insulation layer 18.

A pocket 35 of n+ type material and a pocket 36 of p+ type material are provided in the n-well 33 beneath the metal source contact 31. The pocket 36 extends to the gate 34. An extended drain region 37 of p-type material is formed in the n-well and extends from be-

4

neath the gate to a pocket 38 located beneath the drain contact 32, and the extended drain region continues a similar distance on the opposite side of the drain contact. A top layer 39 of n-material is provided by ion-implantation through the same window of the mask as the extended drain region to cover an intermediate portion thereof. The end portions of the extended drain region are uncovered so as to contact the silicon dioxide layer 12. The top layer is either connected to the n-well or left floating.

The gate 34 controls by field-effect the current flow thereunder laterally through the n-type material to the p-type material in the extended drain region 37. Further flow through the extended drain region can be controlled by the n-well 33 and the top layer 39, which act as gates providing field-effects for pinching off the extended drain region therebetween. Thus, the transistor 30 can be considered as an insulated-gate field-effect transistor (IGFET or MOSFET) connected in series with a double-sided, junction-gate field-effect transistor (JFET). The n-well under the extended drain region has to be depleted before breakdown occurs between the p+ drain contact pocket 38 and the n-well.

Looking now at FIG. 3, an n-channel transistor 10, similar to that shown in FIG. 1, and a p-channel transistor 30, similar to that shown in FIG. 2, are shown as a complementary pair on the same substrate 11 and isolated from each other. Since the details of each transistor has been previously described with reference to FIGS. 1 and 2, no further description is considered necessary.

As shown in FIG. 4, low voltage, C-MOS implemented devices 43 and 44 can be combined on the same p-substrate 11 as the high voltage devices 10 and 30, shown in FIG. 3. These low voltage devices enable low voltage logic and analog function to control the high voltage devices. The device 43 is an n-channel type having a source contact 46, a drain contact 47 and a polysilicon gate 48. A p+ pocket 49 and an n+ pocket 51 are provided in the p- substrate beneath the source contact. The n+ pocket extends to beneath the gate. An n+ pocket 52 is provided beneath the drain contact. The gate 48 is insulated from the substrate by the silicon dioxide layer 12, but the gate controls the current flow through the substrate between pockets 51 and 52. The gate is covered by the insulation layer 18. An n-well 53 is provided in the substrate to accommodate the low voltage, p-channel device 44. This device includes a source contact 54, a drain contact 56 and a polysilicon gate 57. An n+ pocket 58 and a p+ pocket 59 are provided in the n-well beneath the source contact and a p+ pocket 61 is provided in the n-well beneath the drain contact. The gate 57 is insulated from the n-well and extends thereabove between pockets 59 and 61.

It should be noted that the term "substrate" refers to the physical material on which a microcircuit is fabricated. If a transistor is fabricated on a well of n or p type material within a primary substrate of opposite type material, the well material can be considered a secondary substrate. Similarly, if a transistor is fabricated on an epitaxial layer or spi-island that merely supports and insulates the transistor, the epitaxial layer or epi-island can be considered a secondary substrate. An epi-island is a portion of an epitaxial layer of one conductivity type that is isolated from the remaining portion of the epitaxial layer by diffusion pockets of an opposite conductivity type. When complimentary transistors are formed on the same chip, the well in which one compli-

4,811,075

5

mentary transistor is embedded is formed by the same diffusion as the extended drain region for the other transistor.

FIG. 5 shows a symmetrical n-channel device 63 having a source contact 64 and a drain contact 66. A polysilicon gate 67 is insulated from a substrate 68 by a silicon dioxide layer 69 and the gate is covered by an insulation layer 20. An n-type extended source region 71 is provided beneath the source contact and an n+ type pocket 72. A top layer 73 of p-type material is positioned over an intermediate portion of the extended source region, while the end portions of the extended source region contact the silicon dioxide layer thereabove. Beneath the drain contact is an n+ type pocket 74 and an n-type extended drain region 76. A top layer 73 of p-type material is positioned over an intermediate portion of the extended drain region and end portions of the extended drain region contact the silicon dioxide layer. An implant 78 of the p-type material is provided under the gate 67 between the extended source region and the extended drain region for sustaining the threshold voltage. A similar implant 79 for sustaining the punch-through voltage is provided beneath the implant 78. Since the symmetrical channel device has both an extended source and an extended drain, the source can sustain the same high potential as the drain. A symmetric p-channel device could be made in a similar way using opposite conductivity type materials.

From the foregoing description, it will be seen that an efficient, high voltage MOS transistor has been provided. This transistor is compatible with five volt logic which easily can be integrated on the same chip. The transistor has a voltage capability of three hundred volts for an n-channel device, and has a figure of merit, $R_{on} \times A$, of about $2.0 \Omega \text{mm}^2$. The transistor is formed by an insulated-gate field-effect transistor and a double-sided junction-gate field-effect transistor connected in series on the same chip. These transistors can be made as either discrete devices or integrated devices of either n-channel or p-channel conductivity. The integrated devices can be easily combined with low voltage control logic on the same chip. Further devices of opposite conductivity can be combined in a complementary manner on the same chip.

Although the present invention has been described in terms of the presently preferred embodiment, it is to be understood that such disclosure is not to be interpreted as limiting. Various alterations and modifications will no doubt become apparent to those of ordinary skill in the art after having read the above disclosure. Accordingly, it is intended that the appended claims be interpreted as covering all alterations and modifications as fall within the true spirit and scope of the invention.

I claim:

1. A high voltage MOS transistor comprising:
 - a semiconductor substrate of a first conductivity type having a surface
 - a pair of laterally spaced pockets of semiconductor material of a second conductivity type within the substrate and adjoining the substrate surface,
 - a source contact connected to one pocket,
 - a drain contact connected to the other pocket,
 - an extended drain region of the second conductivity type extending laterally each way from the drain contact pocket to surface-adjoining positions,
 - a surface adjoining layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain contact pocket and the surface-adjoining positions,

6

said top layer of material and said substrate being subject to application of a reverse-bias voltage, an insulating layer on the surface of the substrate and covering at least that portion between the source contact pocket and the nearest surface-adjoining position of the extended drain region, and a gate electrode on the insulating layer and electrically isolated from the substrate region thereunder which forms a channel laterally between the source contact pocket and the nearest surface-adjoining position of the extended drain region, said gate electrode controlling by field-effect the flow of current thereunder through the channel.

2. The high-voltage MOS transistor of claim 1 wherein,
 - said top layer has a depth of one micron or less.
3. The high-voltage MOS transistor of claim 1 wherein,
 - said top layer has a doping density higher than $5 \times 10^{16}/\text{cm}^3$ so that the mobility starts to degrade.
4. The high voltage MOS transistor of claim 1 having one channel conductivity type in combination with a complementary high voltage MOS transistor of an opposite channel conductivity type combined on the same chip and isolated from each other.
5. The high voltage MOS transistor of claim 1 combined on the same chip with a low voltage CMOS implemented device.
6. The combination of claim 5 further including,
 - a complementary high voltage MOS transistor, and
 - a complementary low voltage CMOS implemented device on the same chip and isolated from each other.
7. A high voltage MOS transistor comprising:
 - a semiconductor substrate of a first conductivity type having a surface,
 - a pair of laterally spaced pockets of semiconductor material of a second conductivity type within the substrate and adjoining the substrate surface,
 - a source contact connected to one pocket,
 - an extended source region of the second conductivity type extending laterally each way from the source contact pocket to surface-adjoining positions,
 - a surface adjoining layer of material of the first conductivity type on top of an intermediate portion of the extended source region between the surface-adjoining positions,
 - said top layer and said substrate being subject to application of a reverse-bias voltage,
 - a drain contact connected to the other pocket,
 - an extended drain region of the second conductivity type extending laterally each way from the drain contact pocket to surface-adjoining positions,
 - a surface adjoining layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain contact pocket and the surface-adjoining positions,
 - said top layer of material and said substrate being subject to application of a reverse-bias voltage,
 - an insulating layer on the surface of the substrate and covering at least that portion between the nearest surface-adjoining positions of the extended source region and the extended drain region, and
 - a gate electrode on the insulating layer and electrically isolated from the substrate region thereunder which forms a channel laterally between the nearest surface-adjoining positions of the extended source region and the extended drain region, said gate electrode controlling by field-effect the current flow thereunder through the channel.

* * * * *

Appendix 1 – Side-by-side comparison of the '719 and '075 patents.

'719 Patent claim 8

8. A high voltage MOS transistor comprising:
 a semiconductor substrate of a first conductivity type having a surface,
 a pair of laterally spaced source and drain pockets of semiconductor material of a second conductivity type within the substrate and adjoining the substrate surface,
 an extended drain region of the second conductivity type extending laterally each way from said drain pocket to surface-adjoining positions,
 a surface adjoining, top layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain pocket and the surface-adjoining positions,
 said top layer of material and said substrate being subject to application of a reverse-bias voltage,
 an insulating layer on the surface of the substrate and covering at least that portion between the source pocket and the nearest surface-adjoining position of the extended drain region, and
 a gate electrode on the insulating layer and electrically isolated from the substrate region thereunder which forms a channel laterally between the source pocket and the nearest surface-adjoining position of the extended drain region, said gate electrode controlling by field-effect the flow of current thereunder through the channel.

'075 Patent claim 1

1. A high voltage MOS transistor comprising:
 a semiconductor substrate of a first conductivity type having a surface
 a pair of laterally spaced pockets of semiconductor material of a second conductivity type within the substrate and adjoining the substrate surface,
 a source contact connected to one pocket,
 a drain contact connected to the other pocket,
 an extended drain region of the second conductivity type extending laterally each way from the drain contact pocket to surface-adjoining positions,
 a surface adjoining layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain contact pocket and the surface-adjoining positions,
 said top layer of material and said substrate being subject to application of a reverse-bias voltage,
 an insulating layer on the surface of the substrate and covering at least that portion between the source contact pocket and the nearest surface-adjoining position of the extended drain region, and
 a gate electrode on the insulating layer and electrically isolated from the substrate region thereunder which forms a channel laterally between the source contact pocket and the nearest surface-adjoining position of the extended drain region, said gate electrode controlling by field-effect the flow of current thereunder through the channel.

UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

FAIRCHILD SEMICONDUCTOR
CORPORATION, a Delaware corporation,
and INTERSIL CORPORATION, a
Delaware corporation,

Plaintiffs,

v.

POWER INTEGRATIONS, INC., a
Delaware corporation,

Defendants.

C.A. No. 2:06-CV-151 (TJW)

ORDER GRANTING POWER INTEGRATIONS' MOTION TO DISMISS

ON THIS DAY, came on to be considered Power Integrations, Inc.'s Motion to Dismiss, or in the Alternative, to Transfer This Case to Delaware in the above-styled and numbered cause. After considering said motion, the Court is of the opinion that said motion should be GRANTED, and that all matters in this suit against Power Integrations, Inc. are dismissed with prejudice.

IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS

FAIRCHILD SEMICONDUCTOR
CORPORATION, a Delaware corporation,
INTERSIL AMERICAS, INC., a Delaware
corporation and INTERSIL CORPORATION,
a Delaware corporation

Plaintiff,

v.

POWER INTEGRATIONS, INC., a Delaware
corporation,

Defendants.

CIVIL ACTION NO. 2:06-cv-151

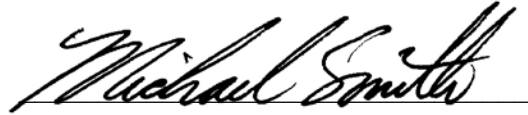
**FAIRCHILD'S UNOPPOSED MOTION TO EXTEND TIME TO RESPOND TO
POWER INTEGRATIONS' MOTION TO DISMISS OR TRANSFER**

COMES NOW Plaintiff Fairchild Semiconductor Corp. ("Fairchild") and moves for an extension of time to file its opposition to Power Integrations' Motion to Dismiss or, in the Alternative, to Transfer This Case to Delaware.

Fairchild's opposition brief is currently due on July 5, 2006. Fairchild has requested that Power Integrations stipulate to an extension until July 26, 2006 for Fairchild to file its opposition brief. Power Integrations has so stipulated and does not oppose the instant motion. All other briefing dates regarding Power Integrations' motion are governed by the Civil Local Rules.

For the foregoing reasons, Fairchild respectfully requests that the Court grant this unopposed motion and enter the proposed order submitted herewith setting July 26, 2006 as the date upon which Fairchild's opposition to Power Integrations' motion to dismiss or transfer will be due and ordering that all other briefing dates will be governed by the Civil Local Rules.

Respectfully submitted by,

A handwritten signature in black ink, appearing to read "Michael C. Smith", written over a horizontal line.

ORRICK, HERRINGTON & SUTCLIFFE LLP
G. Hopkins Guy, III (SBN 124811)
Bas de Blank (SBN 191487)
1000 Marsh Road
Menlo Park, CA 94025
(650) 614-7400

Carl R. Roth, Texas Bar No. 901984225
cr@rothfirm.com
Michael C. Smith, Texas Bar No. 900641877
ms@rothfirm.com
THE ROTH LAW FIRM, P.C.
115 North Wellington, Suite 200
P.O. Box 876
Marshall, Texas 75671
Tel: (903) 935-1665
Fax: (903) 935-1797

Attorneys for Plaintiffs,
FAIRCHILD SEMICONDUCTOR
CORPORATION, INTERSIL CORPORATION,
and INTERSIL AMERICAS, INC.

CERTIFICATE OF CONFERENCE

Counsel for Fairchild has conferred with counsel for Power Integrations regarding the relief sought in the instant motion. Power Integrations does not oppose the extension sought by Fairchild.


Michael C. Smith

CERTIFICATE OF SERVICE

The undersigned hereby certifies that all counsel of record who are deemed to have consented to electronic service are being served with a copy of this document via the Court's CM/ECF system per Local Rule CV-5(a)(3) this 5th day of July, 2006. Any other counsel of record will be served by facsimile transmission and/or first class mail.


Michael C. Smith

IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS

FAIRCHILD SEMICONDUCTOR
CORPORATION, a Delaware corporation,
INTERSIL AMERICAS, INC., a Delaware
corporation and INTERSIL CORPORATION,
a Delaware corporation

Plaintiff,

v.

POWER INTEGRATIONS, INC., a Delaware
corporation,

Defendants.

CIVIL ACTION NO. 2:06-cv-151

ORDER

CAME ON TO BE CONSIDERED Fairchild's Unopposed Motion To Extend Time To Respond To Power Integrations' Motion To Dismiss Or Transfer from July 5, 2006 until and including July 26, 2006.

After consideration, the Court finds that the Motion should be GRANTED. It is therefore ORDERED that Fairchild's deadline to oppose Power Integrations' Motion to Dismiss or Transfer is extended from July 5, 2006 until and including July 26, 2006. All other briefing dates regarding Power Integrations' motion shall be governed by the Civil Local Rules.

**IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION**

**FAIRCHILD SEMICONDUCTOR,
CORPORATION, a Delaware
Corporation, INTERSIL AMERICAS,
INC., a Delaware Corporation, and
INTERFIL CORPORATION, a Delaware
Corporation,**

Plaintiffs,

V.

**POWER INTEGRATIONS, INC., a
Delaware Corporation,**

Defendant.

[illegible]

CIVIL ACTION No. 2:06-cv-151 TWJ

NOTICE OF APPEARANCE

The following designated attorneys hereby enter an appearance as additional counsel of record for Plaintiffs Intersil Americas, Inc. and Intersil Corporation, and are authorized to receive service on all pleadings, notices, orders and other papers in the above-captioned matter on behalf of Plaintiffs.

Michael W. Shore
State Bar No. 18294915
Jeffrey R. Bragalone
State Bar No. 02855775
Joseph F. DePumpo
State Bar No. 00787355
SHORE CHAN BRAGALONE, LLP
325 N. St. Paul Street, Suite 4450
Dallas, Texas 75201
(214) 593-9110
(214) 593-9111 fax
mshore@shorechan.com
jbragalone@shorechan.com
jdepumpo@shorechan.com

Dated: July 7, 2006.

Respectfully Submitted,

s/Joseph F. DePumpo

Michael W. Shore, State Bar No. 18294915
Jeffrey R. Bragalone, State Bar No. 02855775
Joseph F. DePumpo, State Bar No. 00787355
SHORE CHAN BRAGALONE, LLP
Republic Center
325 N. St. Paul Street, Suite 4450
Dallas, Texas 75201
214.743.4170
214.743.4179 (FAX)

ATTORNEYS FOR
INTERSIL AMERICAS, INC., and
INTERSIL CORPORATION

Carl R. Roth, State Bar No. 901984225
Michael C. Smith, State Bar No. 900641877
THE ROTH LAW FIRM, P.C.
115 North Wellington, Suite 200
P.O. Box 876
Marshall, Texas 75671
(903) 935-1665
(903) 935-1797 fax

G. Hopkins Guy, III, Calif. SBN 124811
Vickie Feeman, Calif. SBN 191487
Bas de Blank, Calif. SBN 191487
Brian Vander Zanden, Calif. SBN 233134
ORRICK, HERRINGTON & SUTCLIFFE LLP
1000 Marsh Road
Menlo Park, California 94025
(650) 614-7400
(650) 614-7401 fax

CERTIFICATE OF SERVICE

I hereby certify that all counsel of record who are deemed to have consented to electronic service are being served with a copy of this document via the Court's CM/ECF system per Local Rule CV-5(a)(3) on this 7th day of July, 2006. Any other counsel of record will be served by facsimile transmission and/or first class mail.

s/Joseph F. DePumpo
Joseph F. DePumpo

**IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION**

**FAIRCHILD SEMICONDUCTOR,
CORPORATION, a Delaware
Corporation, INTERSIL AMERICAS,
INC., a Delaware Corporation, and
INTERASIL CORPORATION, a Delaware
Corporation,**

Plaintiffs,

V.

**POWER INTEGRATIONS, INC., a
Delaware Corporation,**

Defendant.

NOTICE OF APPEARANCE

The following designated attorneys hereby enter an appearance as additional counsel of record for Plaintiffs Intersil Americas, Inc. and Intersil Corporation, and are authorized to receive service on all pleadings, notices, orders and other papers in the above-captioned matter on behalf of Plaintiffs.

Michael W. Shore
State Bar No. 18294915
Jeffrey R. Bragalone
State Bar No. 02855775
Joseph F. DePumpo
State Bar No. 00787355
SHORE CHAN BRAGALONE, LLP
325 N. St. Paul Street, Suite 4450
Dallas, Texas 75201
(214) 593-9110
(214) 593-9111 fax
mshore@shorechan.com
jbragalone@shorechan.com
jdepumpo@shorechan.com

Dated: July 10, 2006.

Respectfully Submitted,

s/Jeffrey R. Bragalone

Michael W. Shore, State Bar No. 18294915
Jeffrey R. Bragalone, State Bar No. 02855775
Joseph F. DePumpo, State Bar No. 00787355
SHORE CHAN BRAGALONE, LLP
Republic Center
325 N. St. Paul Street, Suite 4450
Dallas, Texas 75201
214.743.4170
214.743.4179 (FAX)

ATTORNEYS FOR
INTERSIL AMERICAS, INC., and
INTERSIL CORPORATION

Carl R. Roth, State Bar No. 901984225
Michael C. Smith, State Bar No. 900641877
THE ROTH LAW FIRM, P.C.
115 North Wellington, Suite 200
P.O. Box 876
Marshall, Texas 75671
(903) 935-1665
(903) 935-1797 fax

G. Hopkins Guy, III, Calif. SBN 124811
Vickie Feeman, Calif. SBN 191487
Bas de Blank, Calif. SBN 191487
Brian Vander Zanden, Calif. SBN 233134
ORRICK, HERRINGTON & SUTCLIFFE LLP
1000 Marsh Road
Menlo Park, California 94025
(650) 614-7400
(650) 614-7401 fax

CERTIFICATE OF SERVICE

I hereby certify that all counsel of record who are deemed to have consented to electronic service are being served with a copy of this document via the Court's CM/ECF system per Local Rule CV-5(a)(3) on this 10th day of July, 2006. Any other counsel of record will be served by facsimile transmission and/or first class mail.

s/Jeffrey R. Bragalone
Jeffrey R. Bragalone

IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS

FAIRCHILD SEMICONDUCTOR
CORPORATION, a Delaware corporation,
INTERSIL AMERICAS, INC., a Delaware
corporation and INTERSIL CORPORATION,
a Delaware corporation

Plaintiff,

v.

POWER INTEGRATIONS, INC., a Delaware
corporation,

Defendants.

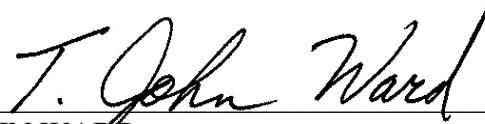
CIVIL ACTION NO. 2:06-cv-151

ORDER

CAME ON TO BE CONSIDERED Fairchild's Unopposed Motion To Extend Time To Respond To Power Integrations' Motion To Dismiss Or Transfer from July 5, 2006 until and including July 26, 2006.

After consideration, the Court finds that the Motion should be GRANTED. It is therefore ORDERED that Fairchild's deadline to oppose Power Integrations' Motion to Dismiss or Transfer is extended from July 5, 2006 until and including July 26, 2006. All other briefing dates regarding Power Integrations' motion shall be governed by the Civil Local Rules.

SIGNED this 7th day of July, 2006.



T. JOHN WARD
UNITED STATES DISTRICT JUDGE

**IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION**

**FAIRCHILD SEMICONDUCTOR,
CORPORATION, a Delaware
Corporation, INTERSIL AMERICAS,
INC., a Delaware Corporation, and
INTERASIL CORPORATION, a Delaware
Corporation,**

Plaintiffs,

V.

**POWER INTEGRATIONS, INC., a
Delaware Corporation,**

Defendant.

CIVIL ACTION No. 2:06-cv-151 TWJ

NOTICE OF APPEARANCE

The following designated attorneys hereby enter an appearance as additional counsel of record for Plaintiffs Intersil Americas, Inc. and Intersil Corporation, and are authorized to receive service on all pleadings, notices, orders and other papers in the above-captioned matter on behalf of Plaintiffs.

Michael W. Shore
State Bar No. 18294915
Jeffrey R. Bragalone
State Bar No. 02855775
Joseph F. DePumpo
State Bar No. 00787355
SHORE CHAN BRAGALONE, LLP
325 N. St. Paul Street, Suite 4450
Dallas, Texas 75201
(214) 593-9110
(214) 593-9111 fax
mshore@shorechan.com
jbragalone@shorechan.com
jdepumpo@shorechan.com

Dated: July 14, 2006.

Respectfully Submitted,

s/Michael W. Shore

Michael W. Shore, State Bar No. 18294915
Jeffrey R. Bragalone, State Bar No. 02855775
Joseph F. DePumpo, State Bar No. 00787355
SHORE CHAN BRAGALONE, LLP
Republic Center
325 N. St. Paul Street, Suite 4450
Dallas, Texas 75201
214.743.4170
214.743.4179 (FAX)

ATTORNEYS FOR
INTERSIL AMERICAS, INC., and
INTERSIL CORPORATION

Carl R. Roth, State Bar No. 901984225
Michael C. Smith, State Bar No. 900641877
THE ROTH LAW FIRM, P.C.
115 North Wellington, Suite 200
P.O. Box 876
Marshall, Texas 75671
(903) 935-1665
(903) 935-1797 fax

G. Hopkins Guy, III, Calif. SBN 124811
Vickie Feeman, Calif. SBN 191487
Bas de Blank, Calif. SBN 191487
Brian Vander Zanden, Calif. SBN 233134
ORRICK, HERRINGTON & SUTCLIFFE LLP
1000 Marsh Road
Menlo Park, California 94025
(650) 614-7400
(650) 614-7401 fax

CERTIFICATE OF SERVICE

I hereby certify that all counsel of record who are deemed to have consented to electronic service are being served with a copy of this document via the Court's CM/ECF system per Local Rule CV-5(a)(3) on this 14th day of July, 2006. Any other counsel of record will be served by facsimile transmission and/or first class mail.

s/Michael W. Shore
Michael W. Shore

IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

FAIRCHILD SEMICONDUCTOR
CORPORATION, a Delaware corporation,
INTERSIL AMERICAS, INC., a Delaware
corporation and INTERSIL CORPORATION,
a Delaware corporation

Plaintiff,

v.

POWER INTEGRATIONS, INC., a Delaware
corporation,

Defendants.

CIVIL ACTION NO. 2:06-cv-151

**OPPOSITION TO MOTION TO DISMISS OR, IN THE ALTERNATIVE, TO
TRANSFER THIS CASE TO DELAWARE**

COME NOW the Plaintiffs and file this their response to Defendant Power Integrations' ("PI") request to dismiss this action or transfer it to Delaware, and in support thereof would show the Court the following.

I. INTRODUCTION

Plaintiff "Intersil"¹ is the owner of the patent-in-suit, U.S. Patent No. 5,264,719 (the "'719 Patent"), and Fairchild Semiconductor Corp. ("Fairchild"), is the exclusive licensee of that patent. While Defendant PI moves to dismiss the action, it does not even contend that plaintiff Intersil lacks standing. For this reason alone, the motion to dismiss must be denied. PI also simply ignores the clear language of the license agreement between Intersil and Fairchild explicitly granting Fairchild exclusive rights. Pursuant to that agreement, Fairchild has complete power to exclude PI from practicing the '719 Patent and therefore has standing to sue as a co-plaintiff with Intersil. PI's motion to dismiss must be denied for this reason as well.

Further, this case should not be transferred to Delaware. The parties in the two pending actions are not the same, as Intersil is not party to the Delaware dispute. The actions do not even

¹ Intersil Americas and Intersil Corp.

involve the same patents or products. This case involves Intersil's and Fairchild's '719 Patent, and the accused products are PI devices. In the Delaware action, by contrast, PI asserts four of its own patents against Fairchild devices. Obviously there is no overlap. Moreover, the Delaware action has been pending for close to two years and in just a few months, trial on the four PI patents at issue in Delaware will be underway. Thus, consolidation of the two actions would not be practical, given the disparate stages of litigation. There is no reason to transfer this distinct action to Delaware when the dispute can and should be litigated efficiently in this venue.

II. ARGUMENT

A. PI's Motion To Dismiss Should Be Denied.

1. Dismissal Of The Action Is Inappropriate Because PI Does Not Dispute That Intersil—The Owner Of The '719 Patent—Is Properly A Plaintiff

PI does not contest that Plaintiff Intersil—the patent owner—has standing to sue. PI admits that Intersil is the owner of the '719 Patent. [PI Brief, at 5 (“[l]egal title appears to have been held at all times by Intersil (or Intersil’s predecessor Harris Corporation) . . .”); Ramsey Decl. (filed herewith), Exs. 1-3] Further, PI recognizes that, as the owner of the asserted patent, Intersil has standing. [PI Brief, at 5 (“a patentee may bring an action for patent infringement”)] This point is well-settled. *See* 35 U.S.C. §281 (“patentee” may bring infringement action). Nowhere in its brief does PI even remotely contest Intersil’s status as a plaintiff in this case. Yet, despite this critical concession, PI nonetheless requests dismissal of the *entire* action with prejudice. [PI Brief, at 7; PI Proposed Order] Given PI’s recognition that Intersil has standing, such relief is entirely inappropriate. For this reason alone, PI’s motion must be denied.

2. Fairchild Has Standing To Sue Because It Is An Exclusive Licensee And Has Sued Jointly With Intersil

Fairchild is an exclusive licensee, therefore it has standing to sue along with Intersil as a joint plaintiff. It is well-settled that “a licensee may possess sufficient interest in the patent to have standing to sue as a co-plaintiff with the patentee.” *Rite-Hite Corp. v. Kelley Co.*, 56 F.3d 1538, 1552 (Fed. Cir. 1995). Such a licensee “is *usually* an ‘exclusive licensee.’” *Id.* (emphasis

added). Exclusive licensees possessing “all substantial rights”² under the patents may sue even without joining the patentee. Exclusive licensees possessing less than “all substantial rights” may sue as long as the patentee is joined as a co-plaintiff. See *Prima Tek II, LLC v. A-Roo Co.*, 222 F.3d 1372, 1377, 1381 (Fed. Cir. 2000) (“the patent owner must ordinarily join, in any infringement action, an exclusive licensee who possesses less than all substantial rights in the patent.”); *Abbott Lab. v. Diamedix Corp.*, 47 F.3d 1128, 1132-1133 (Fed. Cir. 1995) (establishing licensee standing to sue if patentee joined as plaintiff by licensee); *Philadelphia Brief Case Co. v. Specialty Leather Prods. Co.*, 145 F. Supp. 425, 429 (D. N.J. 1956) (same).

PI egregiously misstates this standard asserting that a licensee may *only* sue when “a party obtains an exclusive license to a patent and holds ‘all substantial rights’ under the patent.” [PI Brief, at 4, 7, 10-11] While this is the appropriate standard for determining whether an exclusive licensee may sue *without* joining the patentee—it is not the appropriate test for whether a licensee may sue *with* the patentee. Even if less than “all substantial rights” under the patent are held by the exclusive licensee, it may sue as co-plaintiff with the patentee.

The critical question in determining whether Fairchild has standing in a suit brought with Intersil is whether Fairchild obtained the “the right to exclude others [i.e. PI] from making, using or selling the patented invention . . .” *Rite-Hite Corp.*, 56 F.3d at 1552. In the words of one case relied upon by PI, “it is the licensee’s beneficial ownership of a right to prevent others from making, using or selling the patented technology that provides the foundation for co-plaintiff standing . . .” *Ortho Pharma. Corp. v. Genetics Institute, Inc.*, 52 F.3d 1026, 1032 (Fed. Cir. 1995); see also *Abbott Lab.*, 47 F.3d at 1131 (relied upon by PI; “the transfer of the exclusive right to sue was ‘particularly dispositive’ of the question whether [plaintiff] was authorized to bring suit without joining [patentee]”); *Good Sportsman Mktg. LLC v. Testa Assocs., LLC*, 2005 U.S. Dist. LEXIS 29182, *4-5 (E.D. Tex. 2005) (same).

² “All substantial rights” means: “the right to exclude others from making, using, or selling the invention in the United States, the right to transfer, and the right to sue.” *NOMOS Corp. v. ZMED, Inc.*, 175 F. Supp. 2d 96, 98 (D. Mass. 2001). An exclusive licensee receiving “all substantial rights” is tantamount to an assignee.

There can be no dispute that Fairchild possesses the exclusive right to exclude PI from making, using or selling the patented invention of the ‘719 Patent, and therefore has standing to sue as a co-plaintiff with Intersil. Pursuant to its license agreement with Intersil, Fairchild possesses the “sole and exclusive right” to prevent PI from making, using or selling the invention and to control PI’s economic activity regarding practice of the invention. [Ramsey Decl., Ex. 4 at ¶1.2, ¶3)] This right to exclude is complete, as is clear from the patent license agreement:

3.1. . . . Intersil grants to Fairchild the sole and exclusive right, exclusive even as to Intersil, to enforce the Patents against POWI³, to assert, litigate and prosecute claims of Infringement under the Patents against POWI, including without limitation in any U.S. federal court or before the International Trade Commission, and to seek all equitable, injunctive, monetary and other relief and to collect for later distribution under Paragraph 1.2 any and all past damages in connection with Infringement of the Patents by POWI, and to settle and compromise any disputes with POWI related to the Patents. Except as provided herein, the Parties agree that only Fairchild shall have the authority to threaten, commence, maintain or settle any claim suit or proceeding based upon Infringement of the Patents (or other trespass or similar action relating to the Patents and the inventions therein claimed) by POWI.

[Ramsey Decl., Ex. 4 at ¶3)]

By this agreement, Intersil has clearly promised that no party other than Fairchild will be granted the right to exclude PI from practicing the patent “even as to Intersil.” Fairchild possesses two of the three “substantial rights”—specifically, “the right to exclude others from making, using, or selling the invention in the United States,” and “the right to sue.” *NOMOS Corp. v. ZMED, Inc.*, 175 F. Supp. 2d 96, 98 (D. Mass. 2001). Therefore, Fairchild is an exclusive licensee, upon which standing is conferred to sue PI jointly with the patent owner Intersil. PI incorrectly argues that Fairchild purportedly “has no exclusive right to keep others from making, using or selling products making use of the patented technology.” [PI Brief at 6] As the foregoing makes clear, this disingenuous assertion must be rejected.

PI incorrectly relies on a number of cases in which the licensee failed to join the patent owner as a co-plaintiff. See *Crown Die & Tool Co. v. Nye Tool & Machine Works*, 261 U.S. 24, 40, 44 (1923) (“The plaintiff below could not bring such a suit for past infringements without

³ Power Integrations (“POWI”)

joining with it the owner of the patent when the infringements were committed.”; dismissing on the ground that “the owner of the patent is not a party to this bill. . .”); *Abbott Lab.*, 47 F.3d at 1132-1133 (licensee failed to join patentee as voluntary plaintiff); *Prima Tek II, LLC*, 222 F.3d at 1376, 1381-1382 (same; issue was “whether any of the Appellees in this suit had standing to maintain an infringement action . . . without joining . . . the owner of all six patents in suit.”); *Philadelphia Brief Case Co.*, 145 F. Supp. at 429-430 (same). By contrast, the facts are fundamentally different here, given that the patentee Intersil is obviously joined as a co-plaintiff with exclusive licensee Fairchild. Thus, under the foregoing authority, standing is appropriate.

PI also makes a flawed attempt to rely on authority stating that a non-exclusive “right to sue” clause does not provide standing. *See e.g. Ortho*, 52 F.3d at 1034. However, the transfer of exclusive rights in this case far exceeds the mere non-exclusive “right to sue” at issue in the authority cited by PI. Indeed, Intersil granted Fairchild the complete and exclusive right to prevent PI from making, using or selling the patented invention, even as to Intersil. Fairchild has the right, with respect to PI, to “enforce the Patents,” “to assert, litigate and prosecute claims of Infringement under the Patents” in any context, “to seek all equitable, injunctive, monetary and other relief” to “collect . . . any and all past damages,” “to settle and compromise any disputes” with PI that are “related to the Patents,” and “to threaten, commence, maintain or settle any claim, suit or proceeding based upon Infringement of the Patents.” [Ramsey Decl., Ex. 4 (Patent License Agreement, ¶3)] In other words, Fairchild has the complete right to exclude PI from practicing the ‘719 Patent and to control PI’s activity involving practice of the invention. This is true “even as to Intersil.” It is not merely the right to sue, but the right to exclude in every respect within a particular domain—i.e. the domain of PI’s practice of the invention. This constitutes a transfer of “beneficial ownership of some of the patentee’s proprietary rights,” which indisputably confers standing. *Ortho*, 52 F.3d at 1034.⁴ For these reasons Intersil and

⁴ Similarly, a number of cases relied upon by PI are distinguishable because the patentee retained the same right as was purportedly granted exclusively to the licensee. *See e.g. Ortho*, 52 F.3d at 1033-34 (patentee retained the same “exclusive” rights licensed to the licensee); *Rite-Hite Corp.*, 56 F.3d at 1552-1553 (not even clear that patent rights were being licensed, licensee had “no right . . . to exclude anyone from making, using, or selling the claimed invention” and patentee

Fairchild have standing to sue, and PI's motion to dismiss should be denied.

As admitted by PI, Intersil was, until March 30, 2006, the owner of all rights in the '719 Patent. At that time, Intersil transferred to Fairchild the right to exclude PI and completely control its activity regarding the '719 Patent. This was true "even as to Intersil." Rhetorically, PI's logic would mean that Intersil and Fairchild have no standing to sue or enforce the patent. Intersil could not independently sue PI without Fairchild, since it transferred to Fairchild the sole and exclusive rights to enforce the patent against PI. At the same time, Fairchild could proceed alone, but case law suggests that the better course is to join the patent owner. *Prima Tek II, L.L.C.*, 222 F.3d at 1381 (underlying policy of joinder rule is to prevent duplicative litigation by rights holders against a single accused infringer). Essentially, PI's logic would result in somehow granting PI freedom from suit since neither the owner nor the exclusive licensee would have standing to sue. This is obviously not the law. Joinder of the patent owner and exclusive licensee affords standing to both to proceed against a defendant.

B. The Court Should Not Transfer This Case To Delaware

PI's request to transfer this case to the District of Delaware should also be denied. This case involves entirely different parties and issues than are involved in the pending Delaware action. Transferring the case to Delaware would be contrary to the interests of justice and efficiency. Therefore, pursuant to 28 U.S.C. §1404(a), PI's motion should be denied and this case should proceed in this Court.

1. The Parties And Issues Before The Delaware Court Are Substantially Different Than The Parties And Issues Involved In The Instant Case

Contrary to PI's assertions, there is not substantial overlap between the instant matter and the case pending in the District of Delaware. First, the parties are completely different. PI brought the Delaware action against Fairchild Semiconductor Int'l, Inc and Fairchild

retained the same rights it had licensed). By contrast, here Intersil has granted Fairchild the exclusive right to prevent PI from making, using or selling the patented invention, Intersil has not retained those rights for itself and it cannot license any other party to do the same. [Ramsey Decl., Ex. 4 at ¶3] The fact that Intersil retained the right to sue other parties unrelated to PI is of no consequence to the question of whether Fairchild has standing to sue PI, which it clearly does.

Semiconductor Corp. The instant action, by contrast, is brought by Intersil and Fairchild Semiconductor Corp. against PI. Thus, Intersil is not a party to the Delaware action and Fairchild Semiconductor Int'l, Inc. is not a party to the instant action. [Ramsey Decl., Exs. 6, 7]

Moreover, there is no significant overlap of issues between the two actions. In the Delaware action, PI asserts U.S. Patent Nos. 6,107,851, 6,249,876, 6,229,366 and 4,811,075 against two different Fairchild entities and there are no other patents asserted by any party in the counterclaims. [*Id.*, Exs. 8, 9] By contrast, in the instant case, Intersil and Fairchild Semiconductor Corp. have sued PI for infringement of a completely different patent—the ‘719 Patent. [*Id.*, Ex. 7] Obviously, none of the patents-in-suit overlap between the cases. Such distinct patents, with distinct claim language and specifications, require independent determinations of claim construction, infringement and validity. *See e.g. ResQnet.com, Inc. v. LANSA, Inc.*, 3f46 F.3d 1374, 1384 (Fed. Cir. 2003) (independent claim construction required for different patents, even where language was similar).⁵ Further, because different defendants are involved in the two actions, completely different products are alleged to infringe. Therefore, the jury trial in the Delaware action that will occur in October and December of this year will resolve only issues concerning the four PI patents asserted in that case, but will *not* resolve any issues concerning construction, infringement, validity or enforceability of the ‘719 Patent asserted in the instant action.

PI does not even contend that the Delaware action involves infringement of the ‘719 Patent. However, it concocts an outlandish argument that somehow the validity of the ‘719 Patent will be addressed in the Delaware action. This is untrue. The issues at stake in the

⁵ PI attempts to argue that the cases substantially overlap based on the mere fact that a single claim of the ‘719 Patent uses most of the same wording as is used in one of the patents in suit in Delaware—Patent No. 4,811,075. [PI Brief, at 8, 11, Michael E. Jones Decl., Ex. H] However, the claim language is not identical. Given that the claim language, specifications and file histories are different between the patents, the precise scope of the claims necessarily must be determined independently. *See Datamize, Inc. v. Fid. Brokerage Servs., LLC*, 2004 U.S. Dist. LEXIS 29100, *17-18 (E.D. Tex. 2004). Even where patents in two actions had identical specifications and similar language, no “substantial overlap” of issues was found and transfer was denied. *Id.* The Court observed that: “the Federal Circuit has held that where there are even small differences in the language of claims in related patents, the claim language in each patent should be construed independently.” *Id.*

Delaware action are the infringement, validity and enforceability of *PI*'s patents, including U.S. Patent 4,811,075 with respect to which the '719 Patent is cited as prior art. [Ramsey Decl., Ex. 7, 8] The Delaware action will *not* involve any findings regarding the validity or enforceability of the '719 Patent, as no complaint, answer or counterclaim in that action asserts infringement of the '719 Patent. [*Id.*] In fact, the Delaware court is without jurisdiction to decide the validity or enforceability of the '719 Patent. *See Flexi-Mat Corp. v. Dallas Mfg. Co.*, 2006 U.S. Dist. LEXIS 19528, *39-40 (D. Mass. 2006) ("Without a case or controversy, a district court has no jurisdiction to make a declaratory judgment on the validity of claims."; court had no jurisdiction to decide validity of claims not alleged to be infringed). The '719 Patent is cited by Fairchild in the Delaware action as one of its prior art references. However, the primary prior art assertion actually involves not the '719 Patent, but rather its "parent" patent. But that does not confer jurisdiction to decide the validity of the '719 Patent where it is not alleged to be infringed.

For these reasons, there is absolutely no potential for inconsistent rulings between the cases. Simply put, the two cases involve distinct patents, which will require independent claim constructions and determinations of infringement, validity and enforceability. *See e.g. Datamize, Inc. v. Fid. Brokerage Servs., LLC*, 2004 U.S. Dist. LEXIS 29100, *17-18 (E.D. Tex. 2004) (fact that patent asserted in second action might be relevant to claim construction of patent asserted in first action did *not* support transfer because patent in first action not asserted in second action).⁶ Therefore, as discussed in detail below, *PI*'s motion to transfer to Delaware must be denied.

2. The "First-To-File" Rule Does Not Support Transfer To Delaware

It is "well-established" that a plaintiff's choice of forum is "highly esteemed" and should be given deference. *Datamize, Inc.*, 2004 U.S. Dist. LEXIS 29100 at *23-24. The plaintiff's choice of a forum is "a paramount consideration in any determination of transfer request, and that choice should not be lightly disturbed." *Young v. Armstrong World Indus.*, 601 F. Supp. 399,

⁶ Also, the fact that a claim in a second filed action could be asserted as a defensive theory in the first filed action does not support transfer of the second filed action to the venue in which the first action was filed. *See Rooster Prods. Int'l, Inc. v. Custom Leathercraft Mfg. Co.*, 2005 U.S. Dist. LEXIS 1643, 5-7 (W.D. Tex. 2005) (whether a claim could be brought as a permissive counterclaim is not the test to determine whether transfer is appropriate).

401 (N.D. Tex. 1984).⁷ The plaintiff's choice of forum is particularly important where, as is the case here, plaintiffs allege that defendant has engaged in infringing activity within that forum. *See Datamize, Inc.*, 2004 U.S. Dist. LEXIS 29100 at *23-25. Intersil's and Fairchild's decision to bring this action in the Eastern District of Texas should be respected.

An exception to this general principle is the "first-to-file rule," by which a later-filed action may be transferred to a court in which a first-filed action is pending. However, such transfer is only appropriate when the actions are so duplicative or involve such substantially similar issues that one court should decide both actions. *See Rooster Prods. Int'l, Inc. v. Custom Leathercraft Mfg. Co.*, 2005 U.S. Dist. LEXIS 1643, *5-7 (W.D. Tex. 2005). Here, because (a) the instant matter is the "first filed" action and (b) there is not substantial overlap of issues between the two actions, the first-to-file rule supports proceeding in Texas instead of Delaware. PI's motion to transfer based on the first-to-file rule is disingenuous and must be denied.

To begin with, this action is the first and only action in which the '719 Patent is asserted to be infringed by anyone. Therefore, contrary to PI's assertions, this case is the "first-filed" action. The case *Cummins-Allison Corp. v. Glory Ltd.*, 2004 U.S. Dist. LEXIS 13839 (E.D. Tex. 2004) is instructive. There, certain patents were asserted in an earlier-filed Illinois case and entirely different, but "related," patents were asserted in a later-filed Texas case involving the same parties. The Texas court found that under these circumstances, the Texas case was "first-filed" with respect to the patents asserted in Texas and denied transfer on that basis:

The Court finds that this case is the first-filed case and should proceed in this Court. Although the patents are related and might involve the interpretation of identical claim terms, the patents are different patents than those in suit in the initial Illinois case.

Id. Likewise, because the '719 Patent is not asserted in Delaware, the instant case is the "first

⁷ Further, it has been observed that: "the judicial system inherently provides a plaintiff with his choice of forum: The existence of [forum choices] not only permits but indeed invites counsel in an adversary system, seeking to serve in his client's interests, to select the forum that he considers most receptive to his cause. The motive of the suitor in making this choice is ordinarily of no moment: a court may be selected because its docket moves rapidly, its discovery procedures are liberal, its jurors are generous, the rules of law applied are more favorable, or the judge who presides in that forum is thought more likely to rule in the litigant's favor." *McCuin v. Texas Power & Light Co.*, 714 F.2d 1255, 1261-62 (5th Cir. 1983).

filed” action regarding that patent. Indeed, here the patents are not even “related,” thus the rule applies even more forcefully. Therefore, the action should proceed in this court.

Second, the issues in the Delaware action and the instant action are so divergent that the “first-to-file” rule does not support transfer. To determine whether there is substantial overlap of issues for purposes of the first to file rule, it is necessary to engage in a “comparison of the pleadings” to assess whether there is overlap in the “claims.” *Rooster Prods. Int’l, Inc.*, 2005 U.S. Dist. LEXIS 1643 at *6. A comparison of the Delaware complaint and the complaint in the instant action reveals that the four patents-in-suit in Delaware are not asserted in this case, nor is the sole patent at issue here asserted in Delaware. [Ramsey Decl., Exs. 6, 7] On that basis alone, it is evident there is no substantial overlap of issues.⁸ Therefore, the first-to-file rule does not apply and PI’s motion to transfer should be denied. *See id.* (denying motion to transfer where non-Texas action and Texas action involved different claims); *Datamize, Inc.*, 2004 U.S. Dist. LEXIS 29100 at *3, 7, 34 (denying transfer where non-Texas action involved the “parent” patent which was different, but related to the “child” patent asserted in Texas action).

As discussed above, the resolution of infringement, validity and enforceability of the four patents in suit in the Delaware action will in no way determine or resolve issues of infringement, validity and enforceability of the ‘719 Patent at issue in the instant action. [See *supra* Section B.1.] The fact that the content of each suit will require independent development weighs against transfer. *See id.* at *10 (fact that “overall content of each suit” is “very capable of independent development” weighed against transfer). Because there are different defendants, different accused products and different patent claims, requiring independent construction, there is no substantial overlap of issue and transfer is inappropriate. *See id.* at *11 (where “case involves different defendants, different patent claims, different claim scopes” and “different accused products,” no substantial overlap of issues). PI’s motion to transfer should be denied.

⁸ For this reason, the case *Mann Mfg., Inc. v. Hortex, Inc.*, 439 F.2d 403 (5th Cir. 1971), relied upon by PI at pages 10-11 of its brief, is inapposite. In the *Mann* case the same patent was the subject of a declaratory action of non-infringement in New York and an affirmative infringement action in Texas. By contrast, here there is no overlap of asserted patents whatsoever.

3. **It Would Be Unjust And Inefficient To Transfer This Case To Delaware**

A case should not be transferred where doing so would be contrary to “the convenience of parties and witnesses” or contrary to the “interest of justice.” 28 U.S.C. §1404(a). Similarly, even where the first-to-file rule might otherwise be applicable, transfer is inappropriate where it would be “unjust or inefficient.” *Genentech v. Eli Lilly & Co.*, 998 F.2d 931, 938 (Fed. Cir. 1993). As PI correctly observes, courts consider “all relevant factors” to determine the propriety of transfer. [PI Brief, at 13] The party moving for transfer—in this case PI—bears the burden of proving that relevant factors support transfer. *Network-1 Sec. Solutions, Inc. v. D-Link Corp.*, 2006 U.S. Dist. LEXIS 16545 (E.D. Tex. 2006) (“The movant bears the burden of proof in demonstrating that transfer is warranted.”). If the moving party fails to carry that burden, the motion to transfer must be denied. In the instant case, it would be highly inefficient and contrary to the convenience of the parties and witnesses, the interest of justice and public policy to transfer the action to Delaware. PI has failed to carry its burden of proving otherwise. For all of these reasons, PI’s motion to transfer must be denied.

a. **Transfer Is Inappropriate Because It Would Be Inconvenient For The Parties And Witnesses**

Courts consider the convenience and availability of parties and witnesses in determining whether transfer is appropriate. *See e.g. Genentech*, 998 F.2d at 938. In this case, it would be inconvenient for parties and witnesses to proceed in Delaware. Two of the four parties—plaintiff Intersil and defendant PI—are located in California. [Ramsey Decl., Ex. 6 at ¶¶3-4] As PI points out, the inventor of the ‘719 Patent resides in Florida.⁹ Further, third-party Harris Corporation (from which Intersil acquired the asserted patent) is headquartered in Melbourne Florida. [*Id.*, Ex. 9] Similarly, the prosecuting attorney Charles E. Wands is located in Orlando Florida. [*Id.*, Ex. 10] Obviously these parties and witnesses are much closer to Texas than

⁹ The fact that plaintiff Fairchild has a principal place of business in Maine, closer to Delaware does not weigh in favor of transfer, given that Fairchild itself has chosen Texas as a forum. *See Datamize, Inc., LLC*, 2004 U.S. Dist. LEXIS 29100 at *26 (Where a plaintiff has chosen the forum, there is no inconvenience to plaintiff’s own witnesses and transfer is inappropriate.)

Delaware, increasing the convenience and reducing the cost of obtaining attendance at trial.¹⁰ At the very least, there is no more connection to Delaware than to Texas. Accordingly, PI has not carried its burden on this factor and the plaintiff's choice of forum should control. *See Datamize, Inc.*, 2004 U.S. Dist. LEXIS 29100 at *27-28 (proximity of majority of parties to chosen forum weighed against transfer).

PI does not provide any evidence to the contrary, but merely professes not to be aware of any fact witnesses in Texas. This is a complete failure by PI to carry its burden on this factor and weighs against transfer. *See Datamize, Inc.*, 2004 U.S. Dist. LEXIS 29100 at *26-27 (rejecting argument that Defendant was "not aware of any" witnesses in Texas; "Because Defendants are unaware of any Datamize or defense witnesses located in Texas does not mean none exist. A generalized argument such as this does not overcome Defendants' burden."). For all of these reasons, this factor supports denial of PI's motion.

b. Transfer Is Inappropriate In Light Of The Accessibility And Location Of Sources Of Proof

The accessibility and location of proof is also a relevant factor to consider. *Network-1 Sec. Solutions, Inc.*, 2006 U.S. Dist. LEXIS 16545 at *6. The documentary evidence of two of the three parties, Intersil and PI are likely to be located in California. Similarly, the documentary evidence in the possession of the inventor and prosecution counsel is likely to be located in Florida. These sources of proof are closer to Texas than Delaware, weighing against transfer.

c. Transfer Is Inappropriate Because There Is No Possibility Of Consolidation With The Delaware Action And Transfer Would Only Result In Delay And Prejudice

Courts also consider the possibility of consolidation, in determining whether transfer is appropriate. *See e.g. Genentech*, 998 F.2d at 938. There is no possibility of consolidation in Delaware of the action pending there and the instant action. The Delaware action involves four patents not asserted in the instant case and the patent asserted here is not asserted in Delaware.

¹⁰ The cost of obtaining attendance of witnesses at trial was not even addressed by PI in its motion. Therefore PI has not met its burden on this factor. *See Datamize, Inc.*, 2004 U.S. Dist. LEXIS 29100 at *28 (finding same)

Staggering inefficiencies would result from any attempt to consolidate the cases. The Delaware action has progressed very nearly to trial. Substantial discovery has been conducted regarding infringement, validity and enforceability of the four patents at issue in that case. Summary judgment motions have been heard and ruled upon. Pre-trial materials have been exchanged. This activity has been with respect to four patents that are not involved in the instant dispute.

To inject into the Delaware case an entirely new cause of action for infringement of the '719 Patent would require litigation of infringement, invalidity and enforceability of the '719 Patent, which will not otherwise be addressed. To do so would require a continuance of the scheduled trial until the parties were able to litigate all of the issues in the case. Given how close the Delaware action is to trial, the parties would only be prejudiced by delay and burdened by significant inefficiencies. *See Datamize, Inc.*, 2004 U.S. Dist. LEXIS 29100 at *28-29 (where issues of delay did not weigh clearly in favor of defendant, defendant failed to carry burden and transfer inappropriate). Accordingly, PI has not carried its burden on this factor.

d. Transfer Is Inappropriate Because The Actions Involve Different Parties

Courts consider whether the real parties in interest are the same in two actions, in determining whether transfer is appropriate. *See e.g. Genentech*, 998 F.2d at 938. The Delaware action does not involve the real parties in interest in this case. In particular, as PI concedes in its brief, plaintiff Intersil in this action is not a party to the Delaware action. The fact that Intersil has communicated with Fairchild about the Delaware case and responded to a third-party discovery subpoena, does *not* make it party to the Delaware action. Intersil is nothing but a bystander in the distinct, unrelated dispute in Delaware. In fact, the only appearance Intersil made in Delaware was to file a motion to quash on the basis that discovery related to the instant action should be left to and decided by this Court. [Ramsey Decl., ¶15] This is simply not a basis to argue that Intersil has somehow acquiesced to the primacy of the Delaware court; indeed, it suggests the opposite. Transfer to Delaware would be unjust and inefficient to Intersil, which has chosen the Eastern District of Texas as its desired forum. Therefore, PI has failed to

carry its burden and this factor weighs against transfer.

e. Matters Of Public Interest Weigh Against Transfer

Several public interest factors are considered in determining the propriety of transfer, including: “(1) the relative backlog and other administrative difficulties in the two jurisdictions; (2) the fairness of placing the burdens of jury duty on the citizens of the state with the greater interest in the dispute; (3) the local interest in adjudicating local disputes; and, (4) the appropriateness of having the case in a jurisdiction whose law will govern the dispute in order to avoid difficult problems in conflicts of laws.” *In re Triton Secs. Litig.*, 70 F. Supp. 2d 678, 688 (E.D. Tex. 1999).

Proceeding in Texas would pose no administrative difficulties. The substantial experience of this Court with patent cases and the particularized rules of procedure adopted in this venue for patent cases will lead to great efficiencies. Further, as discussed, because the cases involve different parties, different patents and different accused products there is not substantial overlap of issues between the two cases. Accordingly, there will be no inefficiencies related to inconsistent rulings or duplicative efforts if transfer is denied. *Datamize, Inc.*, 2004 U.S. Dist. LEXIS 29100 at *30-31. Given the differences between the cases, PI’s assertion that pre-trial preparations in this action would be “wasted” pending the final outcome of the Delaware action is incorrect. [PI Brief, at 14]¹¹

Further, the public interest factors of jury duty burden and local interest in adjudicating local disputes weigh in favor of proceeding with the case in Texas. *Id.* at *32. The infringement of the ‘719 Patent has occurred in Texas, therefore citizens in the District have an interest in

¹¹ Even if particular findings in the Delaware case were assumed to be relevant to issues in this case, that fact is still not a basis for transferring this action to Delaware, as no inefficiency would result from proceeding in Texas. The bifurcated Delaware trial will occur in October and December of this year. Findings from that trial will be available for consideration by the Court or jury in this action well before any dispositive motions are heard or trial proceeds in this case. If this action, which is only beginning, were transferred to Delaware, the situation would be precisely the same. The findings from the imminent Delaware trial would be available to a Delaware court or jury at the same time they would be available if this case proceeds in Texas. Thus, contrary to PI’s assertions, no administrative efficiencies would result from transfer, nor are there any inefficiencies imposed by proceeding in Texas.

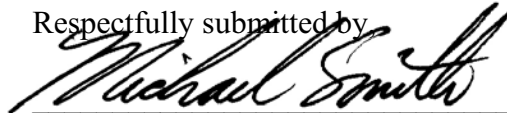
resolving the dispute. PI has failed to show that there is any greater connection with Delaware. PI has produced no evidence of any greater burden on a potential jury in the Eastern District of Texas, a lesser burden on any jury in Delaware, or a greater interest among the citizens of Delaware to try this case. Finally, PI does not contend that any choice of law conflicts that would arise if this case is not transferred. These factors supports denial of PI's motion as well.

III. CONCLUSION

For the foregoing reasons, this Court should deny PI's motion to dismiss for lack of standing and should deny PI's motion to transfer this case to Delaware.

OF COUNSEL:
G. Hopkins Guy, III (SBN 124811)
Bas de Blank (SBN 191487)
Orrick, Herrington & Sutcliffe LLP
1000 Marsh Road
Menlo Park, CA 94025
(650) 614-7400

Respectfully submitted by



Carl R. Roth, Texas Bar No. 901984225
cr@rothfirm.com
Michael C. Smith, Texas Bar No. 900641877
ms@rothfirm.com
THE ROTH LAW FIRM, P.C.
115 North Wellington, Suite 200
P.O. Box 876
Marshall, Texas 75671
Tel: (903) 935-1665
Fax: (903) 935-1797

Attorneys for Plaintiffs,
FAIRCHILD SEMICONDUCTOR
CORPORATION, INTERSIL CORPORATION,
INTERASIL AMERICAS, INC.

SHORE CHAN BRAGALONE, L.L.P.
Michael Shore, Texas Bar No. 18294915
shore@shorechan.com
Jeffrey R. Bragalone, Texas Bar No. 02855775
jbragalone@shorechan.com
325 North St. Paul, Suite 4450
Dallas, Texas 75201
Tel: (214) 593-9110
Fax: (214) 593-9111

Attorneys for Plaintiffs,
INTERASIL CORPORATION, INTERSIL
AMERICAS, INC.

CERTIFICATE OF SERVICE

The undersigned hereby certifies that all counsel of record who are deemed to have consented to electronic service are being served with a copy of this document via the Court's CM/ECF system per Local Rule CV-5(a)(3) this 26th day of July, 2006. Any other counsel of record will be served by facsimile transmission and/or first class mail.

A handwritten signature in black ink, reading "Michael Smith", written over a horizontal line.

Michael C. Smith

Substitute Form PTO-1595

9-77-96

**RECORDATION FORM COVER SHEET
PATENTS ONLY**

09-30-1999

Assistant Commissioner for Patents: Please record the attached original document



101158628

1. Name of conveying party(ies):
Harris Corporation

2. Name and address of receiving party(ies):
Intersil Corporation
2401 Palm Bay Road, N.E.
Palm Bay, FL 32905

Additional name(s) attached? ☐ Yes ☒ NoAdditional names/addresses attached? ☐ Yes ☒ No

3. Nature of conveyance:
- ☒ Assignment
 - ☐ Merger
 - ☐ Security Agreement
 - ☐ Change of Name
 - ☐ Other:

CEIVE

EP 27 1999

Execution Date: **August 13, 1999**

4. Application number(s) or patent number(s):

If this document is being filed with a new application, the execution date of the application is:

A. Patent Application No.(s):

B. Patent No.(s):

Additional numbers attached? ☒ Yes ☐ No

4236231

5. Name/address of party to whom correspondence concerning document should be mailed:

Timothy A. French
Fish & Richardson P.C.
225 Franklin Street
Boston, MA 02110-2804

6. Total number of applications/patents involved: **806**7. Total fee (37 CFR 3.41): **\$32,240.00**☒ Enclosed☐ Authorized to charge deposit account8. Deposit account number: **06-1050**

If the fee above is being charged to deposit account, a duplicate copy of this cover sheet is attached. Please apply any additional charges, or any credits, to our Deposit Account No. 06-1050.

09/29/1999 JSWDAZZ 00000025 4236231

DO NOT USE THIS SPACE

01 FC:581

32240.00 00

9. Statement and signature: *To the best of my knowledge and belief, the foregoing information is true and correct and the attached is the original document.*

Timothy A. French

Name of Person Signing

Signature

09/21/99

Date

Total number of pages including cover sheet, attachments, and document: **1**Date of Deposit Sept 21 1999

I hereby certify under 37 CFR 1.8(a) that this correspondence is being deposited with the United States Postal Service as **first class mail** with sufficient postage on the date indicated above and is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

Augustine McNeil

PATENT**REEL: 010247 FRAME: 0043**

HARRIS PATENT ASSIGNMENT

FOR VALUE RECEIVED, the receipt and sufficiency of which is hereby acknowledged, the undersigned Harris Corporation, a corporation of Delaware having a place of business at 1025 West NASA Blvd., Melbourne, Florida 32919 ("Harris"), does hereby assign, transfer and set over to Intersil Corporation, a corporation of Delaware having a place of business at 2401 Palm Bay Road, N.E., Melbourne, Florida 32905, its successors, legal representatives and assigns (hereinafter "Assignee") the entire right, title and interest in and to each of the United States patents and patent applications listed in the attached Appendix A, together with the inventions disclosed and/or claimed therein, as well as all applications for patent and any Letters Patent which may be granted therefor, in the United States of America and in all foreign countries, and in and to any and all divisions, continuations, continuations-in-part of said applications, or re-issues or extensions of said patents or Letters Patent, and all rights under the International Convention for the Protection of Industrial Property and similar agreements (hereinafter individually and collectively "Patents").

Harris hereby appoints Assignee as its agent and attorney-in-fact to conduct all business before the United States Patent & Trademark Office and the patent offices in all foreign countries in the name of Harris in connection with said Patents.

Harris hereby authorizes and requests that the United States Patent & Trademark Office, and the patent offices of all foreign countries, to issue any and all Letters Patent of the United States and patents in all foreign countries resulting from said application or any division or divisions or continuing applications thereof in the United States and all foreign countries to Assignee, as assignee of the entire interest, and Harris hereby covenants that it has full right to convey the entire interest herein assigned, and that it has not executed and will not execute, any agreement in conflict herewith.

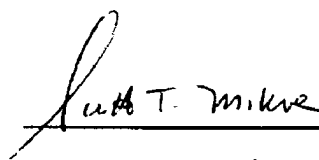
Harris further agrees to cooperate with the Assignee in every way possible and to do all affirmative acts, and to execute all papers which counsel for Assignee shall advise are necessary and/or desirable without charge to Assignee in connection with said Patents including, without limitation, the execution of separate assignments for filing in the United States Patent & Trademark Office and the patent offices of all foreign countries in connection with said Patents.

The undersigned Harris hereby grants to Howard Rothman; John DeAngelis, Reg. No. 30,622; Ferdinand M. Romano, Reg. No. 32,752; and L. Lawton Rogers, III, Reg. No. 24,302 the power to insert on this assignment any further identification which may be necessary or desirable in order to comply with the rules of the United States Patent Office for recordation of this document.

IN WITNESS WHEREOF,

Date August 13, 1999

HARRIS CORPORATION

By:  (Signature)
Scott T. Mikuen (Printed Name)
Assistant Secretary (Title)

ATTEST:

[SEAL]


Secretary

Date August 13, 1999

APPENDIX A

HARRIS CORPORATION

ISSUED PATENTS

Patent Number	Issue Date
4236231	25-Nov-1980
4260431	07-Apr-1981
4272833	09-Jun-1981
4281449	04-Aug-1981
4283236	11-Aug-1981
4288911	15-Sep-1981
4290831	22-Sep-1981
4292730	06-Oct-1981
4299024	10-Nov-1981
4301383	17-Nov-1981
4305106	08-Dec-1981
4309813	12-Jan-1982
4312046	19-Jan-1982
4319257	09-Mar-1982
4334646	15-Jun-1982
4368395	11-Jan-1983
4380710	19-Apr-1983
4389721	21-Jun-1983
4398142	09-Aug-1983
4401940	30-Aug-1983
4402002	30-Aug-1983
4402065	30-Aug-1983
4403399	13-Sep-1983
4409686	11-Oct-1983
4420766	13-Dec-1983
4446444	01-May-1984
4450414	22-May-1984
4454432	12-Jun-1984
4456918	26-Jun-1984
4461000	17-Jul-1984
4462020	24-Jul-1984
4464631	07-Aug-1984
4464825	14-Aug-1984
4466179	21-Aug-1984
4468414	28-Aug-1984
4471236	11-Sep-1984
4471376	11-Sep-1984
4472648	18-Sep-1984
4480219	30-Oct-1984
4495537	22-Jan-1985
4495694	29-Jan-1985
4503387	05-Mar-1985
4514802	30-Apr-1985
4524246	18-Jun-1985
4528461	09-Jul-1985
4528462	09-Jul-1985
4528504	09-Jul-1985
4532003	30-Jul-1985
4532481	30-Jul-1985
4536231	20-Aug-1985
4546539	15-Oct-1985
4554059	19-Nov-1985
4559608	17-Dec-1985

Patent Number	Issue Date
4560948	24-Dec-1985
4566796	28-Jan-1986
4567385	28-Jan-1986
4567578	28-Jan-1986
4578859	01-Apr-1986
4580131	01-Apr-1986
4581548	08-Apr-1986
4584660	22-Apr-1986
4586193	29-Apr-1986
4590664	27-May-1986
4591826	27-May-1986
4594265	10-Jun-1986
4595608	17-Jun-1986
4596068	24-Jun-1986
4599789	15-Jul-1986
4606936	19-Aug-1986
4608530	26-Aug-1986
4613772	23-Sep-1986
4616178	07-Oct-1986
4618743	21-Oct-1986
4620179	28-Oct-1986
4624749	25-Nov-1986
4631636	23-Dec-1986
4632557	30-Dec-1986
4633107	30-Dec-1986
4636743	13-Jan-1987
4636744	13-Jan-1987
4639684	27-Jan-1987
4639896	27-Jan-1987
4644191	17-Feb-1987
4644192	17-Feb-1987
4644383	17-Feb-1987
4650696	17-Mar-1987
4652895	24-Mar-1987
4658253	14-Apr-1987
4665327	12-May-1987
4665425	12-May-1987
4666737	19-May-1987
4669884	02-Jun-1987
4670769	02-Jun-1987
4675798	23-Jun-1987
4677321	30-Jun-1987
4682057	21-Jul-1987
4682059	21-Jul-1987
4683485	28-Jul-1987
4684055	04-Aug-1987
4686384	11-Aug-1987
4694313	15-Sep-1987
4698589	06-Oct-1987
4701644	20-Oct-1987
4702000	27-Oct-1987
4702967	27-Oct-1987
4703505	27-Oct-1987
4703566	03-Nov-1987
4705596	10-Nov-1987
4705597	10-Nov-1987
4708747	24-Nov-1987
4713260	15-Dec-1987

58

Patent Number	Issue Date
4713681	15-Dec-1987
4716071	29-Dec-1987
4717680	05-Jan-1988
4717847	05-Jan-1988
4719598	12-Jan-1988
4720739	19-Jan-1988
4728820	01-Mar-1988
4729008	01-Mar-1988
4733168	22-Mar-1988
4734885	29-Mar-1988
4734886	29-Mar-1988
4752591	21-Jun-1988
4753851	28-Jun-1988
4754388	28-Jun-1988
4755770	05-Jul-1988
4757363	12-Jul-1988
4757528	12-Jul-1988
4760433	26-Jul-1988
4761570	02-Aug-1988
4771016	13-Sep-1988
4780688	25-Oct-1988
4781853	01-Nov-1988
4783637	08-Nov-1988
4786608	22-Nov-1988
4789426	06-Dec-1988
4795718	03-Jan-1989
4801065	31-Jan-1989
4804865	14-Feb-1989
4807012	21-Feb-1989
4808547	28-Feb-1989
4812962	14-Mar-1989
4814285	21-Mar-1989
4818725	04-Apr-1989
4818901	04-Apr-1989
4820968	11-Apr-1989
4823173	18-Apr-1989
4823300	18-Apr-1989
4839711	13-Jun-1989
4845052	04-Jul-1989
4851078	25-Jul-1989
4851257	25-Jul-1989
4854986	08-Aug-1989
4855625	08-Aug-1989
4857764	15-Aug-1989
4859280	22-Aug-1989
4862231	29-Aug-1989
4868778	19-Sep-1989
4873564	10-Oct-1989
4876579	24-Oct-1989
4879520	07-Nov-1989
4879523	07-Nov-1989
4881111	14-Nov-1989
4882698	21-Nov-1989
4888741	19-Dec-1989
4891604	02-Jan-1990
4891606	02-Jan-1990
4893088	09-Jan-1990
4897362	30-Jan-1990

Patent Number	Issue Date
4897366	30-Jan-1990
4897567	30-Jan-1990
4900689	13-Feb-1990
4908566	13-Mar-1990
4908683	13-Mar-1990
4912053	27-Mar-1990
4914501	03-Apr-1990
4916497	10-Apr-1990
4923820	08-May-1990
4923826	08-May-1990
4927777	22-May-1990
4929566	29-May-1990
4929568	29-May-1990
4929923	29-May-1990
4937774	26-Jun-1990
4941027	10-Jul-1990
4945070	31-Jul-1990
4945262	31-Jul-1990
4948746	14-Aug-1990
4949296	14-Aug-1990
4951102	21-Aug-1990
4956306	11-Sep-1990
4968628	06-Nov-1990
4968900	06-Nov-1990
4970573	13-Nov-1990
4970677	13-Nov-1990
4975751	04-Dec-1990
4978868	18-Dec-1990
4978925	18-Dec-1990
4979011	18-Dec-1990
4980651	25-Dec-1990
4982194	01-Jan-1991
4988902	29-Jan-1991
5008719	16-Apr-1991
5010377	23-Apr-1991
5014055	07-May-1991
5014108	07-May-1991
5015877	14-May-1991
5015887	14-May-1991
5021359	04-Jun-1991
5028824	02-Jul-1991
5028973	02-Jul-1991
5030862	09-Jul-1991
5032529	16-Jul-1991
5034343	23-Jul-1991
5034789	23-Jul-1991
5036219	30-Jul-1991
5037765	06-Aug-1991
5038248	06-Aug-1991
5039888	13-Aug-1991
5047974	10-Sep-1991
5051619	24-Sep-1991
5051949	24-Sep-1991
5053345	01-Oct-1991
5053353	01-Oct-1991
5057895	15-Oct-1991
5059982	22-Oct-1991
5060192	22-Oct-1991

58

Patent Number	Issue Date
5066995	19-Nov-1991
5070388	03-Dec-1991
5070451	03-Dec-1991
5070596	10-Dec-1991
5079176	07-Jan-1992
5079608	07-Jan-1992
5079734	07-Jan-1992
5081061	14-Jan-1992
5081063	14-Jan-1992
5081410	14-Jan-1992
5084839	28-Jan-1992
5085084	04-Feb-1992
5086242	04-Feb-1992
5091331	25-Feb-1992
5091336	25-Feb-1992
5095343	10-Mar-1992
5096850	17-Mar-1992
5097319	17-Mar-1992
5105099	14-Apr-1992
5107312	21-Apr-1992
5111268	05-May-1992
5113361	12-May-1992
5117282	26-May-1992
5118632	02-Jun-1992
5119321	02-Jun-1992
5120669	09-Jun-1992
5130569	14-Jul-1992
5134321	28-Jul-1992
5138319	11-Aug-1992
5138413	11-Aug-1992
5140326	18-Aug-1992
5142244	25-Aug-1992
5148475	15-Sep-1992
5150120	22-Sep-1992
5151953	29-Sep-1992
5164802	17-Nov-1992
5184128	02-Feb-1993
5185292	09-Feb-1993
5194867	16-Mar-1993
5196373	23-Mar-1993
5196737	23-Mar-1993
5198385	30-Mar-1993
5200733	06-Apr-1993
5206821	27-Apr-1993
5214329	25-May-1993
5217919	08-Jun-1993
5218213	08-Jun-1993
5218220	08-Jun-1993
5218321	08-Jun-1993
5220868	22-Jun-1993
5228192	20-Jul-1993
5228330	20-Jul-1993
5229661	20-Jul-1993
5233289	03-Aug-1993
5235205	10-Aug-1993
5240876	31-Aug-1993
5241213	31-Aug-1993
5243211	07-Sep-1993

58

Patent Number	Issue Date
5247199	21-Sep-1993
5248894	28-Sep-1993
5248901	28-Sep-1993
5248932	28-Sep-1993
5258939	02-Nov-1993
5260590	09-Nov-1993
5262689	16-Nov-1993
5262976	16-Nov-1993
5264719	23-Nov-1993
5265225	23-Nov-1993
5266135	30-Nov-1993
5270265	14-Dec-1993
5270569	14-Dec-1993
5272104	21-Dec-1993
5276633	04-Jan-1994
5279850	18-Jan-1994
5283461	01-Feb-1994
5287068	15-Feb-1994
5287071	15-Feb-1994
5289336	22-Feb-1994
5293052	08-Mar-1994
5298434	29-Mar-1994
5300877	05-Apr-1994
5302859	12-Apr-1994
5306650	26-Apr-1994
5306944	26-Apr-1994
5307023	26-Apr-1994
5311054	10-May-1994
5311070	10-May-1994
5312262	17-May-1994
5315144	24-May-1994
5317184	31-May-1994
5319757	07-Jun-1994
5322804	21-Jun-1994
5323036	21-Jun-1994
5327006	05-Jul-1994
5329187	12-Jul-1994
5332931	26-Jul-1994
5334273	02-Aug-1994
5334929	02-Aug-1994
5335132	02-Aug-1994
5338960	16-Aug-1994
5341009	23-Aug-1994
5341335	23-Aug-1994
5345236	06-Sep-1994
5347169	13-Sep-1994
5350935	27-Sep-1994
5352327	04-Oct-1994
5357089	18-Oct-1994
5359211	25-Oct-1994
5359236	25-Oct-1994
5362667	08-Nov-1994
5366932	22-Nov-1994
5367211	22-Nov-1994
5369309	29-Nov-1994
5370568	06-Dec-1994
5373183	13-Dec-1994
5382541	17-Jan-1995

58

Patent Number	Issue Date
5382825	17-Jan-1995
5382916	17-Jan-1995
5387555	07-Feb-1995
5391903	21-Feb-1995
5395774	07-Mar-1995
5397714	14-Mar-1995
5399892	21-Mar-1995
5406223	11-Apr-1995
5416351	16-May-1995
5418002	23-May-1995
5420499	30-May-1995
5422288	06-Jun-1995
5423889	13-Jun-1995
5424563	13-Jun-1995
5428492	27-Jun-1995
5429958	04-Jul-1995
5429993	04-Jul-1995
5434357	18-Jul-1995
5436189	25-Jul-1995
5438221	01-Aug-1995
5440506	08-Aug-1995
5446316	29-Aug-1995
5446368	29-Aug-1995
5448100	05-Sep-1995
5448102	05-Sep-1995
5450326	12-Sep-1995
5450339	12-Sep-1995
5451263	19-Sep-1995
5455442	03-Oct-1995
5455782	03-Oct-1995
5463344	31-Oct-1995
5466963	14-Nov-1995
5468668	21-Nov-1995
5469556	21-Nov-1995
5471131	28-Nov-1995
5473193	05-Dec-1995
5481129	02-Jan-1996
5493207	20-Feb-1996
5493581	20-Feb-1996
5497013	05-Mar-1996
5504033	02-Apr-1996
5504449	02-Apr-1996
5508551	16-Apr-1996
5515402	07-May-1996
5515417	07-May-1996
5515434	07-May-1996
5516625	14-May-1996
5517047	14-May-1996
5517058	14-May-1996
5517565	14-May-1996
5519732	21-May-1996
5521436	28-May-1996
5525869	11-Jun-1996
5526392	11-Jun-1996
5526768	18-Jun-1996
5528682	18-Jun-1996
5532635	02-Jul-1996
5539707	23-Jul-1996

56

Patent Number	Issue Date
5541435	30-Jul-1996
5541538	30-Jul-1996
5544095	06-Aug-1996
5546038	13-Aug-1996
5547896	20-Aug-1996
5548542	20-Aug-1996
5552345	03-Sep-1996
5557175	17-Sep-1996
5561303	01-Oct-1996
5561607	01-Oct-1996
5563834	08-Oct-1996
5567978	22-Oct-1996
5569620	29-Oct-1996
5569957	29-Oct-1996
5570392	29-Oct-1996
5570407	29-Oct-1996
5572161	05-Nov-1996
5572162	05-Nov-1996
5574572	12-Nov-1996
5574609	12-Nov-1996
5574618	12-Nov-1996
5574671	12-Nov-1996
5576654	19-Nov-1996
5576695	19-Nov-1996
5577656	26-Nov-1996
5580816	03-Dec-1996
5581444	03-Dec-1996
5581475	03-Dec-1996
5583442	10-Dec-1996
5585310	17-Dec-1996
5585661	17-Dec-1996
5586072	17-Dec-1996
5587103	24-Dec-1996
5594261	14-Jan-1997
5598157	28-Jan-1997
5602052	11-Feb-1997
5602054	11-Feb-1997
5603779	18-Feb-1997
5606288	25-Feb-1997
5608259	04-Mar-1997
5608264	04-Mar-1997
5610093	11-Mar-1997
5610792	11-Mar-1997
5614422	25-Mar-1997
5614852	25-Mar-1997
5614867	25-Mar-1997
5617090	01-Apr-1997
5617344	01-Apr-1997
5617473	01-Apr-1997
5618752	08-Apr-1997
5619270	08-Apr-1997
5621307	15-Apr-1997
5621355	15-Apr-1997
5621477	15-Apr-1997
5621478	15-Apr-1997
5622878	22-Apr-1997
5622890	22-Apr-1997
5625566	29-Apr-1997

Patent Number	Issue Date
5627489	06-May-1997
5631599	20-May-1997
5633180	27-May-1997
5633815	27-May-1997
5636274	03-Jun-1997
5637908	10-Jun-1997
5639688	17-Jun-1997
5640300	17-Jun-1997
5640346	17-Jun-1997
5642247	24-Jun-1997
5643821	01-Jul-1997
5644309	01-Jul-1997
5646067	08-Jul-1997
5648678	15-Jul-1997
5649009	15-Jul-1997
5650344	22-Jul-1997
5650639	22-Jul-1997
5650658	22-Jul-1997
5650971	22-Jul-1997
5652153	29-Jul-1997
5654226	05-Aug-1997
5654662	05-Aug-1997
5654991	05-Aug-1997
5656512	12-Aug-1997
5659261	19-Aug-1997
5659269	19-Aug-1997
5659570	19-Aug-1997
5661736	26-Aug-1997
5663860	02-Sep-1997
5665634	09-Sep-1997
5666083	09-Sep-1997
5668397	16-Sep-1997
5668409	16-Sep-1997
5668468	16-Sep-1997
5669599	23-Sep-1997
5670413	23-Sep-1997
5670799	23-Sep-1997
5671272	23-Sep-1997
5672998	30-Sep-1997
5675281	07-Oct-1997
5675339	07-Oct-1997
5677599	14-Oct-1997
5678030	14-Oct-1997
5680072	21-Oct-1997
5682062	28-Oct-1997
5682111	28-Oct-1997
5682336	28-Oct-1997
5683075	04-Nov-1997
5683939	04-Nov-1997
5684305	04-Nov-1997
5686322	11-Nov-1997
5686822	11-Nov-1997
5689129	18-Nov-1997
5694417	02-Dec-1997
5696452	09-Dec-1997
5701097	23-Dec-1997
5708549	13-Jan-1998
5712870	27-Jan-1998

Patent Number	Issue Date
5717243	10-Feb-1998
5717322	10-Feb-1998
5717617	10-Feb-1998
5717736	10-Feb-1998
5719326	17-Feb-1998
5724370	03-Mar-1998
5728624	17-Mar-1998
5729038	17-Mar-1998
5732105	24-Mar-1998
5736885	07-Apr-1998
5736903	07-Apr-1998
5742204	21-Apr-1998
5744851	28-Apr-1998
5744852	28-Apr-1998
5745563	28-Apr-1998
5750432	12-May-1998
5757036	26-May-1998
5757794	26-May-1998
5764113	09-Jun-1998
5767740	16-Jun-1998
5767757	16-Jun-1998
5770878	23-Jun-1998
5770880	23-Jun-1998
5771012	23-Jun-1998
5773151	30-Jun-1998
5773891	30-Jun-1998
5776814	07-Jul-1998
5777346	07-Jul-1998
5777362	07-Jul-1998
5780311	14-Jun-1998
5782975	21-Jul-1998
5789949	04-Aug-1998
5789982	04-Aug-1998
5790060	04-Aug-1998
5793193	11-Aug-1998
5798557	25-Aug-1998
5798724	29-Aug-1998
5801084	01-Sep-1998
5804846	08-Sep-1998
5805020	08-Sep-1998
5807780	15-Sep-1998
5807783	15-Sep-1998
5808348	15-Sep-1998
5808353	15-Sep-1998
5808489	15-Sep-1998
5808883	15-Sep-1998
5809410	15-Sep-1998
5812029	22-Sep-1998
5812658	22-Sep-1998
5814889	29-Sep-1998
5817564	06-Oct-1998
5821740	13-Oct-1998
5825092	20-Oct-1998
5830048	03-Nov-1998
5830279	03-Nov-1998
5831423	03-Nov-1998
5833758	10-Nov-1998
5837553	17-Nov-1998

Patent Number	Issue Date
5837603	17-Nov-1998
5841169	24-Nov-1998
5841182	24-Nov-1998
5841324	24-Nov-1998
5849627	15-Dec-1998
5851864	22-Dec-1998
5856695	05-Jan-1999
5856700	05-Jan-1999
5856742	05-Jan-1999
5861826	19-Jan-1999
5870266	09-Feb-1999
5872028	16-Feb-1999
5872044	16-Feb-1999
5877041	02-Mar-1999
5877044	02-Mar-1999
5880513	09-Mar-1999
5882423	16-Mar-1999
5883414	16-Mar-1999
5883565	16-Mar-1999
5883921	16-Mar-1999
5892223	06-Apr-1999
5892264	06-Apr-1999
5892375	06-Apr-1999
5892472	06-Apr-1999
5894141	13-Apr-1999
5895953	20-Apr-1999
5896053	20-Apr-1999
5900643	04-May-1999
5913130	15-Jun-1999
5914280	22-Jun-1999
5915168	22-Jun-1999
5920108	06-Jul-1999
5920219	06-Jul-1999
5920224	06-Jul-1999
5920452	06-Jul-1999
5923207	13-Jul-1999
5923209	13-Jul-1999
B1 5051619	02-Mar-1993

PATENT ASSIGNMENT

Electronic Version v1.1
Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	CHANGE OF NAME
CONVEYING PARTY DATA	
Name	Execution Date
INTERSIL CORPORATION	05/25/2001
RECEIVING PARTY DATA	
Name:	INTERSIL COMMUNICATIONS, INC.
Street Address:	1001 Murphy Ranch Road
City:	Milpitas
State/Country:	CALIFORNIA
Postal Code:	95035
PROPERTY NUMBERS Total: 2	
Property Type	Number
Patent Number:	4823173
Patent Number:	5264719
CORRESPONDENCE DATA	
Fax Number:	(703)931-6037
<i>Correspondence will be sent via US Mail when the fax attempt is unsuccessful.</i>	
Phone:	2022363707
Email:	wgwalter@aol.com
Correspondent Name:	Wallace G. Walter
Address Line 1:	5726 Clarence Ave
Address Line 4:	Alexandria, VIRGINIA 22311
NAME OF SUBMITTER:	Wallace G. Walter
Total Attachments: 4 source=IntersilNameChange#page1.tif source=IntersilNameChange#page2.tif source=IntersilNameChange#page3.tif source=IntersilNameChange#page4.tif	

CH \$80.00 4823173

Delaware

PAGE 1

The First State

I, HARRIET SMITH WINDSOR, SECRETARY OF STATE OF THE STATE OF DELAWARE, DO HEREBY CERTIFY THE ATTACHED IS A TRUE AND CORRECT COPY OF THE RESTATED CERTIFICATE OF "INTERSIL CORPORATION", CHANGING ITS NAME FROM "INTERSIL CORPORATION" TO "INTERSIL COMMUNICATIONS, INC.", FILED IN THIS OFFICE ON THE TWENTY-FIFTH DAY OF MAY, A.D. 2001, AT 4:15 O'CLOCK P.M.



Harriet Smith Windsor

3050122 8100

050839147

DATE: 10-13-05

PATENT

REEL: 017468 FRAME: 0603

**AMENDED AND RESTATED CERTIFICATE OF INCORPORATION
OF
INTERSIL CORPORATION**

INTERSIL CORPORATION, a corporation organized and existing under the laws of the State of Delaware, hereby certifies as follows:

FIRST: The present name of the corporation is INTERSIL CORPORATION and the name under which the corporation was originally incorporated is HSS Operating Corporation. The date of filing of its original Certificate of Incorporation with the Secretary of State of the State of Delaware was June 2, 1999.


SECOND: This Amended and Restated Certificate of Incorporation (the "Certificate") restates and integrates and further amends in its entirety the Certificate of Incorporation of this corporation. This Certificate was duly adopted by a majority vote of the stockholders of the corporation in accordance with Sections 228, 242 and 245 of the General Corporation Law of the State of Delaware.

THIRD: This Certificate shall become effective immediately upon its filing with the Secretary of State of the State of Delaware.

FOURTH: Upon the filing of the Certificate with the Secretary of State of the State of Delaware, the Certificate of Incorporation of the corporation shall be amended and restated in its entirety to read as set forth on Exhibit A attached hereto.

IN WITNESS WHEREOF, said corporation has caused this Certificate to be executed by a duly authorized officer this 23rd day of May, 2001.

By:


Gregory Williams
Chief Executive Officer

740322.2.01 5/24/2001 3:35 PM

STATE OF DELAWARE
SECRETARY OF STATE
DIVISION OF CORPORATIONS
FILED 04:15 PM 05/25/2001
010253080 - 3050122

**PATENT
REEL: 017468 FRAME: 0604**

EXHIBIT A

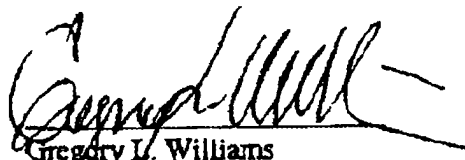
**AMENDED AND RESTATED CERTIFICATE OF INCORPORATION
OF
INTERSIL COMMUNICATIONS, INC.**

1. **Name.** The name of the Corporation is **Intersil Communications, Inc.**
2. **Registered Office and Agent.** The address of the Corporation's registered office in the State of Delaware is 1209 Orange Street, in the City of Wilmington, County of New Castle. The name of the Corporation's registered agent at such address is The Corporation Trust Company.
3. **Purpose.** The purposes for which the Corporation is formed are to engage in any lawful act or activity, including, without limitation, forming and/or acquiring foreign subsidiaries, for which corporations may be organized under the General Corporation Law of the State of Delaware ("DGCL") and to possess and exercise all of the powers and privileges granted by such law and any other law of Delaware.
4. **Authorized Capital.** The aggregate number of shares of stock which the Corporation shall have authority to issue is One Thousand (1,000) shares, all of which are of one class and are designated as Common Stock, par value \$.01 per share.
5. **Incorporator.** The name and mailing address of the incorporator are Marian T. Ryan, 4000 Bell Atlantic Tower, 1717 Arch Street, Philadelphia, Pennsylvania 19103-2793.
6. **Bylaws.** In furtherance and not in limitation of the powers conferred by law, the board of directors of the Corporation is authorized to adopt, amend or repeal the bylaws of the Corporation, except as otherwise specifically provided therein, subject to the powers of the stockholders of the Corporation to amend or repeal any bylaws adopted by the board of directors.
7. **Elections of Directors.** Elections of directors need not be by written ballot unless and except to the extent the bylaws of the Corporation shall so provide.
8. **Right to Amend.** The corporation reserves the right to amend or repeal any provision contained in this Certificate as the same may from time to time be in effect in the manner now or hereafter prescribed by law, and all rights, preferences and privileges conferred on stockholders, director or others hereunder are subject to such reservation.
9. **Unanimous Written Consent Required.** If any action is to be taken by stockholders without a meeting, such action must be authorized by unanimous written consent signed by a l of the holders of outstanding voting stock.

10. *Limitation on Liability.* The directors of the Corporation shall be entitled to the benefits of all limitations on the liability of directors generally that are now or hereafter become available under the DGCL. Without limiting the generality of the foregoing, to the fullest extent permitted by the DGCL, as it exists on the date hereof or as it may hereafter be amended, no director of the Corporation shall be personally liable to the Corporation or its stockholders for monetary damages for breach of fiduciary duty as a director, except for liability (i) for any breach of the director's duty of loyalty to the Corporation or its stockholders, (ii) for acts or omissions not in good faith or which involve intentional misconduct or a knowing violation of law, (iii) under Section 174 of the DGCL, or (iv) for any transaction from which the director derived an improper personal benefit. Any repeal or modification of this Section 10 shall be prospective only, and shall not affect, to the detriment of any director, any limitation on the personal liability of a director of the Corporation existing at the time of such repeal, modification or adoption.

Dated: May 23, 2001

By:



Gregory L. Williams
Chief Executive Officer

PATENT ASSIGNMENT

Electronic Version v1.1

Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT
CONVEYING PARTY DATA	
Name	Execution Date
INTERSIL COMMUNICATIONS, INC.	12/21/2001
RECEIVING PARTY DATA	
Name:	INTERSIL AMERICAS, INC.
Street Address:	1001 MURPHY RANCH ROAD
City:	MILPITAS
State/Country:	CALIFORNIA
Postal Code:	95035
PROPERTY NUMBERS Total: 2	
Property Type	Number
Patent Number:	4823173
Patent Number:	5264719
CORRESPONDENCE DATA	
Fax Number:	(703)931-6037
<i>Correspondence will be sent via US Mail when the fax attempt is unsuccessful.</i>	
Phone:	2022363707
Email:	wgwalter@aol.com
Correspondent Name:	Wallace G. Walter
Address Line 1:	5726 Clarence Ave.
Address Line 4:	Alexandria, VIRGINIA 22311
NAME OF SUBMITTER:	Wallace G. Walter
Total Attachments: 4 source=IntersilContribAgmt#page1.tif source=IntersilContribAgmt#page2.tif source=IntersilContribAgmt#page3.tif source=IntersilContribAgmt#page4.tif	

CH \$80.00 4823173

CONTRIBUTION AGREEMENT

This Contribution Agreement (the "Agreement") is effective as of December 31, 2001 (the "Effective Date") at 11:59 PM United States of America EST (the "Effective Time") by and between Intersil Communications, Inc., a Delaware corporation ("Intersil"), and Intersil Americas Inc., a Delaware corporation ("Intersil Americas").

Background

To promote greater efficiency and economy in the management of the businesses carried on by the parties to this Agreement, Intersil desires to make a capital contribution to Intersil Americas of certain intellectual property and other assets used in the business of Intersil and its affiliates.

Terms

Intending to be legally bound, the parties to this Agreement agree as follows:

1. Effective as of the date first written above, Intersil shall contribute the following to Intersil Americas, in deemed exchange for stock of Intersil Americas in a non-recognition transaction as described in Section 351 of the Internal Revenue Code of 1986, as amended:

(i) all right, title and interest in and to the trademarks shown in Schedule A and all slogans, logotypes, designs, and trade dress associated therewith (the "Trademarks"), together with the U.S. federal registrations and applications for registration of the Trademarks, in and to all income, royalties, damages and payments now or hereafter due or payable with respect thereto and in and to all rights of action arising from the Trademarks, to be held and enjoyed by Intersil Americas for its own use and benefit and for its successors and assigns as the same would have been held by Intersil had this contribution not been made, and the goodwill of the business symbolized by the Trademarks;

(ii) all right, title and interest in and to the U.S. patents and patent applications shown in Schedule A (the "Patents"), including all reissues, divisions, continuations, continuations-in-part, and extensions thereof, to be held and enjoyed by Intersil Americas as fully and entirely as they would have been held and enjoyed by Intersil if this contribution had not been made, including all licenses of and proceeds from the Patents, all claims, demands and rights to recovery that Intersil has or may have in profits and damages for past and future infringements, if any, and all rights to compromise, sue for, and collect such profits and damages;

(iii) all right, title, and interest in and to all inventions shown in Schedule A (the "Inventions"), and all intellectual property rights relating thereto, including, without limitation, trade secret rights in the Inventions, and all rights of action arising from the Inventions, to be held and enjoyed by Intersil Americas for its own use and benefit and for its successors and assigns as the same would have been held by Intersil had this contribution not been made; and

(iv) all right, title, and interest in and to all copyrights owned by Intersil as of the date first written above that are not otherwise excluded from contribution under the terms of this Agreement, whether or not such copyrights have been registered (collectively, the "Copyrights")

including, without limitation, all U.S. registrations and applications for registration of the Copyrights, all licenses of and proceeds from the Copyrights, all publishing, electronic publishing, and other proprietary rights arising from or related to the Copyrights, all causes of action relating to the Copyrights that may have arisen prior to this contribution, and any recovery resulting from such causes of action.

Notwithstanding the foregoing or any specific item listed on Schedule A, the intellectual property used in connection with providing products or services that are regulated by the United States Department of State shall not be contributed to Intersil Americas.

2. Intersil and Intersil Americas shall each take any and all additional actions as may be necessary or appropriate to effect the transactions contemplated by this Agreement. Such actions may include, without limitation, the execution of additional documents to record the contribution made in this Agreement and the filing of such documents with the appropriate governmental authorities.

[Signatures commence on the following page]

IN WITNESS WHEREOF, the parties have caused this Agreement to be executed as of the date below to be effective as of the Effective Date and Effective Time.

INTERSIL COMMUNICATIONS, INC.
a Delaware corporation

By: Paul A. Bernkopf Date: 12/21/01
Name: PAUL A. BERNKOPF
Title: ASST. SECRETARY

INTERSIL AMERICAS INC.
a Delaware Corporation

By: Paul A. Bernkopf Date: 12/21/01
Name: PAUL A. BERNKOPF
Title: ASST. SECRETARY

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

ClientRef	SubCase	Status	Apl #	FileDate	Pat#	IssDate	Title
SE-358		Granted	774474	10-Sep-1985	4677321	30-Jun-1987	A TTL COMPATIBLE INPUT BUFFER
SE352		Granted	793316	31-Oct-1985	4682059	21-Jul-1987	A COMPARATOR INPUT STAGEFOR INTERFACE WITH SIGNAL CURRENT
SE-359		Granted	782691	01-Oct-1985	4650896	17-Mar-1987	PROCESS USING TUNGSTEN FOR MULTILEVEL METALIZATION
SE-363		Granted	936609	01-Dec-1986	4781853	01-Nov-1988	METHOD OF ETCH & ENHANC SILICON ETCHING CAP OF ALKALI HYDROXIDE THROUGH ADD OF POSITIVE VALENCE IMPURITY IONS
SE-363	A	Granted	187268	28-Apr-1988	4859280	22-Aug-1989	METHOD OF ETCH & ENHANC SILICON ETCHING CAP OF ALKALI HYDROXIDE THROUGH ADD OF POSITIVE VALENCE IMPURITY IONS
SE-370		Granted	723238	15-Apr-1985	4705596	10-Nov-1987	SIMULTANEOUS PLASMA SCULPTURING AND DUAL TAPERED VIA ETCH
SE377		Granted	782689	01-Oct-1985	4636744	13-Jan-1987	FRONT END OF AN OPERATIONAL AMPLIFIER
SE704		Granted	771712	03-Sep-1985	4624749	25-Nov-1986	ELECTRODEPOSITION OF SUBMICROMETER METALLIC INTERCONNECT FOR INTEGRATED CIRCUITS
SE-705		Granted	768328	22-Aug-1985	4716071	29-Dec-1987	METHOD FOR ENSURING ADHESION OF CHEMICALLY VAPOR DEPOSITED OXIDE TO GOLD INTEGRATED CIRCUIT INTERCONNECT LINES
SE-705	A	Granted	045526	04-May-1987	4713260	15-Dec-1987	METHOD FOR ENSURING ADHESION OF CHEMICALLY VAPOR DEPOSITED OXIDE TO GOLD INTEGRATED CIRCUIT INTERCONNECT LINES
SE-385		Granted	896097	13-Aug-1986	4755770	05-Jul-1988	LOW NOISE CURRENT SPECTRAL DENSITY INPUT BIAS CURRENT CANCEL SCHEME
SE-394		Granted	723239	15-Apr-1985	4705597	10-Nov-1987	PHOTORESIST TAPERING PROCESS
SE-395		Granted	831384	07-Jan-1986	4823173	18-Apr-1989	HIGH VOLTAGE LATERAL MOS STRUCTURE WITH DEPLETED TOP GATE REGION
SE-395	B	Granted	07705509	24-May-1991	5264719	23-Nov-1993	HIGH VOLTAGE LATERAL MOS STRUCTURE WITH DEPLETED TOP GATE REGION

Patent License Agreement

This Patent License Agreement ("PLA") is entered into on this 30th day of March, 2006 by and between Intersil Corporation ("Intersil") and Fairchild Semiconductor Corporation ("Fairchild") (collectively, the "Parties").

1.

REDACTED

1.1

1.2

Power Integrations, Incorporated, including its parents, subsidiaries and consolidated entities (any or all of which, "POWI"). **REDACTED**

United States Patent No. 4,823,173 and/or United States Patent No. 5,264,719, including any and all re-examinations, reissues or certificates of correction relating to such patents (collectively, the "Patents").

1.3

REDACTED

2.

2.1

REDACTED

2.2

3. **Additional Rights Granted Fairchild**

3.1

REDACTED

Intersil

grants to Fairchild the sole and exclusive right, exclusive even as to Intersil, to enforce the Patents against POWI, to assert, litigate and prosecute claims of Infringement under the Patents against POWI, including without limitation in any U.S. federal court or before the International Trade Commission, and to seek all equitable, injunctive, monetary and other relief and to collect for later distribution under Paragraph 1.2 any and all past damages in connection with Infringement of the Patents by POWI, and to settle and compromise any disputes with POWI related to the Patents. Except as provided herein, the Parties agree that only Fairchild shall have the authority to threaten, commence, maintain or settle any claim, suit or proceeding based upon Infringement of the Patents (or other trespass or similar action relating to the Patents and the inventions therein claimed) by POWI.

3.2

3.3

REDACTED

REDACTED

3.4

3.5

REDACTED

3.6

4. **Representations and Warranties**

4.1 Intersil represent and warrants as follows:

A. Intersil has the authority to enter into this PLA and to convey the rights conveyed herein, and that the execution and performance of this PLA does not conflict with Intersil's certificate of incorporation, by-laws or contract obligations.

B. Intersil is the sole owner of the Patents, the Patents have been and will be maintained, and that all inventors of the inventions claimed in the Patents have assigned title and ownership of the inventions to Intersil.

C.

4.2

A.

REDACTED

B.

C.

5. **Confidentiality**

The terms and conditions of this PLA, all communications, discussions and correspondence relating to this PLA, and all actions taken in performance of the PLA, shall be "Common Interest Information" covered by the Joint Defense and Confidentiality Agreement between the Parties, dated March 12, 2001, and shall be maintained in strict confidence in accordance with such Joint Defense and Confidentiality Agreement.

REDACTED

The parties have duly executed this Agreement as of the date first above written.

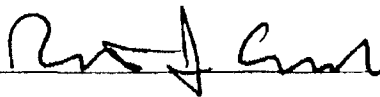
INTERSIL CORPORATION

By: _____

Name: _____

Title: _____

FAIRCHILD SEMICONDUCTOR CORPORATION

By:  _____

Name: Robert J. Conrad

Title: Senior Vice President – Analog Products

The parties have duly executed this Agreement as of the date first above written.

INTERSIL CORPORATION

By: Douglas A. Balog

Name: DOUGLAS A. BALOG

Title: ASST. SECRETARY

FAIRCHILD SEMICONDUCTOR CORPORATION

By: _____

Name: Robert J. Conrad

Title: Senior Vice President – Analog Products

Supplemental Agreement

This Supplemental Agreement amends and, to the extent necessary, modifies *nunc pro tunc* the Patent License Agreement ("PLA") dated March 30, 2006 between Intersil Corporation ("Intersil") and Fairchild Semiconductor Corporation ("Fairchild") (collectively, the "Parties").

Intersil Americas, Inc. ("Intersil Americas"), as title holder of record of United States Patent No. 4,823,173 and United States Patent No. 5,264,719 (the "Patents"), hereby fully ratifies the terms of the March 30, 2006 PLA. Intersil Americas further acknowledges that its parent corporation, Intersil Corporation, was authorized to enter into the PLA on behalf of Intersil Americas, and to agree to the terms stated therein. Intersil Americas agrees to be bound by, and hereby reaffirms, the representations and warranties made by Intersil Corporation in the PLA.

It is the intent of the parties hereto that this Supplemental Agreement shall be retroactive to March 30, 2006, and shall have the effect of assigning and conveying from Intersil Americas to Fairchild, as of March 30, 2006, the specific rights to the Patents as detailed in the PLA as if Intersil Americas – and not Intersil Corporation – was the original party to the PLA. This Supplemental Agreement does not modify the substantive rights of Fairchild under the PLA, and the substantive rights afforded to Intersil Corporation under the PLA remain unchanged, but will be deemed to reside in Intersil Americas. Intersil Corporation shall remain bound under the PLA itself. This Supplemental Agreement does not alter the ongoing obligations, if any, of any Intersil related entity under the Asset Purchase Agreement and the related Intellectual Property Assignment and License Agreement between Intersil Corporation and Fairchild dated January 20, 2001. Intersil Americas assumes no obligations other than as expressly set forth herein and in the body of the PLA.

Executed on May 18, 2006, but effective March 30, 2006.

INTERSil CORPORATION

By: Douglas A. Balog
Name: DOUGLAS A. BALOG
Title: ASST. SECRETARY

INTERSil AMERICAS, INC.

By: Douglas A. Balog
Name: DOUGLAS A. BALOG
Title: ASST. SECRETARY

FAIRCHILD SEMICONDUCTOR CORPORATION

By: Paul D. Deluca
Name: PAUL D. DELUCA
Title: SVP, GENERAL COUNSEL & SECRETARY

IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS

FAIRCHILD SEMICONDUCTOR
CORPORATION, a Delaware corporation,
INTERSIL AMERICAS, INC., a Delaware
corporation and INTERSIL CORPORATION,
a Delaware corporation

Plaintiff,

v.

POWER INTEGRATIONS, INC., a Delaware
corporation,

Defendants.

JURY

CIVIL ACTION NO. 2:06-cv-151

PLAINTIFFS' AMENDED COMPLAINT

Plaintiffs FAIRCHILD SEMICONDUCTOR CORPORATION (hereinafter, "Fairchild"),
INTERSIL AMERICAS, INC. and INTERSIL CORPORATION, (Intersil Americas, Inc. and
Intersil Corp. are collectively "Intersil") by and through their undersigned counsel, hereby
alleges as follows:

THE PARTIES

1. Fairchild Semiconductor Corporation is a Delaware corporation with its principal
place of business in South Portland, Maine.

2. Intersil Corporation is a Delaware corporation with its principal place of business
in Milpitas, California.

3. Intersil Americas, Inc. is a Delaware corporation with its principal place of
business in Milpitas, California.

4. Power Integrations, Inc. is a Delaware is a Delaware corporation with its principal
place of business in San Jose, California.

JURISDICTION AND VENUE

5. This is an action arising under the patent laws of the United States, Title 35 of the United States Code. This court has jurisdiction over the subject matter of this action pursuant to 28 U.S.C. §§ 1331 and 1338(a).

6. Upon information and belief, this Court has personal jurisdiction over the defendant because Power Integrations sells the accused devices within this district.

7. Upon information and belief, venue is proper in the Court pursuant to 28 U.S.C. § 1391(b) and (c) and § 1400 as the defendant is subject to personal jurisdiction in this district.

FIRST CAUSE OF ACTION

INFRINGEMENT OF U.S. PATENT NO. 5,264,719

8. The allegations of paragraphs 1-7 are incorporated as though fully set forth herein.

9. U.S. Patent No. 5,264,719 (the “719 Patent”), entitled *High Voltage Lateral Semiconductor Device*, duly and lawfully issued on November 23, 1993 and was assigned to Harris Corporation. A true and correct copy of the ‘719 Patent is attached hereto as Exhibit A.

10. Upon information and belief, on or about September 27, 1999 the ‘719 Patent was assigned by Harris Corporation to Intersil Corporation. A true and correct copy of that assignment is attached as Exhibit B.

11. Upon information and belief, on or about April 14, 2006, Intersil Corporation changed its name to Intersil Communications, Inc. A true and correct copy of the restated certificate of incorporation is attached as Exhibit C.

12. Upon information and belief, on or about April 14, 2006 the ‘719 Patent was assigned by Intersil Communications, Inc. to Intersil Americas, Inc. A true and correct copy of that assignment is attached as Exhibit D.

13. On or about March 30, 2006, Fairchild Semiconductor Corporation and Intersil Corporation entered into a Patent License Agreement that gave Fairchild the right to assert the

'719 Patent against Power Integrations. A redacted copy of that Patent License Agreement is attached as Exhibit E.

14. On or about May 17, 2006, Fairchild Semiconductor Corporation, Intersil Corporation, and Intersil Americas, Inc. entered into a Supplemental Agreement effective March 30, 2006 that gave Fairchild the right to assert the '719 Patent against Power Integrations. A true and correct copy of that Supplemental Agreement is attached as Exhibit F.

15. Upon information and belief, Power Integrations has been and is now infringing the '719 Patent, both literally and under the doctrine of equivalents, by making, using, selling, offering for sale, and importing devices and products in the United States covered by one or more claims of the '719 Patent.

16. Upon information and belief, Power Integrations has been and is now inducing infringement and contributing to the infringement of the '719 Patent, both literally and under the doctrine of equivalents, by inducing or contributing to the making, using, selling, offering for sale, and importing by others devices and products in the United States covered by one or more claims of the '719 Patent.

17. Power Integrations' infringement has caused irreparable injury to Fairchild and Intersil and will continue to cause irreparable injury until Power Integrations is enjoined from further infringement by the Court.

PRAYER FOR RELIEF

WHEREFORE, FAIRCHILD and INTERSIL pray for the following relief:

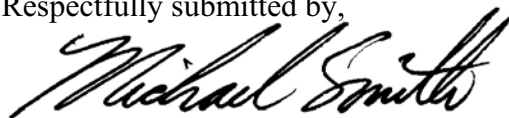
- A. Judgment by the Court that Power Integrations directly infringes the '719 Patent;
- B. Judgment by the Court that Power Integrations induces or contributes to others' infringement of the '719 Patent;
- C. Preliminary and permanent injunctive relief pursuant to 35 U.S.C. § 283 enjoining Power Integrations, its officers, agents, servants, employees, successors, assigns and all other persons or entities acting in concert or participation with Power Integrations or on Power Integrations' behalf from further infringement of the '719 Patent;

- D. Money damages sustained as a result of Power Integrations' infringement of the '719 Patent;
- E. Costs and reasonable attorneys' fees incurred in connection with this action pursuant to 35 U.S.C. § 285; and,
- F. Such other relief as the Court finds just and proper.

DEMAND FOR JURY TRIAL

Pursuant to Rule 38(b) of the Federal Rules of Civil Procedure, Fairchild Semiconductor Corporation and Intersil Corporation hereby demand a trial by jury on this action.

Respectfully submitted by,



ORRICK, HERRINGTON & SUTCLIFFE LLP
G. Hopkins Guy, III (SBN 124811)
Bas de Blank (SBN 191487)
1000 Marsh Road
Menlo Park, CA 94025
(650) 614-7400

Carl R. Roth, Texas Bar No. 901984225
cr@rothfirm.com
Michael C. Smith, Texas Bar No. 900641877
ms@rothfirm.com
THE ROTH LAW FIRM, P.C.
115 North Wellington, Suite 200
P.O. Box 876
Marshall, Texas 75671
Tel: (903) 935-1665
Fax: (903) 935-1797


Attorneys for Plaintiffs,
FAIRCHILD SEMICONDUCTOR
CORPORATION, INTERSIL CORPORATION,
and INTERSIL AMERICAS, INC.

SHORE CHAN, L.L.P.
Michael Shore, Texas Bar No. 18294915
shore@shorechan.com
Jeffrey R. Bragalone, Texas Bar No. 02855775
jbragalone@shorechan.com
325 North St. Paul, Suite 4450
Dallas, Texas 75201
Tel: (214) 593-9110
Fax: (214) 593-9111

Attorneys for Plaintiffs,
INTERFIL CORPORATION, and INTERFIL
AMERICAS, INC.

CERTIFICATE OF SERVICE

The undersigned hereby certifies that all counsel of record who are deemed to have consented to electronic service are being served with a copy of this document via the Court's CM/ECF system per Local Rule CV-5(a)(3) this 19th day of May, 2006. Any other counsel of record will be served by facsimile transmission and/or first class mail.



Michael C. Smith

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

POWER INTEGRATIONS, INC., a
Delaware corporation,

Plaintiff,

v.

FAIRCHILD SEMICONDUCTOR
INTERNATIONAL, INC., a Delaware
corporation, and FAIRCHILD
SEMICONDUCTOR CORPORATION, a
Delaware corporation

Defendants.

C.A. No. 047-1371-JJF

JURY TRIAL REQUESTED

FIRST AMENDED COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Power Integrations, Inc. hereby alleges as follows:

THE PARTIES

1. Power Integrations, Inc. ("Power Integrations") is incorporated under the laws of the state of Delaware, and has a regular and established place of business at 5245 Hellyer Avenue, San Jose, California, 95138.

2. Upon information and belief, defendant Fairchild Semiconductor International, Inc. is incorporated under the laws of the state of Delaware, with its headquarters located at 82 Running Hill Road, South Portland, Maine, 04106. Upon information and belief, defendant Fairchild Semiconductor Corporation is incorporated under the laws of the state of Delaware, with its headquarters located at 82 Running Hill Road, South Portland, Maine, 04106. (Fairchild Semiconductor International, Inc. and Fairchild Semiconductor Corporation hereinafter collectively "Fairchild Semiconductor.")

JURISDICTION AND VENUE

3. This action arises under the patent laws of the United States, Title 35 U.S.C. § 1 *et seq.* This Court has subject matter jurisdiction under 28 U.S.C. §§ 1331 and 1338(a).

4. Upon information and belief, this Court has personal jurisdiction over defendants because defendants are incorporated, doing business and advertising in this judicial District.

5. Upon information and belief, venue is proper in this Court pursuant to 28 U.S.C. §§ 1391(b), (c) and 1400 because the defendants are subject to personal jurisdiction in this judicial District.

GENERAL ALLEGATIONS

6. Power Integrations' products include its integrated pulse width modulation ("PWM") integrated circuits that are used in power supplies for electronic devices such as cellular telephones, LCD monitors and computers. These products are sold throughout the United States, including Delaware.

7. Upon information and belief, defendants manufacture PWM integrated circuits devices (e.g., devices intended for use in power conversion applications such as LCD monitor power supplies or battery chargers for portable electronics), and directly and through their affiliates, uses, imports, sells, and offers to sell the same throughout the United States, including Delaware.

FIRST CAUSE OF ACTION

INFRINGEMENT OF U.S. PATENT NO. 6,107,851

8. The allegations of paragraphs 1-7 are incorporated as though fully set forth herein.

9. Power Integrations is now, and has been since its issuance, the assignee and sole owner of all right, title, and interest in United States Patent No. 6,107,851, entitled "Offline Converter with Integrated Softstart and Frequency Jitter" ("the '851

patent”), which was duly and legally issued on August 22, 2000. A true and correct copy of the ’851 patent is attached hereto as Exhibit A.

10. Upon information and belief, defendants have been and are now infringing, inducing infringement, and contributing to the infringement of the ’851 patent by making, using, importing, selling, and offering to sell devices, including PWM integrated circuit devices, and/or inducing or contributing to the importation, use, offer for sale and sale by others of such devices covered by one or more claims of the ’851 patent, all to the injury of Power Integrations.

11. Defendants’ acts of infringement have injured and damaged Power Integrations.

12. Defendants’ infringement has caused irreparable injury to Power Integrations and will continue to cause irreparable injury until defendants are enjoined from further infringement by this Court.

13. Upon information and belief, Defendants’ infringement has been, and continues to be, willful so as to warrant enhancement of damages awarded as a result of its infringement.

SECOND CAUSE OF ACTION

INFRINGEMENT OF U.S. PATENT NO. 6,249,876

14. The allegations of paragraphs 1-7 are incorporated as though fully set forth herein.

15. Power Integrations is now, and has been since its issuance, the assignee and sole owner of all right, title, and interest in United States Patent No. 6,249,876, entitled “Frequency Jittering Control for Varying the Switching Frequency of a Power Supply” (“the ’876 patent”), which was duly and legally issued on June 19, 2001. A true and correct copy of the ’876 patent is attached hereto as Exhibit B.

16. Upon information and belief, defendants have been and are now infringing, inducing infringement, and contributing to the infringement of the ’876 patent

by making, using, importing, selling, and offering to sell devices, including PWM integrated circuit devices and/or inducing or contributing to the importation, use, offer for sale and sale by others of such devices covered by one or more claims of the '876 patent, all to the injury of Power Integrations.

17. Defendants' acts of infringement have injured and damaged Power Integrations.

18. Defendants' infringement has caused irreparable injury to Power Integrations and will continue to cause irreparable injury until defendants are enjoined from further infringement by this Court.

19. Upon information and belief, Defendants' infringement has been, and continues to be, willful so as to warrant enhancement of damages awarded as a result of its infringement.

THIRD CAUSE OF ACTION

INFRINGEMENT OF U.S. PATENT NO. 6,229,366

20. The allegations of paragraphs 1-7 are incorporated as though fully set forth herein.

21. Power Integrations is now, and has been since its issuance, the assignee and sole owner of all right, title, and interest in United States Patent No. 6,229,366, entitled "Off-Line Converter with Integrated Softstart and Frequency Jitter" ("the '366 patent"), which was duly and legally issued on May 8, 2001. A true and correct copy of the '366 patent is attached hereto as Exhibit C.

22. Upon information and belief, defendants have been and are now infringing, inducing infringement, and contributing to the infringement of the '366 patent by making, using, importing, selling, and offering to sell devices, including PWM integrated circuit devices and/or inducing or contributing to the importation, use, offer for

sale and sale by others of such devices covered by one or more claims of the '366 patent, all to the injury of Power Integrations.

23. Defendants' acts of infringement have injured and damaged Power Integrations.

24. Defendants' infringement has caused irreparable injury to Power Integrations and will continue to cause irreparable injury until defendants are enjoined from further infringement by this Court.

25. Upon information and belief, Defendants' infringement has been, and continues to be, willful so as to warrant enhancement of damages awarded as a result of its infringement.

FOURTH CAUSE OF ACTION

INFRINGEMENT OF U.S. PATENT NO. 4,811,075

26. The allegations of paragraphs 1-7 are incorporated as though fully set forth herein.

27. Power Integrations is now, and has been since its issuance, the assignee and sole owner of all right, title, and interest in United States Patent No. 4,811,075, entitled "High Voltage MOS Transistors" ("the '075 patent"), which was duly and legally issued on March 7, 1989. A true and correct copy of the '075 patent is attached hereto as Exhibit D.

28. Upon information and belief, defendants have been and are now infringing, inducing infringement, and contributing to the infringement of the '075 patent by making, using, importing, selling, and offering to sell devices, including PWM integrated circuit devices and/or inducing or contributing to the importation, use, offer for sale and sale by others of such devices covered by one or more claims of the '075 patent, all to the injury of Power Integrations.

29. Defendants' acts of infringement have injured and damaged Power Integrations.

30. Defendants' infringement has caused irreparable injury to Power Integrations and will continue to cause irreparable injury until defendants are enjoined from further infringement by this Court.

31. Upon information and belief, Defendants' infringement has been, and continues to be, willful so as to warrant enhancement of damages awarded as a result of its infringement.

PRAYER FOR RELIEF

WHEREFORE, Plaintiff requests the following relief:

- (a) judgment against defendants as to willful infringement of the '851 patent;
- (b) judgment against defendants as to willful infringement of the '876 patent;
- (c) judgment against defendants as to willful infringement of the '366 patent;
- (d) judgment against defendants as to willful infringement of the '075 patent;
- (e) a permanent injunction preventing defendants and their officers, directors, agents, servants, employees, attorneys, licensees, successors, assigns, and customers, and those in active concert or participation with any of them, from making, using, importing, offering to sell or selling any devices that infringe any claim of the '851, '876, '366, or '075 patents;
- (f) judgment against defendants for money damages sustained as a result of defendants' infringement of the '851, '876, '366, and '075 patents;
- (g) that any such money judgment be trebled as a result of the willful nature of Defendants' infringement;
- (h) costs and reasonable attorneys' fees incurred in connection with this action pursuant to 35 U.S.C § 285; and
- (i) such other and further relief as this Court finds just and proper.

JURY DEMAND

Plaintiff requests trial by jury.

Dated: October 20, 2004

FISH & RICHARDSON P.C.

By: /s/ John F. Horvath

William J. Marsden, Jr. (#2247)
Sean P. Hayes (#4413)
John F. Horvath (#4557)
919 N. Market Street, Suite 1100
P.O. Box 1114
Wilmington, DE 19801
Telephone: (302) 652-5070
Facsimile: (302) 652-0607

Frank E. Scherkenbach
225 Franklin Street
Boston, MA 02110-2804
Telephone: (617) 542-5070
Facsimile: (617) 542-8906

Michael Kane
60 South Sixth Street
3300 Dain Rauscher Plaza
Minneapolis, MN 55402
Telephone: (612) 335-5070
Facsimile: (612) 288-9696

Howard G. Pollack
Gina M. Steele
Michael R. Headley
500 Arguello Street, Suite 500
Redwood City, CA 94063
Telephone: (650) 839-5070
Facsimile: (650) 839-5071

Attorneys for Plaintiff
POWER INTEGRATIONS, INC.

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

POWER INTEGRATIONS, INC.,)	
)	
Plaintiff,)	
)	
v.)	C.A. No. 04-1371-JJF
)	
FAIRCHILD SEMICONDUCTOR)	
INTERNATIONAL, INC., and FAIRCHILD)	
SEMICONDUCTOR CORPORATION,)	
)	
Defendants.)	

**DEFENDANTS FAIRCHILD SEMICONDUCTOR INTERNATIONAL, INC.
AND FAIRCHILD SEMICONDUCTOR CORPORATION'S FIRST AMENDED
ANSWER AND COUNTERCLAIMS TO PLAINTIFF'S FIRST AMENDED
COMPLAINT FOR PATENT INFRINGEMENT AND DEMAND FOR JURY TRIAL**

Defendants Fairchild Semiconductor International, Inc. and Fairchild Semiconductor Corporation (collectively "FAIRCHILD") answer the First Amended Complaint of Power Integrations, Inc. ("PI") as follows:

FAIRCHILD denies each and every allegation contained in the First Amended Complaint, except as hereinafter specifically admitted or explained. To the extent that the headings, or any other non-numbered statements in Plaintiff's First Amended Complaint contain any allegations, Defendants deny each and every allegation therein.

THE PARTIES

1. In response to paragraph 1 of the First Amended Complaint, FAIRCHILD lacks sufficient knowledge or information to admit or deny the allegations set forth therein and therefore denies each and every allegation contained in paragraph 1.

2. In response to paragraph 2 of the First Amended Complaint, defendant Fairchild Semiconductor International, Inc. admits that it is a corporation duly incorporated under the laws of the State of Delaware, with its headquarters located at 82 Running Hill Road, South Portland, Maine, 04106. Defendant Fairchild Semiconductor Corporation admits that it is a corporation

duly incorporated under the laws of the State of Delaware, with its headquarters located at 82 Running Hill Road, South Portland, Maine, 04106. FAIRCHILD denies any and all remaining allegation of paragraph 2.

JURISDICTION AND VENUE

3. In response to paragraph 3 of the First Amended Complaint, FAIRCHILD denies that it has infringed or now infringes the patents asserted against FAIRCHILD in the First Amended Complaint. FAIRCHILD admits that the First Amended Complaint purports to state a cause of action under the patent laws of the United States, Title 35 U.S.C. § 1 *et seq.* FAIRCHILD admits that the First Amended Complaint purport to state a cause of action over which this Court has subject matter jurisdiction under 28 U.S.C. §§ 1331 and 1338(a).

4. In response to paragraph 4 of the First Amended Complaint, FAIRCHILD admits that this Court has personal jurisdiction over FAIRCHILD.

5. In response to paragraph 5 of the First Amended Complaint, FAIRCHILD admits, for the purpose of this action only, that venue is proper in this judicial district.

GENERAL ALLEGATIONS

6. In response to paragraph 6 of the First Amended Complaint, FAIRCHILD lacks sufficient knowledge or information to admit or deny the allegations set forth therein and therefore denies each and every allegation contained in paragraph 6.

7. In response to paragraph 7 of the First Amended Complaint, FAIRCHILD denies that it manufactures PWM integrated circuits devices in the United States. FAIRCHILD denies that it has been or currently is infringing, inducing infringement, or contributing to the infringement of the any PI patent asserted in the First Amended Complaint. FAIRCHILD admits that it imports a de minimis amount of PWM integrated circuits devices into the United States and that it sells and offers to sell a de minimis amount of PWM integrated circuits devices in the United States. FAIRCHILD denies any and all remaining allegations of paragraph 7 of the First Amended Complaint.

FIRST CAUSE OF ACTION

INFRINGEMENT OF U.S. PATENT NO. 6,107,851

8. In response to paragraph 8 of the First Amended Complaint, FAIRCHILD realleges its answers as set forth in paragraphs 1-7 above and incorporates by reference paragraphs 1 through 7, inclusive, as through fully set forth in this paragraph.

9. In response to paragraph 9 of the First Amended Complaint, FAIRCHILD admits that the title page of United States Patent No. 6,107,851 ("the '851 patent") states on its face that the patent was issued on August 22, 2000. FAIRCHILD admits that on its face the '851 patent is entitled "Offline Converter with Integrated Softstart and Frequency Jitter." FAIRCHILD admits that on its face the '851 patent lists "Power Integrations, Inc." as the assignee. FAIRCHILD admits that a copy of the '851 patent was attached to PI's original Complaint as Exhibit A. FAIRCHILD denies that the '851 patent is dully and legally issued. FAIRCHILD denies any and all remaining allegations of paragraph 9 of the First Amended Complaint.

10. In response to paragraph 10 of the First Amended Complaint, FAIRCHILD denies any and all allegations contained therein.

11. In response to paragraph 11 of the First Amended Complaint, FAIRCHILD denies any and all allegations contained therein.

12. In response to paragraph 12 of the First Amended Complaint, FAIRCHILD denies any and all allegations contained therein.

13. In response to paragraph 13 of the First Amended Complaint, FAIRCHILD denies any and all allegations contained therein.

SECOND CAUSE OF ACTION

INFRINGEMENT OF U.S. PATENT NO. 6,249,876

14. In response to paragraph 14 of the First Amended Complaint, FAIRCHILD realleges its answers as set forth in paragraphs 1-7 above and incorporates by reference paragraphs 1 through 7, inclusive, as through fully set forth in this paragraph.

15. In response to paragraph 15 of the First Amended Complaint, FAIRCHILD admits that the title page of United States Patent No. 6,249,876 ("the '876 patent") states on its face that the patent was issued on June 19, 2001. FAIRCHILD admits that on its face the '876 patent is entitled "Frequency Jittering Control for Varying the Switching Frequency of a Power Supply." FAIRCHILD admits that on its face the '876 patent lists "Power Integrations, Inc." as the assignee. FAIRCHILD admits that a copy of the '876 patent was attached to PI's original Complaint as Exhibit B. FAIRCHILD denies that the '876 patent is dully and legally issued. FAIRCHILD denies any and all remaining allegations of paragraph 15 of the First Amended Complaint.

16. In response to paragraph 16 of the First Amended Complaint, FAIRCHILD denies any and all allegations contained therein.

17. In response to paragraph 17 of the First Amended Complaint, FAIRCHILD denies any and all allegations contained therein.

18. In response to paragraph 18 of the First Amended Complaint, FAIRCHILD denies any and all allegations contained therein.

19. In response to paragraph 19 of the First Amended Complaint, FAIRCHILD denies any and all allegations contained therein.

THIRD CAUSE OF ACTION

INFRINGEMENT OF U.S. PATENT NO. 6,229,366

20. In response to paragraph 20 of the First Amended Complaint, FAIRCHILD realleges its answers as set forth in paragraphs 1-7 above and incorporates by reference paragraphs 1 through 7, inclusive, as through fully set forth in this paragraph.

21. In response to paragraph 21 of the First Amended Complaint, FAIRCHILD admits that the title page of United States Patent No. 6,229,366 ("the '366 patent") states on its face that the patent was issued on May 8, 2001. FAIRCHILD admits that on its face the '366 patent is entitled "Off-Line Converter with Integrated Softstart and Frequency Jitter." FAIRCHILD admits that on its face the '366 patent lists "Power Integrations, Inc." as the

assignee. FAIRCHILD admits that a copy of the '366 patent was attached to PI's original Complaint as Exhibit C. FAIRCHILD denies that the '366 patent is dully and legally issued. FAIRCHILD denies any and all remaining allegations of paragraph 21 of the First Amended Complaint.

22. In response to paragraph 22 of the First Amended Complaint, FAIRCHILD denies any and all allegations contained therein.

23. In response to paragraph 23 of the First Amended Complaint, FAIRCHILD denies any and all allegations contained therein.

24. In response to paragraph 24 of the First Amended Complaint, FAIRCHILD denies any and all allegations contained therein.

25. In response to paragraph 25 of the First Amended Complaint, FAIRCHILD denies any and all allegations contained therein.

FOURTH CAUSE OF ACTION

INFRINGEMENT OF U.S. PATENT NO. 4,811,075

26. In response to paragraph 26 of the First Amended Complaint, FAIRCHILD realleges its answers as set forth in paragraphs 1-7 above and incorporates by reference paragraphs 1 through 7, inclusive, as through fully set forth in this paragraph.

27. In response to paragraph 27 of the First Amended Complaint, FAIRCHILD admits that the title page of United States Patent No. 4,811,075 ("the '075 patent") states on its face that the patent was issued on March 7, 1989. FAIRCHILD admits that on its face the '075 patent is entitled "High Voltage MOS Transistors." FAIRCHILD admits that on its face the '075 patent lists "Power Integrations, Inc." as the assignee. FAIRCHILD admits that a copy of the '075 patent was attached to PI's original Complaint as Exhibit D. FAIRCHILD denies that the '075 patent is dully and legally issued. FAIRCHILD denies any and all remaining allegations of paragraph 27 of the First Amended Complaint.

28. In response to paragraph 28 of the First Amended Complaint, FAIRCHILD denies any and all allegations contained therein.

29. In response to paragraph 29 of the First Amended Complaint, FAIRCHILD denies any and all allegations contained therein.

30. In response to paragraph 30 of the First Amended Complaint, FAIRCHILD denies any and all allegations contained therein.

31. In response to paragraph 31 of the First Amended Complaint, FAIRCHILD denies any and all allegations contained therein.

AFFIRMATIVE AND OTHER DEFENSES

Further Answering the First Amended Complaint, FAIRCHILD asserts the following defenses. FAIRCHILD reserves the right to amend its answer with additional defenses as further information is obtained.

First Defense: Noninfringement of the Asserted Patents

32. FAIRCHILD has not infringed, contributed to infringement of, or induced the infringement of any valid claim of the '851 Patent, the '876 Patent, the '366 Patent, or the '075 Patent, and is not liable for infringement thereof.

33. No product made by FAIRCHILD or process used by FAIRCHILD infringes the '851 Patent, the '876 Patent, the '366 Patent, or the '075 Patent because PI's First Amended Complaint fails to state a claim that meets the requirements of 35 U.S.C. § 271.

Second Defense: Invalidity of the Asserted Patents

34. The '851 Patent, the '876 Patent, the '366 Patent, and the '075 Patent are invalid for failing to comply with the provisions of the Patent Laws, Title 35 U.S.C., including without limitation 35 U.S.C §§ 102, 103, 112, and 121.

Third Defense: Unavailability of Relief

35. PI has failed to plead and meet the requirements of 35 U.S.C. § 271(b) and (c) and is not entitled to any alleged damages from FAIRCHILD.

Fourth Defense: Unavailability of Relief (Marking and Notice)

36. PI has failed to plead and meet the requirements of 35 U.S.C. § 287 on marking and notice, and has otherwise failed to show that it is entitled to any damages prior to the filing date of the First Amended Complaint.

Fifth Defense: Limitation on Damages (Past Damages)

37. PI's claim for relief and prayer for damages are limited by 35 U.S.C. § 286.

Sixth Defense: Limitation on Damages (Increased Damages and Attorney Fees)

38. PI has failed to plead and meet the requirements of 35 U.S.C. § 284 and 285 for increased damages and attorney fees and is not entitled to any such increased damages or attorney fees.

Seventh Defense: Estoppel

39. PI is estopped from alleging that the '851 Patent, the '876 Patent, the '366 Patent, and/or the '075 Patent cover or include any accused product or activity by FAIRCHILD based on arguments made by PI during prosecution of the '851 Patent, the '876 Patent, the '366 Patent, and/or the '075 Patent.

Eighth Defense: Laches

40. On information and belief, PI's claims for relief are barred, in whole or in part, by the equitable doctrine of laches.

Ninth Defense: Waiver

41. On information and belief, PI's claims for relief are barred or unenforceable, in whole or in part, due to waiver.

Tenth Defense: Unenforceability

42. On information and belief, PI's claims for relief are unenforceable, in whole or in part, due to unclean hands.

Eleventh Defense: Unenforceability

43. On information and belief, PI's claims for relief are unenforceable, in whole or in part, due to inequitable conduct. FAIRCHILD incorporates by reference Paragraphs 24-89 of its COUNTERCLAIMS, as if fully restated herein.

COUNTERCLAIMS

First Counterclaim: Declaratory Judgment of Non-Infringement

1. This action arises under the patent laws of the United States, Title 35 U.S.C. §§ 1, *et seq.* This Court has subject matter jurisdiction over this counterclaim under 28 U.S.C. §§ 1331, 1338(a), 2201, and 2202.

2. Fairchild Semiconductor International, Inc. is a Delaware corporation with its principal place of business in South Portland, Maine. Fairchild Semiconductor Corporation is a Delaware corporation with its principal place of business in South Portland, Maine. (Fairchild Semiconductor International, Inc. and Fairchild Semiconductor Corporation are collectively referred to as "FAIRCHILD.")

3. On information and belief, Plaintiff/Counterclaim Defendant Power Integrations, Inc. ("PI") is a Delaware corporation with its principal place of business in San Jose, California.

4. Venue is proper in the District of Delaware pursuant to 28 U.S.C. §§ 1391(b)-(c) and 1400.

5. PI purports to be the owner of U.S. Patent Nos. 6,107,851 ("the '851 Patent"), 6,249,876 ("the '876 Patent"), 6,229,366 ("the '366 Patent"), and 4,811,075 ("the '075 Patent").

6. PI alleges that FAIRCHILD has infringed the '851 Patent, the '876 Patent, the '366 Patent, and the '075 Patent.

7. No product made by FAIRCHILD or process used by FAIRCHILD has infringed, either directly or indirectly, any claim of the '851 Patent, the '876 Patent, the '366 Patent, or the '075 Patent, and FAIRCHILD is not liable for infringement thereof.

8. No activity by FAIRCHILD comes within the requirements of 35 U.S.C. § 271 with respect to the '851 Patent, the '876 Patent, the '366 Patent, or the '075 Patent, and

FAIRCHILD is not liable for infringement of the '851 Patent, the '876 Patent, the '366 Patent, or the '075 Patent under 35 U.S.C. § 271.

9. FAIRCHILD's activities that are outside of the United States do not come within the requirements of 35 U.S.C. § 271 with respect to the '851 Patent, the '876 Patent, the '366 Patent, or the '075 Patent, and do not constitute infringement.

10. An actual controversy, within the meaning of 28 U.S.C. §§ 2201 and 2202, exists between FAIRCHILD, on the one hand, and PI, on the other hand, with respect to the infringement or noninfringement of the '851 Patent, the '876 Patent, the '366 Patent, and/or the '075 Patent.

Second Counterclaim: Declaratory Judgment of Invalidity of the '851 Patent

11. FAIRCHILD repeats and realleges paragraphs 1-10 of its Counterclaims, as if fully restated herein.

12. The '851 Patent, and each claim thereof, is invalid for failing to comply with the provisions of the Patent Laws, including one or more of 35 U.S.C. §§ 102, 103, 112, and 121.

13. An actual controversy, within the meaning of 28 U.S.C. §§ 2201 and 2202, exists between FAIRCHILD, on the one hand, and PI, on the other hand, with respect to whether the claims of the '851 Patent are valid or invalid.

Third Counterclaim: Declaratory Judgment of Invalidity of the '876 Patent

14. FAIRCHILD repeats and realleges paragraphs 1-10 of its Counterclaims, as if fully restated herein.

15. The '876 Patent, and each claim thereof, is invalid for failing to comply with the provisions of the Patent Laws, including one or more of 35 U.S.C. §§ 102, 103, 112, and 121.

16. An actual controversy, within the meaning of 28 U.S.C. §§ 2201 and 2202, exists between FAIRCHILD, on the one hand, and PI, on the other hand, with respect to whether the claims of the '876 Patent are valid or invalid.

Fourth Counterclaim: Declaratory Judgment of Invalidity of the '366 Patent

17. FAIRCHILD repeats and realleges paragraphs 1-10 of its Counterclaims, as if fully restated herein.

18. The '366 Patent, and each claim thereof, is invalid for failing to comply with the provisions of the Patent Laws, including one or more of 35 U.S.C. §§ 102, 103, 112, and 121.

19. An actual controversy, within the meaning of 28 U.S.C. §§ 2201 and 2202, exists between FAIRCHILD, on the one hand, and PI, on the other hand, with respect to whether the claims of the '366 Patent are valid or invalid.

Fifth Counterclaim: Declaratory Judgment of Invalidity of the '075 Patent

20. FAIRCHILD repeats and realleges paragraphs 1-10 of its Counterclaims, as if fully restated herein.

21. The '075 Patent, and each claim thereof, is invalid for failing to comply with the provisions of the Patent Laws, including one or more of 35 U.S.C. §§ 102, 103, 112, and 121.

22. An actual controversy, within the meaning of 28 U.S.C. §§ 2201 and 2202, exists between FAIRCHILD, on the one hand, and PI, on the other hand, with respect to whether the claims of the '075 Patent are valid or invalid.

Sixth Counterclaim: Declaratory Judgment of Unenforceability the '366 Patent

23. FAIRCHILD repeats and realleges paragraphs 1-10 of its Counterclaims, as if fully restated herein.

24. The '366 Patent, and each claim thereof, is unenforceable due to inequitable conduct during the prosecution of the '366 Patent.

25. During prosecution of the '366 Patent, Power Integrations failed to disclose to the United States Patent and Trademark Office ("PTO") prior art that was highly material to the patentability of the claims of the '366 patent under prosecution, and that Power Integrations knew or should have known would have been important to a reasonable examiner. The undisclosed prior art references include at least devices that anticipate or render obvious claims

of the '366 Patent, that were designed, manufactured, offered for sale and sold by Power Integrations more than a year before the application leading to the '366 Patent was filed.

26. An actual controversy, within the meaning of 28 U.S.C. §§ 2201 and 2202, exists between FAIRCHILD, on the one hand, and PI, on the other hand, with respect to whether the claims of the '366 Patent are enforceable or unenforceable.

**Power Integrations' TOP100-4 TopSwitch Datasheets and
Family of Devices**

27. Power Integrations' TOP100-4 TopSwitch family of devices was and is highly material prior art to the patentability of the claims of the '366 patent, would have been important to a reasonable examiner, would have established at least a case of prima facie obviousness of the claims Power Integrations prosecuted in the application for the '366 Patent and anticipates claims of the '366 Patent. These devices were offered for sale and sold by Power Integrations at least as early as May 18, 1997. Power Integrations published in the United States datasheets describing its TOP100-4 TopSwitch family of devices at least as early as July 1996. A copy of such a datasheet is attached hereto as Exhibit A. This is more than a year before Power Integrations filed the application leading to the '366 Patent and thus the TOP100-4 TopSwitch family of devices and the Power Integrations datasheets describing those products are prior art to the '366 Patent.

28. The TOP100-4 TopSwitch family of devices and the datasheets describing those devices were and are highly material to the patentability of the '366 Patent because they teach every element of claims of the '366 Patent. The materiality of this prior art is demonstrated by the fact that Figure 1 from the Power Integrations TOP100-4 TopSwitch datasheet (described in that datasheet as a "typical application") is identical to Figure 2 of the '366 Patent, which the Applicants describe as their "invention" (except that the reference to the prior art TOP100-4 device is replaced with a black box PWM controller). *See*, '366 Patent, col. 4, lines 50-52 ("Fig. 2 is a presently preferred power supply utilizing an [sic] pulse width modulated switch according to the present invention."; *see also*, '366 Patent, col. 5, lines 3-column 6, line 34 (describing

Figure 2, identical to Figure 1 from the prior art TOP100-4 datasheet, as the “preferred embodiment”).

29. Neither Power Integrations, nor its attorneys, nor the Applicants for the ‘366 Patent disclosed to the Patent Office either Power Integrations’ TOP100-4 TopSwitch family of devices or the Power Integrations datasheets describing those devices during the prosecution of the ‘366 Patent. On information and belief, as employees of Power Integrations working on the design and development of Power Integrations’ devices, the Applicants were aware of Power Integrations’ TOP100-4 TopSwitch family of devices and the Power Integrations datasheets describing those devices, knew or should have known of the materiality of those devices and data sheets to the patentability of the pending claims that issued in the ‘366 patent and intentionally or in bad faith withheld this highly material prior art. This constitutes inequitable conduct that renders all claims of the ‘366 patent permanently unenforceable.

Power Integrations’ TOP200-4/14 TopSwitch Datasheets and Family of Devices

30. Power Integrations sold additional devices that anticipate the claims of the ‘366 Patent more than a year before the application leading to that patent was filed. For instance, Power Integrations published the TOP200-4/14 datasheet at least as early as November, 1994, a copy of which is attached hereto as Exhibit B. On information and belief, Power Integrations offered for sale and sold its TOP200-4/14 family of devices more than a year before the application leading to the ‘366 patent was filed.

31. As with the TOP100-4, the TOP200-4/14 (and datasheets describing these devices) were and are highly material to the patentability of the claims of the ‘366 patent, would have been important to a reasonable examiner, would have established at least a case of prima facie obviousness of the claims Power Integrations prosecuted in the application for the ‘366 Patent and anticipate claims of that patent. The materiality of this prior art is demonstrated by the fact that Figure 1 from the Power Integrations TOP200-4/14 TopSwitch datasheet (described in that datasheet as a “typical application”) is identical to Figure 2 of the ‘366 Patent, which the

Applicants describe as their “invention” (except that the reference to the prior art TOP100-4 device is replaced with a black box PWM controller). *See*, ‘366 Patent, col. 4, lines 50-52 (“Fig. 2 is a presently preferred power supply utilizing an [sic] pulse width modulated switch according to the present invention.”); *see also*, ‘366 Patent, col. 5, lines 3-column 6, line 34 (describing Figure 2, identical to figure 1 of the prior art TOP100-4 datasheet, as the “preferred embodiment”).

32. Neither Power Integrations, nor its attorneys, nor the Applicants for the ‘366 Patent disclosed to the Patent Office either Power Integrations’ TOP200-4/14 TopSwitch family of devices or the Power Integrations datasheets describing those devices during the prosecution of the ‘366 Patent. On information and belief, as employees of Power Integrations working on the design and development of Power Integrations’ devices, the Applicants were aware of Power Integrations’ TOP200-4/14 TopSwitch family of devices and the Power Integrations datasheets describing those devices, knew or should have known of the materiality of those devices and data sheets to the patentability of the pending claims that issued in the ‘366 patent and intentionally or in bad faith withheld this highly material prior art. This constitutes inequitable conduct that renders all claims of the ‘366 patent permanently unenforceable.

**Power Integrations’ TOP221-227 TopSwitch Datasheets and
Family of Devices**

33. On information and belief, Power Integrations also offered for sale and sold the TOP221-227 TopSwitch-II family of devices prior to the filing of the application that led to the ‘366 Patent. Further, Power Integrations published in the United States datasheets describing the TOP221-227 TopSwitch-II family of devices at least as early as December, 1997, a copy of which is attached hereto as Exhibit C.

34. As described in the December 1997 datasheet, the prior art TOP221-227 TopSwitch-II family of devices anticipates claims of the ‘366 Patent. Thus, the TOP221-227 TopSwitch-II family of devices – and datasheets describing those devices – were and are highly material to the patentability of the ‘366 Patent, would have been important to a reasonable

examiner and would have established at least a case of prima facie obviousness of the claims Power Integrations prosecuted in the '366 Patent.

35. As with the TOP100-4 and TOP200-4/14 datasheets, Figure 1 from the TOP221-227 datasheet (described as a "typical flyback application") is identical to Figure 2 of the '366 Patent, which the Applicants describe as their "invention" (except that the reference to the prior art TOP100-4 device is replaced with a black box PWM controller). *See*, '366 Patent, col. 4, lines 50-52 ("Fig. 2 is a presently preferred power supply utilizing an [sic] pulse width modulated switch according to the present invention."; *see also*, '366 Patent, col. 5, lines 3-column 6, line 34 (describing Figure 2, identical to Figure 1 of the prior art TOP100-4 datasheet, as the "preferred embodiment").

36. Neither Power Integrations, nor its attorneys, nor the Applicants for the '366 Patent disclosed to the Patent Office either Power Integrations' TOP221-227 TopSwitch-II family of devices or the Power Integrations datasheets describing those devices during the prosecution of the '366 Patent. On information and belief, as employees of Power Integrations working on the design and development of Power Integrations' devices, the Applicants were aware of Power Integrations' TOP221-227 TopSwitch-II family of devices and the Power Integrations datasheets describing those devices, knew or should have known of the materiality of those devices and data sheets to the patentability of the pending claims that issued in the '366 patent and intentionally or in bad faith withheld this highly material prior art. This constitutes inequitable conduct that renders all claims of the '366 patent permanently unenforceable.

Power Integrations' SMP260 Family of Devices and "Off-line Power Integrated Circuit for International Rated 60-watt Power Supplies" article.

37. Power Integrations also offered for sale and sold the PWR-SMP260 family of devices prior to the filing of the application that led to the '366 Patent. On information and belief, these products were also described in datasheets published by Power Integrations in the United States more than a year before Power Integrations filed the application leading to the '366 Patent. A copy of the SMP260 datasheet is attached as Exhibit D.

38. Power Integrations' PWR-SMP260 devices were also described in an article by Richard A. Keller entitled "Off-line Power Integrated Circuit for International Rated 60-watt Power Supplies", published in 1992, ("Keller Article"), a copy of which is attached as Exhibit F. Upon information and belief, at the time of the article Richard A. Keller was employed by Power Integrations.

39. Both the PWR-SMP260 devices and the Keller article were and are highly material prior art to the patentability of the claims of the '366 patent, would have been important to a reasonable examiner, would have established at least a case of prima facie obviousness of the claims Power Integrations prosecuted in the application for the '366 Patent and anticipate claims of the '366 Patent.

40. Neither Power Integrations, nor its attorneys, nor the Applicants for the '366 Patent disclosed either the PWR-SMP260 devices or the Keller Article to the Patent Office during the prosecution of the '366 Patent.

41. On information and belief, as employees of Power Integrations working on the design and development of Power Integrations' devices, the Applicants were aware of Power Integrations' PWR-SMP260 devices and the Keller Article, knew or should have known of the materiality of those devices and the Keller Article to the patentability of the pending claims that issued in the '366 patent and intentionally or in bad faith withheld this highly material prior art. This constitutes inequitable conduct that renders all claims of the '366 patent permanently unenforceable.

Power Integrations' SMP240 Family of Devices

42. Power Integrations also offered for sale and sold the PWR-SMP240 family of devices prior to the filing of the application that led to the '366 Patent. On information and belief, these products were also described in datasheets published by Power Integrations in the United States more than a year before Power Integrations filed the application leading to the '366 Patent. A copy of the SMP240 datasheet is attached as Exhibit E.

43. The PWR-SMP240 devices was and is highly material prior art to the patentability of the claims of the '366 patent, would have been important to a reasonable examiner, would have established at least a case of prima facie obviousness of the claims Power Integrations prosecuted in the application for the '366 Patent and anticipate claims of the '366 Patent.

44. Neither Power Integrations, nor its attorneys, nor the Applicants for the '366 Patent disclosed the PWR-SMP240 devices to the Patent Office during the prosecution of the '366 Patent.

45. On information and belief, as employees of Power Integrations working on the design and development of Power Integrations' devices, the Applicants were aware of Power Integrations' PWR-SMP240 devices, knew or should have known of the materiality of those devices to the patentability of the pending claims that issued in the '366 patent and intentionally or in bad faith withheld this highly material prior art. This constitutes inequitable conduct that renders all claims of the '366 patent permanently unenforceable.

Power Integrations' SMP211 Datasheets and Family of Devices

46. Power Integrations' SMP211 family of devices was and is highly material prior art to the patentability of the claims of the '366 Patent, would have been important to a reasonable examiner, would have established at least a case of prima facie obviousness of the claims Power Integrations prosecuted in the application for the '366 Patent and anticipates claims of the '366 Patent. These devices were offered for sale and sold by Power Integrations at least as early as May 18, 1997. Power Integrations published in the United States datasheets describing its SMP211 family of devices at least as early as 1996. A copy of such a datasheet is attached hereto as Exhibit G. This is more than a year before Power Integrations filed the application leading to the '366 Patent and thus the SMP211 family of devices and the Power Integrations datasheets describing those products are prior art to the '366 Patent.

47. The SMP211 family of devices and the datasheets describing those devices were and are highly material to the patentability of the '366 Patent because they teach every element

of claims of the '366 Patent. Figure 1 of the '366 Patent was described by the Applicants as the "Prior Art". This prior art figure includes a devices labeled "SMP211", which was a prior art Power Integrations device. The Applicants, however, withheld all information about their own SMP211 device from the Patent Examiner.

48. On December 13, 1999, during the prosecution of Application No. 09/080,774, the application that ultimately led to the issuance of the '366 Patent, the Examiner rejected pending claims as anticipated by Prior Art Figure 1:

Claims 29, 35 & 37 are rejected under 35 U.S.C. 102(b) as being anticipated by Applicants' Prior Art Fig. 1.

Applicants' Prior Art Fig. 1 shows a first terminal 95, a second terminal Com, a switch/drive circuit 90 and a frequency variation circuit 140 as recited in claim 29.

Further shown is a rectifier 10, a capacitor 15, a first winding 35 and a second winding 45 as recited in claim 35.

Further shown is a feedback terminal (Error Amplifier in) as recited in claim 37.

The Examiner, however, allowed other claims because of his belief that the prior art did not include an oscillator that generated a maximum duty cycle signal and a signal with a frequency range depending on the frequency variation circuit:

Allowable Subject Matter

The prior Art of record does not appear to disclose or suggest a PWM switch comprising an oscillator for generating a maximum duty cycle signal and a singnal [sic] with a frequency range dependant on a frequency variation circuit as recited in claim 1.

49. However, unknown to the Examiner, the SMP211 device referred to in Figure 1 of the '366 Patent actually included "an oscillator for generating a maximum duty cycle signal and a singnal [sic] with a frequency range dependant on a frequency variation circuit". See Exh. G, Figure 3 and 2-48 – 2-49. Thus, the SMP211 is highly relevant and material to the patentability of the '366 Patent. The Applicants, however, continued to withhold information concerning the SMP211 from the Examiner.

50. Rather than disclose the SMP211, the Applicants amended the rejected claims to include the oscillator limitation that the Examiner erroneously believed to be missing from the prior art of record:

In the December 13, 1999 Office Action, claims 29, 35 and 37 are rejected under 35 U.S.C. § 102(b) as being anticipated by Applicants' Prior Art Figure 1.

Claim 29 as presently amended now expressly recites a regulation circuit that includes an oscillator that provides a maximum duty cycle signal and an oscillation signal having a frequency range that is varied according to a frequency variation signal. The Applicants' Prior Art Figure 1 fails to disclose, teach or suggest such limitations. Accordingly, the Applicants respectfully submit that the instant section 102 rejection has been overcome.

51. Applicants' prior art SMP211 device – and datasheets describing the SMP211 device – clearly disclose “a regulation circuit that includes an oscillator that provides a maximum duty cycle signal and an oscillation signal having a frequency range that is varied according to a frequency variation signal.” *See* Exh. G at Figure 3 and 2-48 – 2-49. Despite this, Applicants continued to withhold any information about their SMP211 devices. While withholding this information, the Applicants argued that the Examiner should allow the amended claims because Applicants had added limitations concerning the maximum duty cycle signal limitation, which they claimed was not present in the prior art of record (even though these limitations are present in the SMP211 devices and datasheets). Thereafter, the Examiner allowed the amended claims based upon the Applicants' false representations regarding the absence of a maximum duty cycle signal from the prior art.

52. Neither Power Integrations, nor its attorneys, nor the Applicants for the '366 Patent disclosed to the Patent Office either Power Integrations' SMP211 family of devices or the Power Integrations datasheets describing those devices during the prosecution of the '366 Patent. On information and belief, as employees of Power Integrations working on the design and development of Power Integrations' devices, the Applicants were aware of Power Integrations' SMP211 family of devices and the Power Integrations datasheets describing those devices, knew or should have known of the materiality of those devices and data sheets to the patentability of the pending claims that issued in the '366 patent and intentionally or in bad faith withheld this

highly material prior art. This constitutes inequitable conduct that renders all claims of the '366 patent permanently unenforceable.

**Power Integrations' SMP3 Family of Devices, Datasheets, and
"Off-Line PWM Switching Regulator IC Handles 3W" Article**

53. In addition, Power Integrations' SMP3 family of devices was and is highly material prior art to the patentability of the claims of the '366 patent, would have been important to a reasonable examiner, would have established at least a case of prima facie obviousness of the claims Power Integrations prosecuted in the application for the '366 Patent and anticipates claims of the '366 Patent. On information and belief, these devices were offered for sale and sold by Power Integrations at least as early as May 18, 1997. These devices are described in an article entitled "Off-Line PWM Switching Regulator IC Handles 3W" by F. Goodenough, published on March 22, 1990 in *Electronic Design* (pp. 35-39) ("Goodenough Article"). A copy of the Goodenough Article is attached hereto as Exhibit I.

54. On information and belief, F. Goodenough was employed by Power Integrations when he wrote and published the Goodenough Article.

55. The prior art SMP3 devices and the Goodenough Article were and are highly material to the patentability of the '851 Patent as both the devices and the Article anticipate claims of that Patent.

56. Despite the highly material nature of the Power Integrations SMP3 devices and the Goodenough Article, neither Power Integrations, nor its attorneys, nor the Applicants for the '851 Patent disclosed either the Power Integrations SMP3 devices or the Goodenough Article to the Patent Office during the prosecution of the '851 Patent. On information and belief, as employees of Power Integrations working on the design and development of Power Integrations' devices, the Applicants were aware of Power Integrations' SMP3 family of devices and the Goodenough Article describing those devices, knew or should have known of the materiality of those devices and Article to the patentability of the pending claims that issued in the '851 Patent,

and intentionally or in bad faith withheld this highly material prior art. This constitutes inequitable conduct that renders all claims of the '851 patent permanently unenforceable.

Seventh Counterclaim: Declaratory Judgment of Unenforceability the '851 Patent

57. FAIRCHILD repeats and realleges paragraphs 1-10 of its Counterclaims, as if fully restated herein.

58. The '851 Patent, and each claim thereof, is unenforceable due to the inequitable conduct during the prosecution of the '851 Patent.

59. During the prosecution of the '851 Patent, Power Integrations failed to disclose to the United States Patent and Trademark Office prior art that was highly material to the patentability of the claims of the '851 Patent, and that Power Integrations knew or should have known would have been important to a reasonable examiner. The undisclosed prior art references include at least devices that anticipate or render obvious claims of the '851 Patent, that were designed, manufactured, offered for sale and sold by Power Integrations more than a year before the application leading to the '851 Patent was filed.

60. An actual controversy, within the meaning of 28 U.S.C. §§ 2201 and 2202, exists between FAIRCHILD, on the one hand, and PI, on the other hand, with respect to whether the claims of the '851 Patent are enforceable or unenforceable.

Power Integrations' SMP402 Datasheets and Family of Devices

61. Power Integrations' SMP402 family of devices was and is highly material prior art to the patentability of the claims of the '851 patent, would have been important to a reasonable examiner, would have established at least a case of prima facie obviousness of the claims Power Integrations prosecuted in the application for the '851 Patent and anticipates claims of the '851 Patent. On information and belief, these devices were offered for sale and sold by Power Integrations at least as early as May 18, 1997. Power Integrations published datasheets in the United States describing its SMP402 family of devices at least as early as January, 1996. A copy of such a datasheet is attached hereto as Exhibit H. This is more than a year before Power Integrations filed the application leading to the '851 Patent and thus the

SMP402 family of devices and the Power Integrations datasheets describing those products are prior art to the '851 Patent.

62. The SMP402 family of devices and the datasheets describing those devices were and are highly material to the patentability of the '851 Patent because they teach every element of claims of the '851 Patent.

63. Power Integrations failed to disclose to the Patent Office either Power Integrations' SMP402 family of devices or the Power Integrations datasheets describing those devices during the prosecution of the '851 Patent. On information and belief, as employees of Power Integrations working on the design and development of Power Integrations' devices, the Applicants were aware of Power Integrations' SMP402 family of devices and the Power Integrations datasheets describing those devices, knew or should have known of the materiality of those devices and data sheets to the patentability of the pending claims that issued in the '851 Patent, and intentionally or in bad faith withheld this highly material prior art. This constitutes inequitable conduct that renders all claims of the '851 patent permanently unenforceable.

**Power Integrations' SMP3 Family of Devices, Datasheets, and
"Off-Line PWM Switching Regulator IC Handles 3W" Article**

64. In addition, Power Integrations' SMP3 family of devices was and is highly material prior art to the patentability of the claims of the '851 patent, would have been important to a reasonable examiner, would have established at least a case of prima facie obviousness of the claims Power Integrations prosecuted in the application for the '851 Patent and anticipates claims of the '851 Patent. On information and belief, these devices were offered for sale and sold by Power Integrations at least as early as May 18, 1997. These devices are described in an article entitled "Off-Line PWM Switching Regulator IC Handles 3W" by F. Goodenough, published on March 22, 1990 in *Electronic Design* (pp. 35-39) ("Goodenough Article"). A copy of the Goodenough Article is attached hereto as Exhibit I.

65. On information and belief, F. Goodenough was employed by Power Integrations when he wrote and published the Goodenough Article.

66. The prior art SMP3 devices and the Goodenough Article were and are highly material to the patentability of the '851 Patent as both the devices and the Article anticipate claims of that Patent.

67. Despite the highly material nature of the Power Integrations SMP3 devices and the Goodenough Article, neither Power Integrations, nor its attorneys, nor the Applicants for the '851 Patent disclosed either the Power Integrations SMP3 devices or the Goodenough Article to the Patent Office during the prosecution of the '851 Patent. On information and belief, as employees of Power Integrations working on the design and development of Power Integrations' devices, the Applicants were aware of Power Integrations' SMP3 family of devices and the Goodenough Article describing those devices, knew or should have known of the materiality of those devices and Article to the patentability of the pending claims that issued in the '851 Patent, and intentionally or in bad faith withheld this highly material prior art. This constitutes inequitable conduct that renders all claims of the '851 patent permanently unenforceable.

**Power Integrations' SMP260 Datasheets, Family of Devices, and
"Off-line Power Integrated Circuit for International Rated 60-watt
Power Supplies" Article**

68. Power Integrations also offered for sale and sold the PWR-SMP260 family of devices prior to the filing of the application that led to the '851 Patent. On information and belief, these products were also described in datasheets published by Power Integrations in the United States more than a year before Power Integrations filed the application leading to the '851 Patent. A copy of the SMP260 datasheet is attached as Exhibit D.

69. Power Integrations' PWR-SMP260 devices were also described in an article by Richard A. Keller entitled "Off-line Power Integrated Circuit for International Rated 60-watt Power Supplies", published in 1992, ("Keller Article"), a copy of which is attached as Exhibit F. Upon information and belief, at the time of the article Richard A. Keller was employed by Power Integrations.

70. The PWR-SMP260 devices and the Keller article were and are both material to the patentability of the '851 Patent as both anticipate claims of that patent.

71. Neither Power Integrations, nor its attorneys, nor the Applicants for the '851 Patent disclosed either the PWR-SMP260 devices or the Keller Article to the Patent Office during the prosecution of the '851 Patent.

72. On information and belief, as employees of Power Integrations working on the design and development of Power Integrations' devices, the Applicants were aware of Power Integrations' PWR-SMP260 devices and the Keller Article, knew or should have known of the materiality of those devices and Article to the patentability of the pending claims that issued in the '851 Patent, and intentionally or in bad faith withheld this highly material prior art. This constitutes inequitable conduct that renders all claims of the '851 patent permanently unenforceable.

Power Integrations' SMP240 Family of Devices

73. Power Integrations also offered for sale and sold the PWR-SMP240 family of devices prior to the filing of the application that led to the '851 Patent. On information and belief, these products were also described in datasheets published by Power Integrations in the United States more than a year before Power Integrations filed the application leading to the '851 Patent. A copy of the SMP240 datasheet is attached as Exhibit E.

74. The PWR-SMP240 devices was and is highly material prior art to the patentability of the claims of the '851 patent, would have been important to a reasonable examiner, would have established at least a case of prima facie obviousness of the claims Power Integrations prosecuted in the application for the '851 Patent and anticipate claims of the '851 Patent.

75. Neither Power Integrations, nor its attorneys, nor the Applicants for the '851 Patent disclosed the PWR-SMP240 devices to the Patent Office during the prosecution of the '851 Patent.

76. On information and belief, as employees of Power Integrations working on the design and development of Power Integrations' devices, the Applicants were aware of Power Integrations' PWR-SMP240 devices, knew or should have known of the materiality of those

devices to the patentability of the pending claims that issued in the '851 patent and intentionally or in bad faith withheld this highly material prior art. This constitutes inequitable conduct that renders all claims of the '851 patent permanently unenforceable.

Power Integrations' SMP211 Datasheets and Family of Devices

77. Power Integrations' SMP211 family of devices was and is highly material prior art to the patentability of the claims of the '851 Patent, would have been important to a reasonable examiner, would have established at least a case of prima facie obviousness of the claims Power Integrations prosecuted in the application for the '851 Patent and anticipates claims of the '851 Patent. These devices were offered for sale and sold by Power Integrations at least as early as May 18, 1997. Power Integrations published in the United States datasheets describing its SMP211 family of devices at least as early as 1996. A copy of such a datasheet is attached hereto as Exhibit G. This is more than a year before Power Integrations filed the application leading to the '851 Patent and thus the SMP211 family of devices and the Power Integrations datasheets describing those products are prior art to the '851 Patent.

78. The SMP211 family of devices and the datasheets describing those devices were and are highly material to the patentability of the '851 Patent because they teach every element of claims of the '851 Patent. Figure 1 of the '851 Patent was described by the Applicants as the "Prior Art". This prior art figure includes a devices labeled "SMP211", which was a prior art Power Integrations device. The Applicants, however, withheld all information about their own SMP211 device from the Patent Examiner.

79. On December 13, 1999, during the prosecution of the '851 Patent, the Examiner rejected pending claims as anticipated by Prior Art Figure 1:

Claims 29, 35 & 37 are rejected under 35 U.S.C. 102(b) as being anticipated by Applicants' Prior Art Fig. 1.

Applicants' Prior Art Fig. 1 shows a first terminal 95, a second terminal Com, a switch/drive circuit 90 and a frequency variation circuit 140 as recited in claim 29.

Further shown is a rectifier 10, a capacitor 15, a first winding 35 and a second winding 45 as recited in claim 35.

Further shown is a feedback terminal (Error Amplifier in) as recited in claim 37. The Examiner, however, allowed other claims because of his belief that the prior art did not include an oscillator that generated a maximum duty cycle signal and a signal with a frequency range depending on the frequency variation circuit:

Allowable Subject Matter

The prior Art of record does not appear to disclose or suggest a PWM switch comprising an oscillator for generating a maximum duty cycle signal and a singnal [sic] with a frequency range dependant on a frequency variation circuit as recited in claim 1.

80. However, unknown to the Examiner, the SMP211 device referred to in Figure 1 of the '851 Patent actually included "an oscillator for generating a maximum duty cycle signal and a singnal [sic] with a frequency range dependant on a frequency variation circuit". See Exh. G, Figure 3 and 2-48 – 2-49. Thus, the SMP211 is highly relevant and material to the patentability of the '851 Patent. The Applicants, however, continued to withhold information concerning the SMP211 from the Examiner.

81. Rather than disclose the SMP211, the Applicants amended the rejected claims to include the oscillator limitation that the Examiner erroneously believed to be missing from the prior art of record:

In the December 13, 1999 Office Action, claims 29, 35 and 37 are rejected under 35 U.S.C. § 102(b) as being anticipated by Applicants' Prior Art Figure 1.

Claim 29 as presently amended now expressly recites a regulation circuit that includes an oscillator that provides a maximum duty cycle signal and an oscillation signal having a frequency range that is varied according to a frequency variation signal. The Applicants' Prior Art Figure 1 fails to disclose, teach or suggest such limitations. Accordingly, the Applicants respectfully submit that the instant section 102 rejection has been overcome.

82. Applicants' prior art SMP211 device – and datasheets describing the SMP211 device – clearly disclose "a regulation circuit that includes an oscillator that provides a maximum duty cycle signal and an oscillation signal having a frequency range that is varied according to a frequency variation signal." See Exh. G at Figure 3 and 2-48 – 2-49. Despite this, Applicants continued to withhold any information about their SMP211 devices. While withholding this information, the Applicants argued that the Examiner should allow the amended claims because

Applicants had added limitations concerning the maximum duty cycle signal limitation, which they claimed was not present in the prior art of record (even though these limitations are present in the SMP211 devices and datasheets). Thereafter, the Examiner allowed the amended claims based upon the Applicants' false representations regarding the absence of a maximum duty cycle signal from the prior art.

83. Neither Power Integrations, nor its attorneys, nor the Applicants for the '851 Patent disclosed to the Patent Office either Power Integrations' SMP211 family of devices or the Power Integrations datasheets describing those devices during the prosecution of the '851 Patent. On information and belief, as employees of Power Integrations working on the design and development of Power Integrations' devices, the Applicants were aware of Power Integrations' SMP211 family of devices and the Power Integrations datasheets describing those devices, knew or should have known of the materiality of those devices and data sheets to the patentability of the pending claims that issued in the '851 patent and intentionally or in bad faith withheld this highly material prior art. This constitutes inequitable conduct that renders all claims of the '851 patent permanently unenforceable.

Seventh Counterclaim: Declaratory Judgment of Unenforceability the '876 Patent

84. FAIRCHILD repeats and realleges paragraphs 1-10 of its Counterclaims, as if fully restated herein.

85. The '876 Patent, and each claim thereof, is unenforceable due to inequitable conduct during the prosecution of the '876 Patent.

86. During prosecution of the '876 Patent, Power Integrations failed to disclose to the United States Patent and Trademark Office ("PTO") prior art that was highly material to the patentability of the claims of the '876 patent under prosecution, and that Power Integrations knew or should have known would have been important to a reasonable examiner. The undisclosed prior art references include at least Power Integrations public disclosure of the technology described in Power Integrations '851 Patent.

87. Power Integrations purports to have invented the invention claimed in the '876 Patent on May 21, 1998. On information and belief, on September 2, 1997 and over eight months before the date of the alleged invention claimed in the '876 Patent, Power Integrations made public disclosure of the alleged invention of the '851 Patent. Thus, the alleged invention of the '851 Patent is prior art to the alleged invention of the '876 Patent pursuant to 35 U.S.C. § 102(a).

88. Indeed, in their Invention Disclosure Form, the inventors of the '876 Patent describe the alleged invention of the '851 Patent as "PRIOR ART" and include a Figure labeled "Frequency Jittering Prior Art." Power Integrations, however, never informed the Patent Office that the '851 Patent was prior art to the '876 Patent. Power Integrations included the figure from its Invention Disclosure Form that it had previously identified as "PRIOR ART" as Figure 3 of the '876 Patent. Rather than inform the Patent Office that this Figure depicted the prior art, Power Integrations simply stated that "FIG. 3 is a schematic diagram of an analog frequency jittering device" and incorporated the '851 Patent by reference into the specification of the '876 Patent.

89. The '851 Patent and the public disclosure of devices that embody the '851 Patent are highly material to the patentability of the claims of the '876 Patent and Power Integrations knew or should have known that they would have been important to a reasonable examiner.

90. An actual controversy, within the meaning of 28 U.S.C. §§ 2201 and 2202, exists between FAIRCHILD, on the one hand, and PI, on the other hand, with respect to whether the claims of the '876 Patent are enforceable or unenforceable.

Eighth Counterclaim: Declaratory Judgment of Unenforceability the '075 Patent

91. FAIRCHILD repeats and realleges paragraphs 1-10 of its Counterclaims, as if fully restated herein.

92. The '075 Patent, and each claim thereof, is unenforceable due to inequitable conduct during the prosecution of the '075 Patent.

93. During prosecution of the '075 Patent, the Applicant, Klaus Eklund, and his attorneys failed to disclose to the United States Patent and Trademark Office ("PTO") prior art that was highly material to the patentability of the claims of the '075 patent under prosecution, and that Mr. Eklund and his attorneys knew or should have known would have been important to a reasonable examiner. The undisclosed prior art references include at least technical articles known to Mr. Eklund that were published more than a year before the application leading to the '075 Patent was filed.

94. An actual controversy, within the meaning of 28 U.S.C. §§ 2201 and 2202, exists between FAIRCHILD, on the one hand, and PI, on the other hand, with respect to whether the claims of the '075 Patent are enforceable or unenforceable.

***A Highly Reliable 16 Output High Voltage NMOS/CMOS Logic IC with Shielded Source Structure*, by H. Wakaumi, T. Suzuki, M. Saito and H. Sakuma, IEDM 83, pp. 416-419 (1983) and *High-Voltage DMOS and PMOS in Analog IC's* by A.W. Ludikhuize, IEDM 82, pp. 81-84 (1982).**

95. The article "*A Highly Reliable 16 Output High Voltage NMOS/CMOS Logic IC with Shielded Source Structure*", by H. Wakaumi, T. Suzuki, M. Saito and H. Sakuma ("Wakaumi Article") and the article "*High-Voltage DMOS and PMOS in Analog IC's*" by A.W. Ludikhuize ("Ludikhuize Article") are highly material prior art to the patentability of the claims of the '075 patent, would have been important to a reasonable examiner, would have established at least a case of prima facie obviousness of the claims Mr. Eklund prosecuted in the application for the '075 Patent. The Wakaumi Article was published in the IEDM journal at least as early as 1983. A copy of the Wakaumi Article is attached hereto as Exhibit J. The Ludikhuize Article was published in the IEDM journal at least as early as 1982. A copy of the Ludikhuize Article is attached hereto as Exhibit K. Since both articles were published more than a year before Power Integrations filed the application leading to the '075 Patent, they are prior art to the '075 Patent.

96. The materiality of the Wakaumi and Ludikhuize Articles is demonstrated by the fact that Mr. Eklund was aware of both articles at the time he allegedly conceived of the '075 Patent, considered the articles to be "key" references, and specifically identified at least the

Wakaumi Article in notes that he now claims describe the invention leading to the '075 Patent. Indeed, one of ordinary skill in the art would have been motivated to combine the Wakaumi and Ludikhuize Articles and the combination of these Articles meets every element of each asserted claim of the '075 Patent. Thus, the claims of the '075 Patent are obvious in light of the Wakaumi and Ludikhuize Articles.

97. Despite his admitted knowledge and appreciation of the Wakaumi and Ludikhuize Articles, neither Mr. Eklund nor his attorneys disclosed either Article to the Patent Office during the prosecution of the '075 Patent. This constitutes inequitable conduct that renders all claims of the '075 Patent permanently unenforceable.

PRAYER FOR RELIEF

WHEREFORE, FAIRCHILD prays for the following relief:

A. The Court enter judgment against PI, and dismiss with prejudice, any and all claims of PI's First Amended Complaint for Patent Infringement; and order that Plaintiff take nothing as a result of the First Amended Complaint;

B. The Court enter judgment declaring that FAIRCHILD has not infringed, contributed to infringement of, or induced infringement of the '851 Patent, the '876 Patent, the '366 Patent, or the '075 Patent;

C. The Court enter judgment declaring that the '851 Patent, the '876 Patent, the '366 Patent, and the '075 Patent are invalid;

D. The Court enter judgment declaring that the '851 Patent, the '876 Patent, the '366 Patent, and the '075 Patent are unenforceable;

E. The Court award to FAIRCHILD its reasonable costs and attorneys' fees against PI pursuant to the provisions of 35 U.S.C. § 285;

F. The Court award to FAIRCHILD pre-judgment interest and costs of this action; and,

G. The Court grant to FAIRCHILD such other and further relief as may be deemed just and appropriate.

DEMAND FOR JURY TRIAL

Pursuant to Rule 38(b) of the Federal Rules of Civil Procedure and Rule 38.1 of the Local Rules of the United States District Court for the District of Delaware, Fairchild Semiconductor International, Inc. and Fairchild Semiconductor Corporation hereby demand a trial by jury on this action.

ASHBY & GEDDES

/s/ Lauren E. Maguire

Steven J. Balick (I.D. #2114)
John G. Day (I.D. #2403)
Lauren E. Maguire (I.D. #4261)
222 Delaware Avenue, 17th Floor
P.O. Box 1150
Wilmington, DE 19899
(302) 654-1888
sbalick@ashby-geddes.com
jday@ashby-geddes.com
lmaguire@ashby-geddes.com

*Attorneys for Defendants
Fairchild Semiconductor International,
Inc. and Fairchild Semiconductor
Corporation*

Of Counsel:

G. Hopkins Guy, III
Bas de Blank
ORRICK, HERRINGTON & SUTCLIFFE LLP
1000 Marsh Road
Menlo Park, CA 94025
Tel: (650) 614-7400

Dated: February 23, 2006
166925.1

Worldwide Operator

Search Harris

[Harris Home](#) | [Contact Us](#) | [About Harris](#) | [Careers](#) | [Investors](#)



HARRIS CORPORATION

[Home](#)

[Products](#)

[Support & Training](#)

[About Harris](#)

[Worldwide Operations](#)

[Investor Relations](#)

[Corporate Governance](#)

[News & Information](#)

[Tradeshows](#)

[Careers](#)

[Customer Login](#)

[Contact Us](#)

[Site Map](#)

Technical Excellence in the Same Time Zone

Customers around the globe want to be confident that their unique communications needs are understood and supported by people who are within easy reach. As part of Harris' commitment being a leader in the worldwide communications market, we have continued to strengthen our international position by establishing a strong local presence in each of the markets we serve. We call this endeavor "Technical Excellence in the Same Time Zone." It means that, wherever you are in the world, you have local or regional access to expert Harris sales and service personnel speak your language, understand your region's communications infrastructure, and are familiar with the regulatory requirements of your area.

Harris is headquartered in the U.S. and has sales and service facilities in more than 90 countries

- Corporate Headquarters
- Division Headquarters
- Worldwide Locations

CORPORATE HEADQUARTERS

Harris Corporation Headquarters
1025 West NASA Boulevard
Melbourne, Florida 32919-0001

For product information:

U.S. and Canada Callers dial: 1-800-4-HARRIS
International Callers dial: 1-321-727-9207

Switchboard:

Switchboard: 1-321-727-9100
Email: webmaster@harris.com

More contact information including maps and driving directions »

DIVISION HEADQUARTERS

Government Communications Systems Division

Communication, command, control, computer, and intelligence (C4I) systems; custom aircraft spaceborne communication systems; and data processing systems that collect, process, display and distribute information.

RF Communications Division
Secure radio products, systems, and networks; and encryption solutions for military, government and commercial organizations worldwide.

2400 Palm Bay Road, NE
Palm Bay, FL USA 32905
Tel: 1-321-727-9100
Fax: 1-321-727-4500
Email: govt@harris.com
View all Government Communications Systems Division locations

1680 University Avenue
Rochester, NY USA 14610
Tel: 1-585-244-5830
Fax: 585-242-4755
Email: rcomm@harris.com
View RF Communications Division Contacts

Broadcast Communications Division
Analog and digital broadcast equipment, studio systems, automation and network management systems.

4393 Digital Way
Mason, OH USA 45040
Tel: 1-513-459-3400
Fax: 1-513-701-5301
Email: broadcast@harris.com
View Broadcast Communications Division Contacts

Microwave Communications Division
Wireless network solutions.

Keystone Park
(Research Triangle Park)
637 Davis Drive
Morrisville, North Carolina 27560
Tel: 1-919-767-3230
Fax: 1-919-767-3233
Email: microwave@harris.com
View all Microwave Communications Division locations

WORLDWIDE LOCATIONS

Asia Pacific

Malaysia
Harris Asia Pacific (M) Sdn. Bhd.
Suite 803
Menara Amcorp,

Europe, Middle East and Africa

France
Harris Communication S.A.S.
Centrale Parc, Bâtiment n°4 Pasteur
Avenue Sully Prud'homme

Amcorp Trade Centre
No. 18 Jalan Pesiaran Barat
Petaling Jaya, Selangor
Malaysia 46050
Tel: 603-7956-8666
Fax: 603-7956-3666

Philippines

Harris Corporation
8/F Pacific Star Building
Sen. Gil Puyat Corner
Makati Avenue
Makati City, Manila
Philippines 1200
Tel: 632-818-5111 Ext: 102
Fax: 632-818-8165

Singapore

Harris Corporation
122 Middle Road, #04-03
Midlink Plaza
Singapore City
Singapore 188973
Tel: 65-6333-9038
Fax: 65-6333-9039

Thailand

Harris Corporation
ITF Tower II, 10/F
140/14 Silom Road
Khet Bangrak
Bangkok 10500
Thailand
Tel: 662-231-6219 or 6748
Fax: 662-231-6218

Vietnam

Harris Corporation
Unit 603, 6th Floor
Sun Red River Building
23 Phan Chu Trinh Street
Hoan Kiem District
Hanoi
Vietnam 10000
Tel: 844-933-1314
Fax: 844-933-1315

Canada

Montreal
Harris Corporation
3 Hôtel de Ville,
Dollard-des-Ormeaux
Montreal, Quebec

92298 Châtenay-Malabry Cedex
France
Tel: 33-1-55-52-80-00
Fax: 33-1-55-52-80-01

Harris - ITIS
Centre Espace Performance
Bâtiment 5
35769 Saint Gregoire Cedex
France
Tel: 33-2-99-23-7220
Fax: 33-2-99-23-1091

United Kingdom

Harris Systems Ltd.
Eskdale Road
Winnersh, Wokingham
Berkshire RG41 5TS
United Kingdom
Tel: 44-118-964-8000
Fax: 44-118-964-8001

Austria

Harris Corporation
Oberer Paspelsweg 6-8
6830 Rankweil-Brederis
Austria
Tel: 43-5522-9011-2200
Fax: 43-5522-9011-2561

Romania

Harris Communications
International Inc.
World Trade Center
Bd. Expozitie nr. 2
Ap. D 1.10, Et. 1
78334 Bucharest 1
Romania
Tel: +40-21-319-1262
Fax: +40-21-319-1123

Russia

Harris Corporation
15, Office 605, 6th Floor
Bolshoi Cherkassky Petreulok
Moscow 103626,
Russia
Tel: 7-095-923-3169
Fax: 7-095-927-0939

Saudi Arabia

Harris Corporation
P.O. Box 6777
King Abdul Azziz Road

Caribbean and Latin America

Canada H9B 3G4
Tel: 514-421-8400
Fax: 514-421-4222

Argentina

Harris Corporation
Tucumán 540 Piso 28 J
Buenos Aires
Argentina C1049AAL
Tel: 54-11-4325-0182
Fax: 54-11-4325-0183

Brazil

Harris do Brasil Ltda.

Edificio Stadium
Al. Rio Negro 1030
Conjuntos 202/204/206

Alphaville

Barueri, Sao Paulo

Brazil CEP 06454-000

Tel: 55-11-4197-3000

Fax: 55-11-4197-3001

Mexico

Harris S.A. de C.V.

Torre Esmeralda II

Blvd Manuel Avila Carmacho #36, Piso 17

Col Lomas de Chapultepec

Mexico D.F., C.P. 11000

Tel: 52-55-5249-3700

Fax: 52-55-5249-3701

Nigeria

Harris Communications Systems Nigeria Ltd
Imperial Place, Plot 274
Ajose Adeogun Street, VI
Lagos, Nigeria
Tel: 234-1-444-8888 or 234-1-444-8889
Fax: 234-1-270-1888

People's Republic of China

Beijing

Harris Corporation
Tower 2, Room 1817-1818
Beijing Bright China
Chang'An Building
No.7, Jian Guo Men Nei Avenue
Dong Cheng District,
Beijing 100005
P.R. China
Tel: 86-10-6510-1880
Fax: 86-10-6510-1870

Shanghai

Harris Communications Limited
Room 3711, Citic Square
1168 Nanjing Road (West),
Shanghai 200041
P.R. China
Tel: 86-21-5292-5660
Fax: 86-21-5292-5955

Shenzhen

Harris Communications
(Shenzhen) Ltd.
R3-B2, High-Tech Industrial Park
Nanshan District
Shenzhen 518057
P.R. China
Tel: 86-755-2663-7928
Fax: 86-755-2663-7048

assuredcommunications™

Contact Harris. Terms of Use. © 2006 Harris Cor

ATTORNEYS & AGENTS

Herbert L. Allen

Jeffrey S. Boyles

Paul J. Ditmeyer

Linda C. Dolan

Ava K. Doppelt

Robert Dyer

Enrique G. Estevez, Ph.D.

Brian R. Gilchrist

Jacqueline E. Hartt, Ph.D.

Meaghan P. Hemmings

David W. Henry

Stephen H. Luther

Stephen D. Milbrath

Carl M. Napolitano, Ph.D.

Cian G. O'Brien

Christopher F. Regan

David L. Sigalow

Ryan T. Santurri

David L. Stewart

Michael W. Taylor

Robert H. Thornburg

Charles E. Wands

ATTORNEYS & AGENTS

Charles E. Wands
Of Counsel, Registered Patent Attorney

Email:

cewands@addmg.com

Telephone:

407-841-2330

Facsimile:

407-841-2343

Orlando

Practice Areas:

- Patent Acquisition and Counseling

Admitted:

- 1982: Florida

- 1982: United States Supreme Court

- 1982: United States Court of Appeals, Fifth and Eleventh Circuits, District of Columbia

- 1982: United States District Court, Middle District of Florida, District of Columbia

- 1971: Virginia Bar

- 1971: District of Columbia Bar

- United States Patent and Trademark Office

Education:

- 1970: George Washington University, J.D.

- 1966: Georgia Institute of Technology B.S.E.E.




Biography:

Mr. Wands specializes in patent prosecution and patent infringement studies. He also counsels clients in electrical areas plus computer hardware and software. Mr. Wands was formerly a Patent Examiner for the United States Patent Office.

Richard K. Warther

John F. Woodson, II

 Print Page

Affiliations:

- American Bar Association
- The District of Columbia Bar
- The Florida Bar
- Society of Exploration Geophysicists
- Virginia Bar Association



[Español](#) [Locations](#) [Legal](#) [Sitemap](#) [Contact Us](#)

ALLEN

DYER

DOPPETT

MILBRATH &

GILCHRIST, P.A.

INTELLECTUAL PROPERTY ATTORNEYS

ABOUT US

ATTORNEYS & AGENTS

PRACTICE AREAS

RESOURCE CENTER

CONTACT US

 Print Page

Orlando (Principal Office)

Allen, Dyer, Doppelt, Milbrath & Gilchrist, P.A.
255 South Orange Avenue, Suite 1401
Orlando, Florida 32801
Tel.: 407-841-2330
Fax: 407-841-2343
The postal address for the Orlando office is:

Allen, Dyer, Doppelt, Milbrath & Gilchrist, P.A.
P.O. Box 3791
Orlando, Florida 32802-3791
Get Directions

Jacksonville

4720 Sallsbury Rd
Suite 241
Jacksonville, FL 32256
Tel: 904-470-0002
Fax: 407-841-2343
Get Directions

Melbourne

1901 S. Harbor City Blvd.,
Suite 507
Melbourne, Florida 32901
Tel.: 321-725-4760
Fax: 321-984-7078
Get Directions

Colorado Springs

102 South Tejon Street
Suite 1100
Colorado Springs, FL 80903

Get Directions

E-mail contact:

Direct contact: We prefer that you contact the attorney or agent of your choice directly by e-mail. Please check under the attorney or agent's name in our Attorneys & Agents section for the direct e-mail address.

General inquiry: If you prefer to send a general inquiry to the firm, you may send an e-mail to:

info@addmg.com

[Español](#) [Locations](#) [Legal](#) [Sitemap](#) [Contact Us](#)



IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS

MARSHALL DIVISION

FAIRCHILD SEMICONDUCTOR
CORPORATION, a Delaware corporation,
INTERSIL AMERICAS, INC., a Delaware
corporation and INTERSIL CORPORATION,
a Delaware corporation

Plaintiff,

v.

POWER INTEGRATIONS, INC., a Delaware
corporation,

Defendants.

CIVIL ACTION NO. 2:06-cv-151

**DECLARATION OF GABRIEL M. RAMSEY IN SUPPORT OF
OPPOSITION TO MOTION TO DISMISS OR, IN THE ALTERNATIVE,
TO TRANSFER THIS CASE TO DELAWARE**

I, Gabriel M. Ramsey, the undersigned, declare as follows:

1. I am an associate at the Menlo Park office of Orrick, Herrington & Sutcliffe, LLP. I have personal knowledge of each fact stated herein, and am competent to testify to the same.

2. Attached hereto as Exhibit 1 is a true and correct copy of the September 27, 1999 assignment of the '719 Patent from Harris Corp. to Intersil Corp.

3. Attached hereto as Exhibit 2 is a true and correct copy of the restated certificate of incorporation of Intersil Corp., changing its name to Intersil Communications, Inc.

4. Attached hereto as Exhibit 3 is a true and correct copy of the April 14, 2006 assignment of the '719 Patent from Intersil Communications, Inc. to Intersil Americas, Inc.

5. Attached hereto as Exhibit 4 is a true and correct copy of a redacted version of the March 30, 2006 exclusive license of the '719 Patent from Intersil Corp. to Fairchild Semiconductor Corp.

6. Attached hereto as Exhibit 5 is a true and correct copy of the May 17, 2006

Supplemental Agreement, effective March 30, 2006, between Intersil Corp., Intersil Americas, Inc. and Fairchild Semiconductor Corp. ratifying and granting the exclusive license of the '719 Patent to Fairchild Semiconductor Corp.

7. Attached hereto as Exhibit 6 is a true and correct copy of "Plaintiff's Amended Complaint," filed in the instant action by Fairchild Semiconductor Corp., Intersil Americas, Inc. and Intersil Corp. against Power Integrations, Inc. and asserting U.S. Patent No. 5,264,719.

8. Attached hereto as Exhibit 7 is a true and correct copy of the "First Amended Complaint for Patent Infringement," filed in the Delaware action (C.A. No. 04-1371-JJV) by Power Integrations, Inc. against Fairchild Semiconductor Int'l, Inc. and Fairchild Semiconductor Corp., and asserting U.S. Patent Nos. 6,107,851, 6,249,876, 6,229,366, and 4,811,075.

9. Attached hereto as Exhibit 8 is a true and correct copy of "Defendants Fairchild Semiconductor International, Inc. and Fairchild Semiconductor Corporation's First Amended Answer And Counterclaims To Plaintiff's First Amended Complaint for Patent Infringement and Demand for Jury Trial," filed in the Delaware action (C.A. No. 04-1371-JJV). In this document Fairchild does not allege any counterclaims of infringement of any patent.

10. Attached hereto as Exhibit 9 is a true and correct copy of a document located at <<http://www.harris.com/harris/contact/worldwide-operations.html#1>> indicating that Harris Corporation's corporate headquarters are located in Melbourne, Florida.

11. Attached hereto as Exhibit 10 are true and correct copies of documents located at <http://www.addmg.com/people_wands.html> and <<http://www.addmg.com/contact.html>> indicating that attorney Charles E. Wands is located in Orlando, Florida.

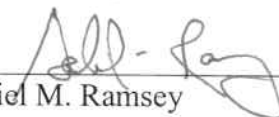
12. Some of the same claim language is used between the '719 Patent in this case and the '075 Patent in the Delaware action. However, the claims are not identical. The specifications and file histories of the patents-in-suit in the Delaware action and the '719 Patent in suit in the instant action are different. The '719 Patent has a different inventor than the patents-in-suit in Delaware. Different products are accused to infringe in the Delaware action (Fairchild's products are accused there) and the instant action (PI's products are accused here).

13. The '719 Patent is asserted among other prior art in the Delaware action. However, the primary prior art assertion in the Delaware case involves not the '719 Patent, but its "parent" patent.

14. In the Delaware action, a bifurcated trial is set for October, 2006 and December, 2006. Substantial discovery has been conducted regarding infringement, validity and enforceability of the four patents at issue in that case. Summary judgment motions have been heard and ruled upon. Pre-trial materials have been exchanged. Infringement of the '719 Patent is not asserted in the Delaware action, therefore pre-trial proceedings have not and trial in that action will not deal with infringement, validity or enforceability of the '719 Patent.

15. Upon information and belief, the only appearance that Intersil has made in the Delaware action (C.A. No. 04-1371-JJV) was to file a motion to quash on the basis that discovery related to the above-captioned action should be left to and decided by this Court

I declare under penalty of perjury under the laws of the United States that the foregoing is true and correct. Executed in Menlo Park, California on July 26, 2006.



Gabriel M. Ramsey

IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS

MARSHALL DIVISION

FAIRCHILD SEMICONDUCTOR
CORPORATION, a Delaware corporation,
INTERSIL AMERICAS, INC., a Delaware
corporation and INTERSIL CORPORATION,
a Delaware corporation

Plaintiff,

v.

POWER INTEGRATIONS, INC., a Delaware
corporation,

Defendants.

CIVIL ACTION NO. 2:06-cv-151

**ORDER DENYING POWER INTEGRATIONS' MOTION TO DISMISS OR, IN THE
ALTERNATIVE, TO TRANSFER THIS CASE TO DELAWARE**

ON THIS DAY, came on to be considered Power Integrations, Inc.'s Motion to Dismiss,
or in the Alternative, to Transfer This Case to Delaware in the above-styled and numbered cause.
After considering said motion, the Court is of the opinion that said motion should be DENIED.

Appendix K

Revised: 12/3/03

UNITED STATES DISTRICT COURT
EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION
APPLICATION TO APPEAR PRO HAC VICE

06 JUL '08 PM 3:24

1. This application is being made for the following: Case No. 2-06CV-151
Style: Fairchild Semiconductor Corporation and Intersil Corporation v. Power Integrations.
2. Applicant is representing the following party/ies: Fairchild Semiconductor Corporation
3. Applicant was admitted to practice in California in December 1986
4. Applicant is in good standing and is otherwise eligible to practice law before this court.
5. Applicant is not currently suspended or disbarred in any other court
6. Applicant ~~has~~ has not had an application for admission to practice before another court denied (please circle appropriate language). If so, give complete information on a separate page.
7. Applicant ~~has~~ has not ever had the privilege to practice before another court suspended (please circle). If so, give complete information on a separate page.
8. Applicant ~~has~~ has not been disciplined by a court or Bar Association or committee thereof that would reflect unfavorably upon applicant's conduct, competency or fitness as a member of the Bar (please circle). If so, give complete information on a separate page.
9. Describe in detail on a separate page any charges, arrests or convictions for criminal offense(s) filed against you. Omit minor traffic offenses.
10. There are no pending grievances or criminal matters pending against the applicant.
11. Applicant has been admitted to practice in the following courts:
Supreme Court of Virginia (inactive); Supreme Court of California; US District Court, ND California; US Court of Appeals for the 9th Circuit; US Court of Appeals for the Federal Circuit; and US Patent and Trademark Office.
12. Applicant has read and will comply with the Local Rules of the Eastern District of Texas, including Rule AT-3, the "Standards of Practice to be Observed by Attorneys."
13. Applicant has included the requisite \$25 fee (see Local Rule AT-1(d)).
14. Applicant understands that ~~he~~ she is being admitted for the limited purpose of appearing in the case specified above only.

Appendix K

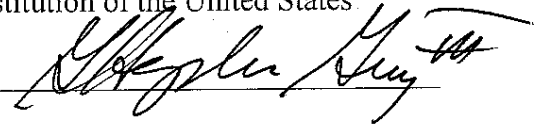
Revised: 12/3/03

Application Oath:

I, G. Hopkins Guy, III, do solemnly swear (or affirm) that the above information is true; that I will discharge the duties of attorney and counselor of this court faithfully; that I will demean myself uprightly under the law and the highest ethics of our profession; and that I will support and defend the Constitution of the United States.

Date: April __, 2006

Signature



Name: G. Hopkins Guy, III

State Bar Number: 124811

Firm Name: Orrick, Herrington & Sutcliffe LLP

Address/P O. Box: 1000 Marsh Road

City/State/Zip: Menlo Park, CA 94025

Telephone #: (650) 614-7400

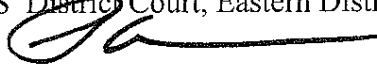
Fax #: (650) 614-7401

E-mail Address: hopguy@orrick.com

Applicant is authorized to enter an appearance as counsel for the party/parties listed above. This application has been approved for the court this 18 day of

July, 20 06

David J Maland, Clerk
U.S. District Court, Eastern District of Texas



By

Deputy Clerk

Appendix K

Revised: 12/3/03

UNITED STATES DISTRICT COURT
EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION
APPLICATION TO APPEAR PRO HAC VICE

06 JUL 18 PM 3:24

TE DISTRICT MARSHALL

10 BY



1. This application is being made for the following: Case No.:# 2-06CV-151
Style: Fairchild Semiconductor Corporation and Intersil Corporation v. Power Integrations
2. Applicant is representing the following party/ies: Fairchild Semiconductor Corporation
3. Applicant was admitted to practice in California in 1997
4. Applicant is in good standing and is otherwise eligible to practice law before this court
5. Applicant is not currently suspended or disbarred in any other court.
6. Applicant has has not had an application for admission to practice before another court denied (please circle appropriate language). If so, give complete information on a separate page.
7. Applicant has has not ever had the privilege to practice before another court suspended (please circle). If so, give complete information on a separate page
8. Applicant has has not been disciplined by a court or Bar Association or committee thereof that would reflect unfavorably upon applicant's conduct, competency or fitness as a member of the Bar (please circle). If so, give complete information on a separate page.
9. Describe in detail on a separate page any charges, arrests or convictions for criminal offense(s) filed against you. Omit minor traffic offenses
10. There are no pending grievances or criminal matters pending against the applicant.
11. Applicant has been admitted to practice in the following courts:
Northern District of California and Central District of California
12. Applicant has read and will comply with the Local Rules of the Eastern District of Texas, including Rule AT-3, the "Standards of Practice to be Observed by Attorneys."
13. Applicant has included the requisite \$25 fee (see Local Rule AT-1(d)).
14. Applicant understands that he/she is being admitted for the limited purpose of appearing in the case specified above only

Appendix K

Revised: 12/3/03

Application Oath:

I, Bas de Blank, do solemnly swear (or affirm) that the above information is true; that I will discharge the duties of attorney and counselor of this court faithfully; that I will demean myself uprightly under the law and the highest ethics of our profession; and that I will support and defend the Constitution of the United States.

Date: July 17, 2006

Signature Bas de Blank

Name: Bas de Blank

State Bar Number: 191487

Firm Name: Orrick, Herrington & Sutcliffe LLP

Address/P O. Box: 1000 Marsh Road

City/State/Zip: Menlo Park, CA 94025

Telephone #: (650) 614-7400

Fax #: (650) 614-7401

E-mail Address: basdeblank@orrick.com

Applicant is authorized to enter an appearance as counsel for the party/parties listed above. This application has been approved for the court this 18 day of

July, 2006.

David J. Maland, Clerk

U S. District Court, Eastern District of Texas

By

[Signature]
Deputy Clerk

Appendix K

Revised: 12/3/03

UNITED STATES DISTRICT COURT
EASTERN DISTRICT OF TEXAS
Marshall DIVISION
APPLICATION TO APPEAR PRO HAC VICE

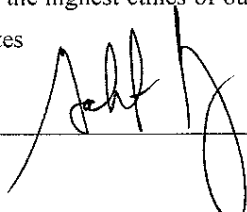
06 JUL 18 PM 3:26

- 1 This application is being made for the following: Case # 2:06-CV-151 IN EASTERN DISTRICT OF TEXAS
Style: Fairchild Semiconductor Corp. et al v. Power Integrations, Inc.
- 2 Applicant is representing the following party/ies:
Fairchild Semiconductor Corp.; Intersil Corp.; Intersil Americas
- 3 Applicant was admitted to practice in CA (state) on Dec. 4, 2000 (date)
- 4 Applicant is in good standing and is otherwise eligible to practice law before this court
- 5 Applicant is not currently suspended or disbarred in any other court.
- 6 Applicant has has not had an application for admission to practice before another court denied (please circle appropriate language) If so, give complete information on a separate page.
- 7 Applicant has has not ever had the privilege to practice before another court suspended (please circle) If so, give complete information on a separate page
- 8 Applicant has has not been disciplined by a court or Bar Association or committee thereof that would reflect unfavorably upon applicant's conduct, competency or fitness as a member of the Bar (please circle) If so, give complete information on a separate page
9. Describe in detail on a separate page any charges, arrests or convictions for criminal offense(s) filed against you Omit minor traffic offenses N/A
10. There are no pending grievances or criminal matters pending against the applicant
- 11 Applicant has been admitted to practice in the following courts:
California State Courts; U.S. District Courts (N.D.Cal; C.D.Cal; S.D.Cal.); Ninth Circuit Court of Appeals
- 12 Applicant has read and will comply with the Local Rules of the Eastern District of Texas, including Rule AT-3, the "Standards of Practice to be Observed by Attorneys"
- 13 Applicant has included the requisite \$25 fee (see Local Rule AT-1(d)).
- 14 Applicant understands that he/she is being admitted for the limited purpose of appearing in the case specified above only.

Application Oath:

I, Gabriel M. Ramsey do solemnly swear (or affirm) that the above information is true; that I will discharge the duties of attorney and counselor of this court faithfully; that I will demean myself uprightly under the law and the highest ethics of our profession; and that I will support and defend the Constitution of the United States

Date 07/17/06


Signature 

Name (please print) Gabriel M. Ramsey
State Bar Number 209218
Firm Name: Orrick Herrington & Sutcliffe
Address/P.O. Box: 1000 Marsh Road
City/State/Zip: Menlo Park, CA 94025
Telephone #: (650) 614-7400
Fax #: (650) 614-7401
E-mail Address: gramsey@orrick.com

Applicant is authorized to enter an appearance as counsel for the party/parties listed above. This application has been approved for the court this 18 day of July, 2006.

David J. Maland, Clerk
U.S. District Court, Eastern District of Texas

By


Deputy Clerk

UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

FAIRCHILD SEMICONDUCTOR
CORPORATION, a Delaware corporation,
INTERSIL AMERICAS, INC., a Delaware
corporation, and INTERSIL
CORPORATION, a Delaware corporation,

Plaintiffs,

v.

POWER INTEGRATIONS, INC., a
Delaware corporation,

Defendants.

C.A. No. 2-06CV-151 JTW

Jury

**POWER INTEGRATIONS' REPLY IN SUPPORT OF MOTION TO DISMISS OR, IN
THE ALTERNATIVE, TO TRANSFER THIS CASE TO DELAWARE**

Fairchild and Intersil's opposition to Power Integrations' Motion to Dismiss or Transfer ("Opposition") is long on rhetoric and short on common sense. In Delaware, Fairchild says the '719 patent at issue in this case is the same as the '075 patent asserted in Delaware. That invalidity argument is Fairchild's primary defense in Delaware, where the court is educated in the technology and invested in the case. If there were ever a case of a belated, unnecessary filing, Fairchild's Texas case is it. No one ever suggested this Court does not have jurisdiction, or that this Court is not a perfectly fine place to litigate a patent case, but that is not the issue at hand. This Court has consistently transferred cases where a prior action involved the same real parties in interest and substantially the same issues. Despite Plaintiffs' best efforts to obscure the facts, that is the situation here.

A. Intersil's Alleged Standing Does Not Moot Power Integrations' Motion.

Most of the Opposition emphasizes that Fairchild has exclusive rights against Power Integrations – exclusive “even as to Intersil.” *See, e.g.*, Opposition at 4-6. To make this point, Plaintiffs quote the relevant language from the license, *id.*, and they further argue that Fairchild is the real party in interest in this case. *Id.* at 13. If that is the case, though, Intersil has no rights against Power Integrations, both in form and in substance, and it therefore cannot maintain any sort of action against Power Integrations. Because Intersil has no standing to sue Power Integrations, with or without Fairchild, the addition of Intersil as a party cannot be sufficient to moot the motion at hand.

B. Power Integrations Did Not Misstate the Standard for Standing.

Fairchild does not have standing in this case—even as a co-plaintiff with the patentee. There is no case stating that a party with rights limited in the manner of Fairchild’s – i.e., having the right only to pursue a single target – has standing of any kind, even as a co-plaintiff. If there were any such law, the Court can be certain that Fairchild and Intersil would have cited it. They did not, and that failure is fatal to Plaintiffs’ argument.

Moreover, the fact that Fairchild and Intersil chose to draft their license such that neither can presently sue Power Integrations is their problem, not Power Integrations’. Plaintiffs suggest this cannot be the law, Opposition at 6, but they again provide no authority for their assertion. The standing requirements are clear, and parties can choose to satisfy them or not. Fairchild and Intersil have not provided any reasons or basis upon which the Court might fix the problem, and the Court should decline to do so.

C. To the Extent the Court Does Not Dismiss This Case, It Should Transfer the Case to Delaware.

This case is a simple slap-back suit that involves the same subject matter as the earlier-filed Delaware case. To whatever extent the Court does not believe the problems with the license as drafted are fatal to the instant suit, it should transfer the case to Delaware.

1. The Issues and Witnesses in this Case Will Significantly Overlap with the Delaware Case.

Plaintiffs' failure to engage on Power Integrations' primary argument – that Fairchild's validity defense in the Delaware case turns on who was first to invent the subject matter of the '719 patent – shows that transfer is wholly proper in this context. The fact that Fairchild waited so long to file this case is irrelevant; if anything, it underscores how wasteful it would be to start litigating the same issues in Texas at this point.

Plaintiffs' assertion that their Texas cases involves "entirely different parties and issues" (e.g., page 6 and footnote 8) is demonstrably false. First, Plaintiffs inexplicably argue that the Delaware case involves "two different Fairchild entities," Opposition at 7, but there is no dispute that Fairchild Semiconductor Corporation – the real party in interest – is involved in both suits. *See Ramsey Decl. re Opposition at ¶¶ 8-9 and Exhibit 9.* Second, the core validity issue for both the '075 patent asserted in Delaware and the '719 patent in this matter – who invented the common subject matter first – is the same in both cases. *See Power Integrations' Opening Brief at 8-9.* In fact, the alleged common subject matter in these two patents is Fairchild's core argument in both cases. Trying to avoid this simple fact by directing the Court to the Delaware answer and counterclaims, rather than to the issues as already developed in discovery and as they will in fact be presented at trial, will not make it go away. In short, Plaintiffs have no principled response to the fundamental point on which this motion turns.

Plaintiffs are also incorrect with respect to the products in question, as the products in fact overlap. Although Fairchild has yet to accused any specific products of infringement, the Power Integrations products that will be accused of infringement in this Texas case are no doubt the products that practice the '075 patent asserted in the Delaware case, and Power Integrations will be putting on evidence of those products at trial to show commercial success of the '075 patent. Conversely, the Fairchild products that infringe the '075 patent (which will also, obviously, be explored in detail at the first Delaware trial) will be among the products Plaintiffs no doubt rely on in Texas to show their own commercial success. Every coin has two sides, and this is no exception.

2. Delaware Is More Convenient and Will Be More Efficient in this Case.

Plaintiffs' convenience analysis is nonexistent. Plaintiffs identify no witness in Texas, just as Power Integrations predicted. *See* Power Integrations' Opening Brief at 12. There may be a single prosecuting attorney in Florida, but no one has suggested the prosecuting attorney would be a trial witness, so that is beside the point. Notably, Plaintiffs are careful to avoid naming "the '719 inventor" – Jim Beasom – because the reality there is that he is a paid consultant to Plaintiffs who will travel wherever they ask. In fact, Mr. Beasom has already been listed on Fairchild's trial witness list in the Delaware matter. *See* Declaration of Mike Jones ("Jones Decl.") Ex. I. As such, the witness factors do not favor Texas. As for parties, the caption to Plaintiffs' Opposition shows that all three are Delaware corporations, and Fairchild's Maine operations are far closer to Delaware than to Texas, additional factors that favor the Delaware action.

As for Plaintiffs' "staggering inefficiencies" argument, Opposition at 13, the mere pendency of the two suits has already demonstrated where the true inefficiency lies. Rather than

waiting for the October and December trials to decide the core issue in common – who was first to invent the subject matter of the '075 patent – Plaintiffs seek to maintain a parallel case in Texas. Then, rather than have the Delaware Court decide what to do with what remains (if anything) of the '719 case when it is already completely familiar with the substantive issues, Plaintiffs want to ask another, already overburdened, Court to start over. That simply cannot be anyone's definition of "efficient."

As a last-ditch effort, Plaintiffs present a real party in interest argument that contradicts what they said elsewhere in their opposition. Although most of Plaintiffs' brief makes the point that Fairchild (the same Fairchild as in the Delaware case) is the real party in interest here, for the transfer argument, Plaintiffs flip-flop and say that **Intersil** is the real party in interest. Opposition at 13. This inconsistency is fatal to the instant motion, as it reveals the utter lack of substance to Plaintiffs' position.

The Court should therefore grant Power Integrations' Motion to Dismiss or, in the alternative, transfer this case to Delaware for Judge Farnan to address in light of the current dispute between Fairchild and Power Integrations.

Dated: August 2, 2006

Respectfully submitted,

OF COUNSEL

Frank E. Scherkenbach
Fish & Richardson P.C.
225 Franklin Street
Boston, Massachusetts 02110-2804
Telephone: (617) 542-5070
Facsimile: (617) 542-8906

By: /s/ Michael E. Jones
Michael E. Jones
State Bar No. 10929400
mikejones@potterminton.com
POTTER MINTON
A Professional Corporation
110 N. College, Suite 500
Tyler, TX 75702
Telephone: (903) 597-8311
Facsimile: (903) 593-0846

Attorneys for Defendant
POWER INTEGRATIONS, INC.

CERTIFICATE OF SERVICE

The undersigned hereby certifies that all counsel of record who are deemed to have consented to electronic service are being served with a copy of this document via the Court's CM/ECF system per Local Rule CV-5(a)(3) on August 2, 2006. Any other counsel of record will be served by facsimile transmission and first class mail on this date.

/s/ Michael E. Jones

Michael E. Jones

UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

FAIRCHILD SEMICONDUCTOR
CORPORATION, a Delaware corporation,
INTERSIL AMERICAS, INC., a Delaware
corporation, and INTERSIL
CORPORATION, a Delaware corporation,

Plaintiffs,

v.

POWER INTEGRATIONS, INC., a
Delaware corporation,

Defendants.

C.A. No. 2-06CV-151 JTW

Jury

**DECLARATION OF MICHAEL E. JONES IN SUPPORT OF POWER
INTEGRATIONS' REPLY IN SUPPORT OF MOTION TO DISMISS OR, IN THE
ALTERNATIVE, TO TRANSFER THIS CASE TO DELAWARE**

I, Michael E. Jones, hereby state that I am over 21 years of age and make this declaration based upon my personal knowledge and/or information and belief:

1. I filed a Notice of Appearance in this case on April 21, 2006. I am counsel for the Defendant, Power Integrations, Inc.

2. Attached hereto as Exhibit "I" is a true and correct copy of Exhibit 9, Defendants' Witness List provided by Fairchild Semiconductor International, Inc. and Fairchild Semiconductor Corp in the Delaware action.

I declare under penalty of perjury under the laws of the United States of America that the foregoing declaration is true and correct.

Executed this 2nd day of August, 2006.

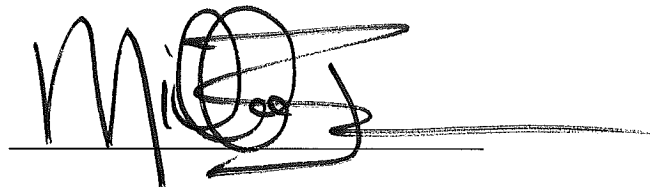
A handwritten signature in black ink, appearing to read "Michael E. Jones", written over a horizontal line.

EXHIBIT I

EXHIBIT 9**Defendants' Witness List**

Defendants Fairchild Semiconductor International, Inc. and Fairchild Semiconductor Corp. may call one or more of the following witnesses in its case in chief as a live witness.

Fairchild reserve the right to have the witness testify through deposition:

Name	Address
James D. Beasom	James D. Beasom 506 South Wildwood Ln Melbourne FL 32904-2562
Thomas Beaver	Fairchild Semiconductor Corporation 82 Running Hill Road South Portland, ME 04106
Robert Conrad	Fairchild Semiconductor Corporation 82 Running Hill Road South Portland, ME 04106
Peter Gwozdz <i>Fairchild's Expert Witness</i> Specialty – Semiconductor processes and structures.	College of Engineering San Jose State University San Jose CA 95192
Paul Horowitz <i>Fairchild's Expert Witness</i> Specialty – Electronic circuit design, including PWM devices.	Harvard, FAS Department of Physics Lyman Lab 225 19 Oxford St Cambridge MA 02138
KO Jang	Fairchild Korea Semiconductor Ltd. (420-711) 82-3 Todang-Dong Wonmi-District Bucheon City, Kyonggi Province Korea
C.K. Jeon	Fairchild Korea Semiconductor Ltd. (420-711) 82-3 Todang-Dong Wonmi-District Bucheon City, Kyonggi Province Korea
Michael Keeley <i>Fairchild's Expert Witness</i> Specialty – Economics, including patent damages.	Cornerstone Research 1000 El Camino Real Menlo Park, CA 94025
Bob Moore	Bob Moore 143 Dickinson St. NE Palm Bay, FL 32907

Robert Morrill	Sidley, Austin, Brown & Wood LLP 555 California Street Suite 2000 San Francisco, CA 94104
John Prentice	Conexant 2401 Palm Bay Rd., NE Bldg. 62, Mail Stop B017 Room B294 Palm Bay, FL 32905
Stephen Schott	Fairchild Semiconductor Corporation 82 Running Hill Road South Portland, ME 04106
Gu-Yeon Wei <i>Fairchild's Expert Witness</i> Specialty – Electronic circuit design, including PWM devices.	Harvard, FAS Department of Physics Lyman Lab 225 19 Oxford St Cambridge MA 02138

In addition, Defendants Fairchild Semiconductor International, Inc. and Fairchild Semiconductor Corp. may call one or more of the following witnesses to testify via deposition. Fairchild reserves the right to have them testify as a live witness:

Fairchild will provide this identification along with its deposition designations according to the schedule agreed to by the parties.

Appendix K

Revised: 12/3/03

UNITED STATES DISTRICT COURT
EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION
APPLICATION TO APPEAR PRO HAC VICE

FILED CLERK
U.S. DISTRICT COURT

2006 AUG -3 PM 4: 13

1. This application is being made for the following: Case # 2:06-cv-00151 TJW

Style: Fairchild Semiconductor Corporation, et al v. Power Integrations, Inc.

TEXAS EASTERN

2. Applicant is representing the following party/ies:

BY JA

Power Integrations, Inc.

3. Applicant was admitted to practice in CA (state) on 11/26/02 (date)

4. Applicant is in good standing and is otherwise eligible to practice law before this court.

5. Applicant is not currently suspended or disbarred in any other court.

6. Applicant ~~has~~ has not had an application for admission to practice before another court denied (please circle appropriate language). If so, give complete information on a separate page.

7. Applicant ~~has~~ has not ever had the privilege to practice before another court suspended (please circle). If so, give complete information on a separate page.

8. Applicant ~~has~~ has not been disciplined by a court or Bar Association or committee thereof that would reflect unfavorably upon applicant's conduct, competency or fitness as a member of the Bar (please circle). If so, give complete information on a separate page.

9. Describe in detail on a separate page any charges, arrests or convictions for criminal offense(s) filed against you. Omit minor traffic offenses.

10. There are no pending grievances or criminal matters pending against the applicant.

11. Applicant has been admitted to practice in the following courts:

CAFC; CA 9th Cir.; USDC, N.D. CA; USDC, S.D. CA; USDC, C.D. CA; USDC, E.D. CA

12. Applicant has read and will comply with the Local Rules of the Eastern District of Texas, including Rule AT-3, the "Standards of Practice to be Observed by Attorneys."

13. Applicant has included the requisite \$25 fee (see Local Rule AT-1(d)).

14. Applicant understands that he/~~she~~ is being admitted for the limited purpose of appearing in the case specified above only.

Application Oath:

I, Michael R. Headley do solemnly swear (or affirm) that the above information is true; that I will discharge the duties of attorney and counselor of this court faithfully; that I will demean myself uprightly under the law and the highest ethics of our profession; and that I will support and defend the Constitution of the United States.

Date 7/31/06

Signature Michael R. Headley

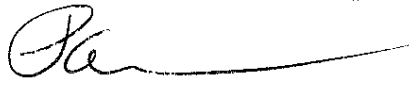
Name (please print) Michael R. Headley
State Bar Number CA 220834
Firm Name: Fish & Richardson P.C.
Address/P O. Box: 500 Arguello Street, Ste 500
City/State/Zip: Redwood City, CA 94063
Telephone #: (650) 839-5070
Fax #: (650) 839-5071
E-mail Address: headley@fr.com

Applicant is authorized to enter an appearance as counsel for the party/parties listed above. This application has been approved for the court this 3 day of July, 2006

David J. Maland, Clerk

U.S. District Court, Eastern District of Texas

By


Deputy Clerk

Appendix K

UNITED STATES DISTRICT COURT
EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION
APPLICATION TO APPEAR PRO HAC VICE

Revised: 12/3/03

FILED CLERK
U.S. DISTRICT COURT

2006 AUG -3 PM 4:13

1. This application is being made for the following: Case # 2:06-cv-00151-TJW TEXAS EASTERN
Style: Fairchild Semiconductor Corporation, et al v. Power Integrations, Inc.
BY [Signature]
2. Applicant is representing the following party/ies:
Power Integrations, Inc.
3. Applicant was admitted to practice in MA & CA (state) on 05/14/03 (date)
12/89
4. Applicant is in good standing and is otherwise eligible to practice law before this court.
5. Applicant is not currently suspended or disbarred in any other court.
6. Applicant ~~has~~ has not had an application for admission to practice before another court denied (please circle appropriate language). If so, give complete information on a separate page.
7. Applicant ~~has~~ has not ever had the privilege to practice before another court suspended (please circle). If so, give complete information on a separate page.
8. Applicant ~~has~~ has not been disciplined by a court or Bar Association or committee thereof that would reflect unfavorably upon applicant's conduct, competency or fitness as a member of the Bar (please circle). If so, give complete information on a separate page.
9. Describe in detail on a separate page any charges, arrests or convictions for criminal offense(s) filed against you. Omit minor traffic offenses.
10. There are no pending grievances or criminal matters pending against the applicant.
11. Applicant has been admitted to practice in the following courts: California Supreme Court; CAFC; USDC, D. MA; USDC, N.D. CA; USDC, C.D. CA; USDC, E.D. CA
12. Applicant has read and will comply with the Local Rules of the Eastern District of Texas, including Rule AT-3, the "Standards of Practice to be Observed by Attorneys."
13. Applicant has included the requisite \$25 fee (see Local Rule AT-1(d)).
14. Applicant understands that he/~~she~~ is being admitted for the limited purpose of appearing in the case specified above only.

Application Oath:

I, Frank E. Scherkenbach do solemnly swear (or affirm) that the above information is true; that I will discharge the duties of attorney and counselor of this court faithfully; that I will demean myself uprightly under the law and the highest ethics of our profession; and that I will support and defend the Constitution of the United States.

Date 8/3/06


Signature

Frank E. Scherkenbach

Name (please print) Frank E. Scherkenbach
State Bar Number MA (653819) CA (142549)
Firm Name: Fish & Richardson P.C.
Address/P.O. Box: 225 Franklin Street
City/State/Zip: Boston, MA 02110
Telephone #: (617) 542-5070
Fax #: (617) 542-8906
E-mail Address: scherkenbach@fr.com
Secondary E-Mail Address: kryan@fr.com

Applicant is authorized to enter an appearance as counsel for the party/parties listed above. This application has been approved for the court this 3 day of Aug, 2006

David J. Maland, Clerk
U.S. District Court, Eastern District of Texas

By 

Deputy Clerk

Respectfully submitted,

/s/ Allen F. Gardner

Allen F. Gardner
State Bar No. 24043679
allengardner@potterminton.com
POTTER MINTON
A Professional Corporation
110 N. College, Suite 500
Tyler, Texas 75702
903/597-8311
903/593-0846 Facsimile

ATTORNEYS FOR POWER
INTEGRATIONS, INC.

CERTIFICATE OF SERVICE

I hereby certify that all counsel of record who have consented to electronic service and are being served with a copy of this document via the Court's CM/ECF system per Local Rule CV-5(a)(3) on this the 4th day of October, 2006. Any other counsel of record will be served by first class mail on this same date.

/s/ Allen F. Gardner

Allen F. Gardner

UNITED STATES DISTRICT COURT

EASTERN

DISTRICT OF

TEXAS

FAIRCHILD SEMICONDUCTOR CORP.,
ET AL.
V.
POWER INTEGRATIONS, INC.

NOTICE

CASE NUMBER: 2:06-CV-151(TJW)

TYPE OF CASE:

☒ CIVIL☐ CRIMINAL

X TAKE NOTICE that a proceeding in this case has been set for the place, date, and time set forth below:

PLACE
United States District Court
100 E. Houston Street
MARSHALL, TX 75670

ROOM NO.
Judge T. John Ward's Courtroom
DATE AND TIME
March 6, 2007 @ 1:30 p.m.

TYPE OF PROCEEDING

SCHEDULING CONFERENCE

TAKE NOTICE that a proceeding in this case has been continued as indicated below:

PLACE	DATE AND TIME PREVIOUSLY SCHEDULED	CONTINUED TO DATE AND TIME
-------	------------------------------------	----------------------------

David J. Maland
US MAGISTRATE JUDGE OR CLERK OF COURT

January 26, 2007
DATE

Sonja H. Dupree
(BY) DEPUTY CLERK

TO: ALL COUNSEL OF RECORD

ACKNOWLEDGMENT

NOTICE TO COUNSEL: Please sign in the space provided below and return to the court by facsimile, (903) 935-2295, within three (3) days of your receipt of the enclosed notice.

I acknowledge receipt of the indicated notice on the date shown below.

Case No. _____

Signature of Atty. _____
Date

Print Name of Atty. _____

Counsel for _____
(Name of Party)

Type of Proceeding: _____
(e.g., Scheduling Conference)

Date of Proceeding: _____

Time of Proceeding: _____

Location of Proceeding: _____

IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

FAIRCHILD SEMICONDUCTOR .	§	
CORPORATION, a Delaware corporation,	§	
INTERSIL AMERICAS, INC., a Delaware	§	
corporation, and INTERSIL	§	
CORPORATION, a Delaware corporation	§	
	§	
V.	§	CIVIL NO. 2:06-CV-151(TJW)
	§	
POWER INTEGRATIONS, INC., a	§	
Delaware corporation	§	

**NOTICE OF SCHEDULING CONFERENCE,
PROPOSED DEADLINES FOR DOCKET CONTROL ORDER
AND DISCOVERY ORDER**

The court, *sua sponte*, issues this Notice of Scheduling Conference, Proposed Deadlines for Docket Control Order and Discovery Order.

Notice of Scheduling Conference

Pursuant to Fed. R. Civ. P. 16 and Local Rule CV-16, the Scheduling Conference in this case is set for **March 6, 2007, at 1:30 p.m. in Marshall, Texas.** The parties are directed to meet and confer in accordance with Fed. R. Civ. P. 26(f) prior to the conference. The parties are excused from the requirement of filing a written proposed discovery plan in this case.

Proposed Deadlines for Docket Control Order

The proposed deadlines for docket control order set forth in the attached Appendix A shall be discussed at the Scheduling Conference. The court will not modify the proposed trial date except for good cause shown.

Discovery Order

After a review of the pleaded claims and defenses in this action and in furtherance of the

management of the court's docket under Fed. R. Civ. P. 16, it is ORDERED AS FOLLOWS:

1. **Disclosures.** Except as provided by paragraph 1(h), and, to the extent not already disclosed, within thirty (30) days after the Scheduling Conference, each party shall disclose to every other party the following information:
 - (a) the correct names of the parties to the lawsuit;
 - (b) the name, address, and telephone number of any potential parties;
 - (c) the legal theories and, in general, the factual bases of the disclosing party's claims or defenses (the disclosing party need not marshal all evidence that may be offered at trial);
 - (d) the name, address, and telephone number of persons having knowledge of relevant facts, a brief statement of each identified person's connection with the case, and a brief, fair summary of the substance of the information known by any such person;
 - (e) any indemnity and insuring agreements under which any person or entity carrying on an insurance business may be liable to satisfy part or all of a judgment entered in this action or to indemnify or reimburse for payments made to satisfy the judgment;
 - (f) any settlement agreements relevant to the subject matter of this action;
 - (g) any statement of any party to the litigation;
 - (h) for any testifying expert, by the date set by the court in the Docket Control Order, each party shall disclose to the other party or parties:
 - a. the expert's name, address, and telephone number;
 - b. the subject matter on which the expert will testify;
 - c. if the witness is retained or specially employed to provide expert testimony in the case or whose duties as an employee of the disclosing party regularly

involve giving expert testimony:

- (a) all documents, tangible things, reports, models, or data compilations that have been provided to, reviewed by, or prepared by or for the expert in anticipation of the expert's testimony; and
- (b) the disclosures required by Fed. R. Civ. P. 26(a)(2)(B) and Local Rule CV-26.

- d. for all other experts, the general substance of the expert's mental impressions and opinions and a brief summary of the basis for them or documents reflecting such information;

Any party may move to modify these disclosures for good cause shown.

- 2. **Protective Orders.** Upon the request of any party before or after the Scheduling Conference, the court shall issue the Protective Order in the form attached as Appendix B. Any party may oppose the issuance of or move to modify the terms of the Protective Order for good cause.

- 3. **Additional Disclosures.** In addition to the disclosures required in Paragraph 1 of this Order, at the Scheduling Conference, the court shall amend this discovery order and require each party, without awaiting a discovery request, to provide, to the extent not already provided, to every other party the following:

- (a) the disclosures required by the Patent Rules for the Eastern District of Texas;
- (b) within forty-five (45) days after the Scheduling Conference, a copy of all documents, data compilations, and tangible things in the possession, custody, or control of the party that are relevant to the case, except to the extent these disclosures are affected by the time limits set forth in the Patent Rules for the Eastern District of Texas. By

written agreement of all parties, alternative forms of disclosure may be provided in lieu of paper copies. For example, the parties may agree to exchange images of documents electronically or by means of computer disk; or the parties may agree to review and copy disclosure materials at the offices of the attorneys representing the parties instead of requiring each side to furnish paper copies of the disclosure materials;

- (c) within forty-five (45) days after the Scheduling Conference, a complete computation of any category of damages claimed by any party to the action, making available for inspection and copying as under Rule 34, the documents or other evidentiary material on which such computation is based, including materials bearing on the nature and extent of injuries suffered; and
- (d) within forty-five (45) days after the Scheduling Conference, those documents and authorizations described in Local Rule CV-34; and

The court shall order these disclosures in the absence of a showing of good cause by any party objecting to such disclosures.

4. **Discovery Limitations.** At the Scheduling Conference, the court shall also amend this discovery order to limit discovery in this cause to the disclosures described in Paragraphs 1 and 3 together with 60 interrogatories, 60 requests for admissions, the depositions of the parties, depositions on written questions of custodians of business records for third parties, depositions of three (3) expert witnesses per side and forty (40) hours of additional depositions per side. "Side" means a party or a group of parties with a common interest. Any party may move to modify these limitations for good cause.
5. **Privileged Information.** There is no duty to disclose privileged documents or information.

However, the parties are directed to meet and confer concerning privileged documents or information after the Scheduling Conference. Within sixty (60) days after the Scheduling Conference, the parties shall exchange privilege logs identifying the documents or information and the basis for any disputed claim of privilege in a manner that, without revealing information itself privileged or protected, will enable the other parties to assess the applicability of the privilege or protection. Any party may move the court for an order compelling the production of any documents or information identified on any other party's privilege log. If such a motion is made, the party asserting privilege shall respond to the motion within the time period provided by Local Rule CV-7. The party asserting privilege shall then file with the Court within thirty (30) days of the filing of the motion to compel any proof in the form of declarations or affidavits to support their assertions of privilege, along with the documents over which privilege is asserted for *in camera* inspection. If the parties have no disputes concerning privileged documents or information, then the parties shall inform the court of that fact within sixty (60) days after the Scheduling Conference.

6. **Pre-trial disclosures.** Absent a showing of good cause by any party, the court shall require the following additional disclosures:

Each party shall provide to every other party regarding the evidence that the disclosing party may present at trial as follows:

- (a) The name and, if not previously provided, the address and telephone number, of each witness, separately identifying those whom the party expects to present at trial and those whom the party may call if the need arises.
- (b) The designation of those witnesses whose testimony is expected to be presented by means of a deposition and, if not taken stenographically, a transcript of the pertinent

portions of the deposition testimony.

- (c) An appropriate identification of each document or other exhibit, including summaries of other evidence, separately identifying those which the party expects to offer and those which the party may offer if the need arises.

Unless otherwise directed by the court, these disclosures shall be made at least 30 days before trial. Within 14 days thereafter, unless a different time is specified by the court, a party may serve and file a list disclosing (1) any objections to the use under Rule 32(a) of a deposition designated by another party under subparagraph (B), and (2) any objections, together with the grounds therefor, that may be made to the admissibility of materials identified under subparagraph (c). Objections not so disclosed, other than objections under Rules 402 and 403 of the Federal Rules of Evidence, shall be deemed waived unless excused by the court for good cause shown.

- 7. **Signature.** The disclosures required by this order shall be made in writing and signed by the party or counsel and shall constitute a certification that, to the best of the signer's knowledge, information and belief, such disclosure is complete and correct as of the time it is made. If feasible, counsel shall meet to exchange disclosures required by this order; otherwise, such disclosures shall be served as provided by Fed. R. Civ. P. 5. The parties shall promptly file a notice with the court that the disclosures required under this order have taken place.
- 8. **Duty to Supplement.** After disclosure is made pursuant to this order, each party is under a duty to supplement or correct its disclosures immediately if the party obtains information on the basis of which it knows that the information disclosed was either incomplete or incorrect when made, or is no longer complete or true.

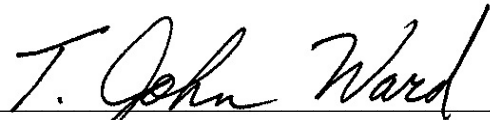
9. **Disputes.**

- (a) Except in cases involving claims of privilege, any party entitled to receive disclosures may, after the deadline for making disclosures, serve upon a party required to make disclosures a written statement, in letter form or otherwise, of any reason why the party entitled to receive disclosures believes that the disclosures are insufficient. The written statement shall list, by category, the items the party entitled to receive disclosures contends should be produced. The parties shall promptly meet and confer. If the parties are unable to resolve their dispute, then the party required to make disclosures shall, within fourteen (14) days after service of the written statement upon it, serve upon the party entitled to receive disclosures a written statement, in letter form or otherwise, which identifies (1) the requested items that will be disclosed, if any, and (2) the reasons why any requested items will not be disclosed. The party entitled to receive disclosures may thereafter file a motion to compel.
- (b) Counsel are directed to contact the chambers of the undersigned for any “hot-line” disputes before contacting the Discovery Hotline provided by Local Rule CV-26(e). If the undersigned is not available, the parties shall proceed in accordance with Local Rule CV-26(e).

- 10. **No Excuses.** A party is not excused from the requirements of this Discovery Order because it has not fully completed its investigation of the case, or because it challenges the sufficiency of another party’s disclosures, or because another party has not made its disclosures. Absent court order to the contrary, a party is not excused from disclosure because there are pending motions to dismiss, to remand or to change venue.

11. **Filings.** Any filings in excess of twenty (20) pages, counsel is directed to provide a courtesy copy to Chambers, simultaneously with the date of filing.
12. **Modifications to Patent Rules.** The attached Appendix C applies to this case and supplements the Patent Rules for the Eastern District of Texas. These modifications are not intended to apply to any other case except as may be expressly provided by order of this Court.

SIGNED this 29th day of January, 2007.

A handwritten signature in black ink, reading "T. John Ward", written over a horizontal line.

T. JOHN WARD
UNITED STATES DISTRICT JUDGE

APPENDIX A

PROPOSED DEADLINES FOR DOCKET CONTROL ORDER

PROPOSED DEADLINES TO BE DISCUSSED AT THE SCHEDULING CONFERENCE MARCH 6, 2007

**Monday,
July 7, 2008**

Jury Selection - 9:00 a.m. in **Marshall, Texas**

June 25, 2008

Pretrial Conference - 9:30 a.m. in **Marshall, Texas**

June 20, 2008

Joint Pretrial Order, Joint Proposed Jury Instructions and Form of the Verdict.

June 20, 2008

Motions in Limine (due three days before final Pre-Trial Conference).

Three (3) days prior to the pre-trial conference provided for herein, the parties shall furnish a copy of their respective Motions in Limine to the Court by facsimile transmission, **903/935-2295**. The parties are directed to confer and advise the Court on or before 3:00 o'clock p.m. the day before the pre-trial conference which paragraphs are agreed to and those that need to be addressed at the pre-trial conference. **The parties shall limit their motions in limine to those issues which, if improperly introduced into the trial of the cause, would be so prejudicial that the Court could not alleviate the prejudice with appropriate instruction(s).**

June 23, 2008

Response to Dispositive Motions (including *Daubert* motions)

June 6, 2008

Notice of Request for Daily Transcript or Real Time Reporting of Court Proceedings. If a daily transcript or real time reporting of court proceedings is requested for trial, the party or parties making said request shall file a notice with the Court and e-mail the Court Reporter, Susan Simmons, at lssimmons@yahoo.com.

June 9, 2008	For Filing Dispositive Motions and any other motions that may require a hearing (including <i>Daubert</i> motions) Responses to dispositive motions filed prior to the dispositive motion deadline, including <i>Daubert</i> Motions, shall be due in accordance with Local Rule CV-7(e). Motions for Summary Judgment shall comply with Local Rule CV56.
May 9, 2008	Defendant to Identify Trial Witnesses
April 9, 2008	Plaintiff to Identify Trial Witnesses
April 9, 2008	Discovery Deadline
<hr/>	30 Days after claim construction ruling Designate Rebuttal Expert Witnesses other than claims construction Expert witness report due Refer to Discovery Order for required information.
<hr/>	15 Days after claim construction ruling Comply with P.R. 3-8.
<hr/>	15 Days after claim construction ruling Party with the burden of proof to designate Expert Witnesses other than claims construction Expert witness report due Refer to Discovery Order for required information.
January 9, 2008	Claim construction hearing 9:00 a.m., Marshall, Texas.
December 17, 2007	Comply with P.R. 4-5(c).
December 10, 2007	Comply with P.R. 4-5(b).

November 26, 2007	Comply with P.R. 4-5(a).
November 1, 2007	Discovery deadline—claims construction issues
October 25, 2007	Respond to Amended Pleadings
October 11, 2007	Amend Pleadings (It is not necessary to file a Motion for Leave to Amend before the deadline to amend pleadings except to the extent the amendment seeks to add a new patent in suit. It is necessary to file a Motion for Leave to Amend after October 11, 2007).
October 11, 2007	Comply with P.R. 4-3.
September 11, 2007	Comply with P.R. 4-2.
August 22, 2007	Comply with P.R. 4-1.
April 23, 2007	Comply with P.R. 3-3.
May 7, 2007	Privilege Logs to be exchanged by parties (or a letter to the Court stating that there are no disputes as to claims of privileged documents).
April 5, 2007	Join Additional Parties
March 16, 2007	Comply with P.R. 3-1

**To be discussed at
Scheduling Conference**

Mediation to be completed

If the parties agree that mediation is an option, the Court will appoint a mediator or the parties will mutually agree upon a mediator. If the parties choose the mediator, they are to inform the Court by letter the name and address of the mediator. The courtroom deputy will immediately mail out a "mediation packet" to the mediator for the case. The mediator shall be deemed to have agreed to the terms of Court Ordered Mediation Plan of the United States District Court of the Eastern District of Texas by going forth with the mediation. General Order 99-2.

March 6, 2007

Scheduling Conference (All attorneys are directed to Local Rule CV-16 for scope of the Scheduling Conference).

The parties are directed to Local Rule CV-7(d), which provides in part that "[i]n the event a party fails to oppose a motion in the manner prescribed herein the court will assume that the party has no opposition." Local Rule CV-7(e) provides that a party opposing a motion has **12 days, in addition to any added time permitted under Fed. R. Civ. P. 6(e)**, in which to serve and file a response and any supporting documents, after which the court will consider the submitted motion for decision.

OTHER LIMITATIONS

1. All depositions to be read into evidence as part of the parties' case-in-chief shall be **EDITED** so as to exclude all unnecessary, repetitious, and irrelevant testimony; **ONLY** those portions which are relevant to the issues in controversy shall be read into evidence.
2. The Court will refuse to entertain any motion to compel discovery filed after the date of this Order unless the movant advises the Court within the body of the motion that counsel for the parties have first conferred in a good faith attempt to resolve the matter. See Eastern District of Texas Local Rule CV-7(h).
3. The following excuses will not warrant a continuance nor justify a failure to comply with the discovery deadline:
 - (a) The fact that there are motions for summary judgment or motions to dismiss pending;

- (b) The fact that one or more of the attorneys is set for trial in another court on the same day, unless the other setting was made prior to the date of this order or was made as a special provision for the parties in the other case;
- (c) The failure to complete discovery prior to trial, unless the parties can demonstrate that it was impossible to complete discovery despite their good faith effort to do so.

APPENDIX B

IN THE UNITED STATES DISTRICT COURT FOR THE EASTERN DISTRICT OF TEXAS MARSHALL DIVISION

FAIRCHILD SEMICONDUCTOR .	§	
CORPORATION, a Delaware corporation,	§	
INTERSIL AMERICAS, INC., a Delaware	§	
corporation, and INTERSIL	§	
CORPORATION, a Delaware corporation	§	
	§	
V.	§	CIVIL NO. 2:06-CV-151(TJW)
	§	
POWER INTEGRATIONS, INC., a	§	
Delaware corporation	§	

STANDARD PROTECTIVE ORDER

The Court, *sua sponte*, issues this Protective Order to facilitate document disclosure and production under the Local Rules of this Court and the Federal Rules of Civil Procedure. Unless modified pursuant to the terms contained in this Order, this Order shall remain in effect through the conclusion of this litigation.

In support of this order, the court finds that:

1. Documents or information containing confidential proprietary and business information and/or trade secrets (“Confidential Information”) that bear significantly on the parties’ claims or defenses is likely to be disclosed or produced during the course of discovery in this litigation;
2. The parties to this litigation may assert that public dissemination and disclosure of Confidential Information could severely injure or damage the party disclosing or producing the Confidential Information and could place that party at a competitive disadvantage;
3. Counsel for the party or parties receiving Confidential Information are presently without

sufficient information to accept the representation(s) made by the party or parties producing Confidential Information as to the confidential, proprietary, and/or trade secret nature of such Confidential Information; and

4. To protect the respective interests of the parties and to facilitate the progress of disclosure and discovery in this case, the following Order should issue:

IT IS THEREFORE ORDERED THAT:

1. Documents or discovery responses containing Confidential Information disclosed or produced by any party in this litigation are referred to as “Protected Documents.” Except as otherwise indicated below, all documents or discovery responses designated by the producing party as “Confidential” and which are disclosed or produced to the attorney’s for the other parties to this litigation are Protected Documents and are entitled to confidential treatment as described below.
2. Protected Documents shall not include (a) advertising materials, (b) materials that on their face show that they have been published to the general public, or (c) documents that have submitted to any governmental entity without request for confidential treatment.
3. At any time after the delivery of Protected Documents, counsel for the party or parties receiving the Protected Documents may challenge the Confidential designation of all or any portion thereof by providing written notice thereof to counsel for the party disclosing or producing the Protected Documents. If the parties are unable to agree as to whether the confidential designation of discovery material is appropriate, the party or parties receiving the Protected Documents shall certify to the Court that the parties cannot reach an agreement as to the confidential nature of all or a portion of the Protected Documents. Thereafter, the party or parties disclosing or producing the Protected Documents shall have ten (10) days

from the date of certification to file a motion for protective order with regard to any Protected Documents in dispute. The party or parties producing the Protected Documents shall have the burden of establishing that the disputed Protected Documents are entitled to confidential treatment. If the party or parties producing the Protected Documents do not timely file a motion for protective order, then the Protected Documents in dispute shall no longer be subject to confidential treatment as provided in this Order. All Protected Documents are entitled to confidential treatment pursuant to the terms of this Order until and unless the parties formally agree in writing to the contrary, a party fails to timely move for a protective order, or a contrary determination is made by the Court as to whether all or a portion of a Protected Document is entitled to confidential treatment.

4. Confidential Treatment. Protected Documents and any information contained therein shall not be used or shown, disseminated, copied, or in any way communicated to anyone for any purpose whatsoever, except as provided for below.
5. Protected Documents and any information contained therein shall be disclosed only to the following persons ("Qualified Persons"):
 - (a) Counsel of record in this action for the party or party receiving Protected Documents or any information contained therein;
 - (b) Employees of such counsel (excluding experts and investigators) assigned to and necessary to assist such counsel in the preparation and trial of this action; and
 - (c) The Court.

Protected Documents and any information contained therein shall be used solely for the prosecution of this litigation.

6. Counsel of record for the party or parties receiving Protected Documents may create an index of the Protected Documents and furnish it to attorneys of record representing or having

represented parties involved in litigation involving the claims alleged in this suit against the party or parties disclosing or producing the Protected Documents. The index may only identify the document, date, author, and general subject matter of any Protected Document, but may not reveal the substance of any such document. Counsel for the party or parties receiving Protected Documents shall maintain a current log of the names and addresses of persons to whom the index was furnished.

7. The term “copy” as used herein means any photographic, mechanical or computerized copy or reproduction of any document or thing, or any verbatim transcript, in whole or in part, of such document or thing.
8. To the extent that Protected Documents or information contained therein are used in depositions, at hearings, or at trial, such documents or information shall remain subject to the provisions of this Order, along with the transcript pages of the deposition testimony and/or trial testimony referring to the Protected Documents or information contained therein.
9. Any court reporter or transcriber who reports or transcribes testimony in this action shall agree that all “confidential” information designated as such under this Order shall remain “confidential” and shall not be disclosed by them, except pursuant to the terms of this Order, and that any notes or transcriptions of such testimony (and any accompanying exhibits) will be retained by the reporter or delivered to counsel of record.
10. Inadvertent or unintentional production of documents or information containing Confidential Information which are not designated “confidential” shall not be deemed a waiver in whole or in part of a claim for confidential treatment.
11. The party or parties receiving Protected Documents shall not under any circumstances sell, offer for sale, advertise, or publicize Protected Documents or any information contained

therein.

12. After termination of this litigation, the provisions of this Order shall continue to be binding, except with respect to those documents and information that become a matter of public record. This Court retains and shall have continuing jurisdiction over the parties and recipients of the Protected Documents for enforcement of the provisions of this Order following termination of this litigation.
13. Upon termination of this action by dismissal, judgment, or settlement, counsel for the party or parties receiving Protected Documents shall return the Protected Documents to the counsel for the party or parties disclosing or producing the Protected Documents. The party or parties receiving the Protected Documents shall keep their attorney work product which refers or relates to any Protected Documents. Attorney work product may be used in subsequent litigation provided that such use does not disclose Protected Documents or any information contained therein.
14. This Order shall be binding upon the parties and their attorneys, successors, executors, personal representatives, administrators, heirs, legal representatives, assigns, subsidiaries, divisions, employees, agents, independent contractors, or other persons or organizations over which they have control.
15. The Court anticipates and encourages the parties to file a motion to modify the terms hereof with respect to the sharing of Protected Documents with experts and consultants; shifting the cost burden of production equitably; and other terms that may be reasonably required to protect a party as provided in Rule 26(b) or (c) of the Federal Rules of Civil Procedure.

So ORDERED AND SIGNED this _____ day of _____, 2007.

T. JOHN WARD
UNITED STATES DISTRICT JUDGE

APPENDIX C

ORDER RELATING TO PATENT CASES BEFORE JUDGE T. JOHN WARD

The Court issues certain modifications to the Eastern District Patent Rules. The modifications relate to three issues: (1) Notice Requirements, (2) Infringement and Invalidity Contentions for Software, and (3) Deadlines Related to Claim Construction.

I. Notice Requirements

The Court has seen a dramatic increase in the number of disputes related to parties serving “supplemental,” “additional,” or “revised” P.R. 3-1 or P.R. 3-3 disclosures. In the past, parties were not required to provide notice to the Court regarding compliance with P.R. 3-1 or P.R. 3-3. Thus, certain parties attempted to avoid the rule that Preliminary Contentions are final except as provided in P.R. 3-6 and P.R. 3-7. Accordingly, the Court modifies P.R. 3-1 and P.R. 3-3 in the following manner:

P.R. 3-1(g): Any time a party claiming patent infringement serves Preliminary Infringement Contentions on an opposing party, the party claiming patent infringement shall also file with the Court a Notice of Compliance with P.R. 3-1.

P.R. 3-3(e): Any time a party opposing patent infringement serves Preliminary Invalidity Contentions on an opposing party, the party opposing patent infringement shall also file with the Court a Notice of Compliance with P.R. 3-3.

Under this Court’s interpretation of the Patent Rules, leave of Court is required for serving “amended,” “supplemental,” or “revised” P.R. 3-1 or P.R. 3-3 disclosures. The Court will strike “amendments,” “supplements,” or “revisions” of P.R. 3-1 or P.R. 3-3 disclosures that do not comply with P.R. 3-6 or P.R. 3-7.

II. Infringement and Invalidity Contentions for Software

Additional modifications to the Patent Rules regarding P.R. 3-1 and P.R. 3-3 are being made

to reduce discovery disputes and motion practice resulting from patents that contain software claim limitations. The Patent Rules require a party asserting claims of patent infringement to take a firm position in the litigation as it relates to infringement early on in the case. This and other courts in the Eastern District of Texas, however, recognize that software claim limitations present unique challenges for the parties because parties claiming patent infringement do not typically have access to an opposing party's source code before filing suit. At the same time, parties opposing a claim for patent infringement are hampered in their ability to prepare a defense absent specific infringement contentions from the party asserting claims of patent infringement.

The lack of access to source code coupled with an opponent's right to prepare a defense has led to numerous discovery disputes. To alleviate these disputes and to provide clear direction to the parties as to their rights and responsibilities under the Patent Rules, the Court modifies the Patent Rules in a manner consistent with such cases as *American Video Graphics, L.P. v. Electronic Arts, Inc.*, 359 F. Supp. 2d 558 (E.D. Tex. 2005).

The Court's modifications to P.R. 3-1 and P.R. 3-3 are set out below.

P.R. 3-1 (h): If a party claiming patent infringement asserts that a claim element is a software limitation, the party need not comply with P.R. 3-1 for those claim elements until 30 days after source code for each Accused Instrumentality is produced by the opposing party. Thereafter, the party claiming patent infringement shall identify, on an element-by-element basis for each asserted claim, what source code of each Accused Instrumentality allegedly satisfies the software limitations of the asserted claim elements.

P.R. 3-3(f): If a party claiming patent infringement exercises the provisions of P.R. 3-1(g), the party opposing a claim of patent infringement may serve, not later than 30 days after receipt of a P.R. 3-1(g) disclosure, supplemental "Preliminary Invalidity Contentions" that amend only those claim elements identified as software limitations by the party claiming patent infringement.

Thus, if a party claiming patent infringement asserts that a claim element (or the entire claim) is software, that party need only identify the element as a software limitation in its initial compliance

with P.R. 3-1, but does not need to identify where such limitation is met in the Accused Instrumentality. After receipt of the source code for an Accused Instrumentality, the party is permitted 30 days to supplement its P.R. 3-1 disclosure to identify, with specificity, the source code of the Accused Instrumentality that allegedly satisfies the software claim elements. P.R. 3-1(g) does not allow Plaintiff the opportunity to modify or amend any non-software claim contentions.

Likewise, once a party opposing a claim of patent infringement is in receipt of a P.R. 3-1(g) disclosure, the party is allowed 30 days to modify its initial P.R. 3-3 disclosures, but only to the extent the modifications relate to the software claim elements identified by the party claiming patent infringement. P.R. 3-3(e) does not allow a party opposing a claim of infringement an opportunity to modify or amend any non-software contentions.

III. Claim Construction Deadlines

The final amendments to the Patent Rules relate to claim construction deadlines. In the Eastern District Patent Rules, claim construction deadlines are triggered by the filing of the parties' Infringement and Invalidity Contentions. The increase of patent cases before this Court has resulted in a large number of Claim Construction hearings and, as a result, strict application of the Patent Rules yields a P.R. 4-5 deadline approximately three months or more before Court could accommodate a Claim Construction Hearing.

To facilitate the case, resolve discovery disputes, and have claim construction hearings a reasonable time after briefing is complete, the Court modifies the deadlines in P.R. 4-1 and P.R. 4-3 as set forth below:

4-1. Exchange of Proposed Terms and Claim Elements for Construction.

(a) Not later than *140 days before the date set for the Claim Construction Hearing*, each party shall simultaneously exchange a list of claim terms, phrases, or clauses which that party contends should be construed by the Court, and identify any claim element which that party contends should be governed by 35 U.S.C. § 112(6).

4-3. Joint Claim Construction and Prehearing Statement.

Not later than *30 days after “Exchange of Preliminary Claim Constructions and Extrinsic Evidence” in compliance with P.R. 4.2*, the parties shall complete and file a Joint Claim Construction and Prehearing Statement, which shall contain the following information:

Thus, the Court’s modifications will make the trigger of P.R. 4-1 through P.R. 4-5 the date of the Claim Construction Hearing. For clarification, the Court notes that the “140 days” set forth in P.R. 4-1 was not chosen to confuse the parties but was instead chosen so as to be evenly divisible by 7. Thus, whatever the date of the Claim Construction Hearing, the deadline for complying with P.R. 4-1 will always fall on a weekday. If that weekday is a Federal Holiday, the deadline for complying with P.R. 4-1 is extended to the first day that is not a Saturday, Sunday or other Federal Holiday.

Appendix K

Revised: 12/3/03

UNITED STATES DISTRICT COURT
EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION
APPLICATION TO APPEAR PRO HAC VICE

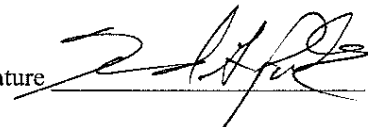
FILED CLERK
U.S. DISTRICT COURT
2007 JAN 29 PM 4:09
TEXAS EASTERN

1. This application is being made for the following: Case #2:06-cv-00151 TJW
Style: Fairchild Semiconductor Corporation, et al. v. Power Integrations, Inc.
2. Applicant is representing the following party/ies:
Power Integrations, Inc.
3. Applicant was admitted to practice in California (state) on December 22, 1992 (date).
4. Applicant is in good standing and is otherwise eligible to practice law before this court.
5. Applicant is not currently suspended or disbarred in any other court.
6. Applicant has not had an application for admission to practice before another court denied please circle appropriate language. If so, give complete information on a separate page.
7. Applicant has not ever had the privilege to practice before another court suspended (please circle). If so, give complete information on a separate page.
8. Applicant has not been disciplined by a court or Bar Association or committee thereof that would reflect unfavorably upon applicant's conduct, competency or fitness as a member of the Bar (please circle). If so, give complete information on a separate page.
9. Describe in detail on a separate page any charges, arrests or convictions for criminal offense(s) filed against you. Omit minor traffic offenses.
10. There are no pending grievances or criminal matters pending against the applicant.
11. Applicant has been admitted to practice in the following courts:
California Supreme Court, December 22, 1992; Federal Circuit Court of Appeals, August 2, 1994; United States District Court, Northern District of California, March 2, 1995; United States District Court, Eastern District of California, March 29, 1999; United States District Court, Central District of California, June 5, 1995.
12. Applicant has read and will comply with the Local Rules of the Eastern District of Texas, including Rule AT-3, the "Standards of Practice to be Observed by Attorneys."
13. Applicant has included the requisite \$25 fee (see Local Rule AT-1(d)).
14. Applicant understands that he she is being admitted for the limited purpose of appearing in the case specified above only.

Application Oath:

I, Howard G. Pollack do solemnly swear (or affirm) that the above information is true; that I will discharge the duties of attorney and counselor of this court faithfully; that I will demean myself uprightly under the law and the highest ethics of our profession; and that I will support and defend the Constitution of the United States.

Date 1/26/07

Signature 

Appendix K

Revised: 12/3/03

Name (please print) _____
State Bar Number 162897
Firm Name: FISH & RICHARDSON P.C.
Address/P.O. Box: 500 Arguello Street, Suite 500
City/State/Zip: Redwood City, California 94063
Telephone #: (650) 839-5070
Fax #: (650) 839-5071
E-mail Address: pollack@fr.com
Secondary E-Mail Address: _____

Applicant is authorized to enter an appearance as counsel for the party/parties listed above. This application has been approved for the court this ____ day of _____, 20 ____.

David J. Maland, Clerk
U.S. District Court, Eastern District of Texas

By _____

Deputy Clerk

United States District Court

for the

Eastern District of Texas at Tyler

Date: Monday, January 29, 2007

Received from:

POTTER MINTON
P.O. BOX 359
TYLER, TX 75710

<u>Account</u>	<u>Amount</u>
6855XX	\$25.00
Total	\$25.00

<u>Account</u>	<u>Description</u>
085000	- Attorney Admission Fees
086400	- New Case Fee
086900	- Filing Fees
121000	- Conscience Fund
129900	- Gifts
143500	- Interest
322340	- Sale of Publications
322350	- Copy Fees
322360	- Miscellaneous Fees
322380	- Recoveries of Court Costs
322386	- Cost of Prosecution
504100	- Crime Victims Fund
508800	- Immigration Fees
510000	- Civil Filing Fee (1/2)
5100PL	- Partial Filing Fee (PLRA)
510100	- Registry Fee
604700	- Registry Funds/General and Special Funds
613300	- Unclaimed Monies
6855XX	- Deposit Funds

Payment method: Check
Case or other reference: 2:06CV151
Comments: PHV APPLICATION FOR HOWARD G. POLLACK - FIRM CK 066043

Received by: MC

Appendix K

Revised: 12/3/03

UNITED STATES DISTRICT COURT
EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION
APPLICATION TO APPEAR PRO HAC VICE

FILED CLERK
U.S. DISTRICT COURT

2007 JAN 29 PM 4:09

TEXAS EASTERN

BY BW

- 1 This application is being made for the following: Case #2:06-cv-00151 TJW
Style: Fairchild Semiconductor Corporation, et al. v. Power Integrations, Inc.
- 2 Applicant is representing the following party/ies:
Power Integrations, Inc.
- 3 Applicant was admitted to practice in California (state) on December 22, 1992 (date)
- 4 Applicant is in good standing and is otherwise eligible to practice law before this court
- 5 Applicant is not currently suspended or disbarred in any other court
- 6 Applicant has not had an application for admission to practice before another court denied please circle appropriate language If so, give complete information on a separate page.
- 7 Applicant has not ever had the privilege to practice before another court suspended (please circle). If so, give complete information on a separate page
- 8 Applicant has not been disciplined by a court or Bar Association or committee thereof that would reflect unfavorably upon applicant's conduct, competency or fitness as a member of the Bar (please circle) If so, give complete information on a separate page.
- 9 Describe in detail on a separate page any charges, arrests or convictions for criminal offense(s) filed against you. Omit minor traffic offenses
- 10 There are no pending grievances or criminal matters pending against the applicant
- 11 Applicant has been admitted to practice in the following courts:
California Supreme Court, December 22, 1992; Federal Circuit Court of Appeals, August 2, 1994; United States District Court, Northern District of California, March 2, 1995; United States District Court, Eastern District of California, March 29, 1999; United States District Court, Central District of California, June 5, 1995.
- 12 Applicant has read and will comply with the Local Rules of the Eastern District of Texas, including Rule AT-3, the "Standards of Practice to be Observed by Attorneys "
- 13 Applicant has included the requisite \$25 fee (see Local Rule AT-1(d))
- 14 Applicant understands that he she is being admitted for the limited purpose of appearing in the case specified above only

Application Oath:

I, Howard G. Pollack do solemnly swear (or affirm) that the above information is true; that I will discharge the duties of attorney and counselor of this court faithfully; that I will demean myself uprightly under the law and the highest ethics of our profession; and that I will support and defend the Constitution of the United States.

Date

1/26/07

Signature

[Signature]

SCANNED


Appendix K

Revised: 12/3/03

Name (please print) _____
State Bar Number 162897
Firm Name: FISH & RICHARDSON P.C.
Address/P.O. Box: 500 Arguello Street, Suite 500
City/State/Zip: Redwood City, California 94063
Telephone #: (650) 839-5070
Fax #: (650) 839-5071
E-mail Address: pollack@fr.com
Secondary E-Mail Address: _____

Applicant is authorized to enter an appearance as counsel for the party/parties listed above. This application has been approved for the court this 29 day of Jan, 2007.

David J. Maland, Clerk
U.S. District Court, Eastern District of Texas

By 

Deputy Clerk

**UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION**

**FAIRCHILD SEMICONDUCTOR
CORPORATION, a Delaware corporation,
INTERSIL AMERICAS, INC., a Delaware
corporation and INTERSIL
CORPORATION,
a Delaware corporation
Plaintiffs,**

V.

**POWER INTEGRATIONS, INC., a
Delaware corporation.
Defendant**

2:06-cv-151 (TJW)

**NOTICE OF APPEARANCE OF ADDITIONAL COUNSEL
FOR DEFENDANT POWER INTEGRATIONS, INC.**

Defendant POWER INTEGRATIONS, INC. (“POWER INTEGRATIONS”) files this Notice of Appearance of Additional Counsel, and hereby notifies the Court that J. Matt Rowan of the law firm Potter Minton, A Professional Corporation, 110 N. College, Suite 500, Tyler, Texas 75702, is appearing as additional counsel for POWER INTEGRATIONS in the above-referenced matter. All pleadings, discovery, correspondence and other material should be served upon counsel at the address referenced above.

Respectfully submitted,

/s/ J. Matt Rowan

J. Matt Rowan
State Bar No. 24033137
A43@potterminton.com
POTTER MINTON
A Professional Corporation
110 N. College, Suite 500
Tyler, Texas 75702
903/597-8311
903/593-0846 Facsimile

ATTORNEYS FOR POWER
INTEGRATIONS, INC.

CERTIFICATE OF SERVICE

I hereby certify that all counsel of record who have consented to electronic service and are being served with a copy of this document via the Court's CM/ECF system per Local Rule CV-5(a)(3) on this the 31st day of January, 2007. Any other counsel of record will be served by first class mail on this same date.

/s/ J. Matt Rowan

J. Matt Rowan

Appendix K

Revised: 12/3/03

UNITED STATES DISTRICT COURT
EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION
APPLICATION TO APPEAR PRO HAC VICE

FILED-CLERK
U.S. DISTRICT COURT

2007 MAR -1 PM 3: 37

TX EASTERN-MARSHALL

BY 

1. This application is being made for the following: Case No.:# 2-06CV-151

Style: Fairchild Semiconductor Corporation and Intersil Corporation v. Power Integrations

2 Applicant is representing the following party/ies: Fairchild Semiconductor Corporation

3. Applicant was admitted to practice in California on July 19, 1995. Applicant is in good standing and is otherwise eligible to practice law before this court.

5 Applicant is not currently suspended or disbarred in any other court

6. Applicant ~~has~~/has not had an application for admission to practice before another court denied (please circle appropriate language) If so, give complete information on a separate page.

7. Applicant ~~has~~ /has not ever had the privilege to practice before another court suspended (please circle). If so, give complete information on a separate page.

8. Applicant ~~has~~ /has not been disciplined by a court or Bar Association or committee thereof that would reflect unfavorably upon applicant's conduct, competency or fitness as a member of the Bar (please circle). If so, give complete information on a separate page.

9. Describe in detail on a separate page any charges, arrests or convictions for criminal offense(s) filed against you. Omit minor traffic offenses.

10. There are no pending grievances or criminal matters pending against the applicant.

11. Applicant has been admitted to practice in the following courts:

Northern District of California, Central District of California, U.S. Court of Appeals for Fed. Circuit.

12. Applicant has read and will comply with the Local Rules of the Eastern District of Texas, including Rule AT-3, the "Standards of Practice to be Observed by Attorneys."

13. Applicant has included the requisite \$25 fee (see Local Rule AT-1(d)).

14. Applicant understands that he/she is being admitted for the limited purpose of appearing in the case specified above only.

Appendix K

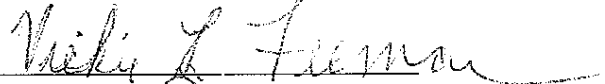
Revised: 12/3/03

Application Oath:

I, Vickie L. Feeman, do solemnly swear (or affirm) that the above information is true; that I will discharge the duties of attorney and counselor of this court faithfully; that I will demean myself uprightly under the law and the highest ethics of our profession; and that I will support and defend the Constitution of the United States.

Date: February 28, 2007

Signature



Name: Vickie L. Feeman

State Bar Number: 177487

Firm Name: Orrick, Herrington & Sutcliffe LLP

Address/P. O. Box: 1000 Marsh Road

City/State/Zip: Menlo Park, CA 94025

Telephone #: (650) 614-7400

Fax #: (650) 614-7401


E-mail Address: vfeeman@orrick.com

Applicant is authorized to enter an appearance as counsel for the party/parties listed above. This application has been approved for the court this 1 day of Mar, 2007.

David J. Maland, Clerk

U.S. District Court, Eastern District of Texas

By



Deputy Clerk

Receipt for Payment

Receipt No: 2-1-0002318

United States District Court

for the

Eastern District of Texas at Marshall

Date: **Thursday, March 1, 2007**

Received from:

**ROTH LAW FIRM
MARSHALL, TX**

<u>Account</u>	<u>Amount</u>
6855XX	\$50.00
Total	\$50.00

<u>Account</u>	<u>Description</u>
085000	- Attorney Admission Fees
086400	- New Case Fee
086900	- Filing Fees
121000	- Conscience Fund
129900	- Gifts
143500	- Interest
322340	- Sale of Publications
322350	- Copy Fees
322360	- Miscellaneous Fees
322380	- Recoveries of Court Costs
322386	- Cost of Prosecution
504100	- Crime Victims Fund
508800	- Immigration Fees
510000	- Civil Filing Fee (1/2)
5100PL	- Partial Filing Fee (PLRA)
510100	- Registry Fee
604700	- Registry Funds/General and Special Funds
613300	- Unclaimed Monies
6855XX	- Deposit Funds

Payment method: **Check**
Case or other reference: **2:06cv151 PHV Feeman VanderZanden**
Comments: **CK 20364**

Received by: pa

SHORECHAN
BRAGALONE_{LLP}

Michael W. Shore
Republic Center
325 North Saint Paul Street
Suite 4450
Dallas, Texas 75201
214.593.9140 Direct Dial
214.593.9111 Facsimile
shore@shorechan.com

March 5, 2007

EMAIL PDF FORMAT

Michael Headley, Esq.
Fish & Richardson PC
500 Arguello Street-Suite 500
Redwood City, California 94063

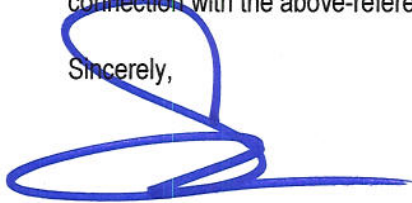
Re: Fairchild Semiconductor Corporation, Intersil Americas, Inc., and Intersil Corporation
vs. Power Integrations, Inc., United States District Court, Eastern District of Texas,
Marshall Division, Case No. 2:06-CV-151 TWJ

Dear Counsel:

I am scheduled to be out of the office on vacation for the period March 10-17, 2007.

I would kindly request that the Court and all counsel of record not schedule any hearings or depositions in connection with the above-referenced matter during this time period.

Sincerely,



Michael W. Shore

IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

FAIRCHILD SEMICONDUCTOR §
CORPORATION, ET AL.

VS. § CIVIL ACTION NO. 2:06-CV-151

POWER INTEGRATIONS, INC. §

MEMORANDUM OPINION AND ORDER

The court grants in part and denies in part Power Integrations, Inc.’s motion to dismiss or, in the alternative, to transfer this case to Delaware (#20).

On October 20, 2004, Power Integrations, Inc. (“Power Integrations”) sued Fairchild Semiconductor International, Inc. and Fairchild Semiconductor Corporation (collectively, “Fairchild”) for patent infringement in the District Court for the District of Delaware. In the Delaware litigation, Power Integrations asserts four patents against Fairchild. One of the patents is U.S. Patent No. 4,811,075 (“the ‘075 patent”). In the Delaware case, Fairchild contends that the ‘075 patent is invalid over U.S. Patent No. 5,264,719 (“the ‘719 patent”). With respect to the ‘719 patent, one of the disputes is whether it is prior art to the ‘075 patent.

Intersil Corporation (“Intersil”) owns the ‘719 patent. During the pendency of the Delaware case, Fairchild Semiconductor Corporation acquired from Intersil “the sole and exclusive right, exclusive even as to Intersil, to enforce” the ‘719 patent against Power Integrations (and only Power Integrations). Intersil and Fairchild Semiconductor Corporation then filed the present suit in this court against Power Integrations, asserting infringement of the ‘719 patent.

Power Integrations has filed a motion in this court to dismiss the case for lack of standing or, alternatively, to transfer the case to Delaware under the first-to-file rule and/or 28 U.S.C. § 1404(a).¹ The court declines to reach the standing arguments. Instead, the court finds that this case should be transferred under the first-to-file rule.

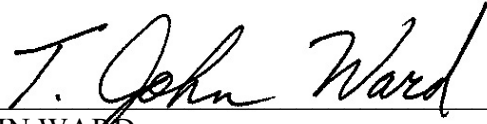
There is a substantial overlap in parties. The real parties in interest to this case are Fairchild Semiconductor Corporation and Power Integrations. These parties are involved in the Delaware case. As a result, there is a substantial overlap, notwithstanding the addition of Intersil as a party plaintiff.

There is also a substantial overlap in the subject matter of the two suits. Like the Delaware case, the question of who was first to invent the technology in the '719 patent is presented in this case. In addition, in the Delaware case, Power Integrations will seek to prove that its products embody the claims of its '075 patent to show commercial success. Fairchild will likely accuse those same products of infringing the claims of the '719 patent in the present case. The issues in the two cases substantially overlap.

In view of the overlapping parties and subject matter, the Delaware court is the first-filed court. *Mann Mfg., Inc. v. Hortex*, 439 F.2d 403 (5th Cir. 1971). The court therefore grants in part and denies in part the defendant's motion to dismiss or, in the alternative, to transfer this case to Delaware (#14). The court transfers this case to the District of Delaware for the reasons assigned herein.

¹ As to the standing argument, Power Integrations contends that Fairchild is not an exclusive licensee and thus has no standing to sue on the '719 patent. In addition, Power Integrations contends that Intersil has no standing because, by virtue of the license, it conveyed away to Fairchild any right to sue Power Integrations.

SIGNED this 6th day of March, 2007.

A handwritten signature in black ink, reading "T. John Ward", is written over a horizontal line.

T. JOHN WARD
UNITED STATES DISTRICT JUDGE